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Assessing the forming temperature role on amorphous and polycrystalline HfO_2-based 4kbit RRAM arrays performance

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Abstract

The impact of temperature during the forming operation on the electrical cells performance and the post-programming stability were evaluated in amorphous and polycrystalline HfO_2-based arrays. Forming (between -40 and 150 ºC), reset and set (at room temperature) operations were applied using the incremental step pulse with verify algorithm (ISPVA). The improvements achieved on the forming operation in terms of time and voltages reduction do not impact on the subsequent reset/set results. ISPVA perturbations in LRS/HRS current distributions are almost negligible after the first reset/set operation. In this study the best improvement in forming operation is achieved in polycrystalline samples at 80 ºC.

Keywords

RRAM, 4kbit-array, amorphous HfO_2, polycrystalline HfO_2, temperature impact, forming

1. Introduction

Resistive Random Access Memories (RRAM) based on HfO_2 is one of the most promising technology candidates for replacing Flash memories [1]. This technology has shown fast low-power switching operations, high-integration density [2], and compatibility with CMOS processes [3]. The choice of a proper Metal-Insulator-Metal (MIM) technology for RRAM cells, exhibiting good uniformity and low switching voltages, is still a key issue for array structures fabrication and reliable electrical operation. Such a process step is mandatory to bring this technology to a maturity level.

RRAM behavior is based on the electrical modification of the conductance of a MIM stack: the set operation moves the cell into a Low Resistive State (LRS), whereas reset operation brings the cell back to a High Resistive State (HRS) [4]. In order to activate the resistive switching behavior, the RRAM cells require a preliminary forming operation [3]. This initial operation plays a fundamental role in determining the subsequent devices performance [5].

In this work, the forming operation was performed at different temperatures on 4kbits arrays in order to study its impact on the cells performance and on the post-programing stability. Amorphous and polycrystalline HfO_2-based cells were characterized in order to figure out whether the dielectric technology plays a fundamental role in the results.

2. Experimental

The measurements were performed on 4 kbits memory devices, as Fig. 1(a) shows. Each cell is a 1T-1R RRAM single device constituted by a select NMOS transistor manufactured in 0.25 µm BiCMOS technology. Such a transistor also sets the current compliance. Its drain is in series to a variable resistor connected to the bitline (BL). The variable resistor is a MIM device integrated on the metal line 2 of the CMOS process. The cross-sectional TEM image of the integrated RRAM cell is shown in Fig. 1(b). The MIM resistor is a $TiN/HfO_2/Ti/TiN$ stack of 150 nm TiN layers deposited by magnetron sputtering, a 7 nm Ti layer (under TiN top electrode), and an 8 nm HfO_2 layer grown by two different Atomic Vapor Deposition (AVD) processes resulting either in amorphous (A-array) and polycrystalline (P-array) HfO_2 films. The resistor area is equal to 0.4 μm^2.

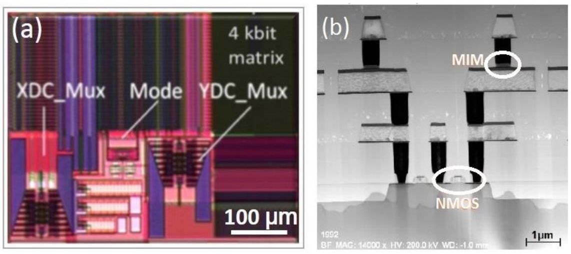

Fig.1: Photo of 4kbit memory array (a) and cross-sectional TEM image of the 1T-1R integrated cell (b).

In order to control the formation and rupture of the conductive filament (CF), the Incremental Step Pulse with Verify Algorithm (ISPVA) [6] is applied instead of a simple DC voltage sweep [7]. The ISPVA technique consists of a sequence of increasing voltage pulses (Fig. 2) on the BL during set and forming operations, whereas this sequence is applied on the source line (SL) during reset operation: t_{pulse} = 10 µs, $t_{fall/rise}$ = 1 µs. The amplitude of the pulses in reset and set operations ranges between V_{pulse} = 0.2−3 V increasing with 0.1 V, whereas in forming ranges between V_{pulse} = 2−5 V increasing with 0.01 V. The applied transistor gate voltage values through the wordline (WL) were 2.7 V for reset and 1.4 V for set and forming. After every pulse a Read-verify operation is performed with V_{WL} = 1.4 V, V_{read} = 0.2 V (applied over the BL) for 10 µs. When the Read current reaches the target value of 18 µA the set and forming operations are stopped, whereas the reset operation is stopped when the target value of 6 µA is achieved. Forming operation was performed in the temperature range from -40 to +150 ºC, whereas reset and set operations were performed at room temperature.

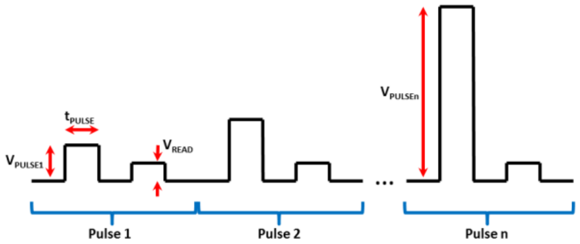

Fig.2: Schematic illustration of the Incremental Step Pulse with Verify Algorithm (ISPVA).

3. Results and discussion

The impact of the temperature onto the forming yield (defined as the cell percentage showing a read verify current after forming over 18 μA) in A-array and P-array is illustrated in Fig. 3. A-array shows a strong temperature dependency, the yield is increasing with raising temperature, achieving a value of about 95 % at 150 ºC. In contrast, the yield in P-array is almost temperature independent, achieving its best value (about 96 %) at 80 ºC.

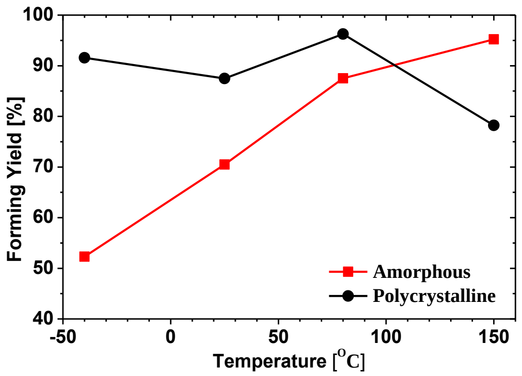

Fig.3: Forming Yield as function of temperature in Amorphous and Polycrystalline arrays.

Fig. 4 shows the cumulative distributions of the currents just after the filament forming. Although in both arrays higher temperatures lead to more compact distributions of currents, this temperature impact is stronger in A-array. According to Raghavan [8] grain boundaries (GB) in polycrystalline oxides serve as a sink of oxygen vacancies to segregate to. Therefore, in P-array the percolation path formation depends more strongly on the GB distribution, whereas in A-array the thermal excitation in the oxide matrix plays a more fundamental role. The nMOS transistor integrated in the 1T-1R device was investigated separately in Perez et al [9]. Its results ensure that the temperature impact on the current characteristics is solely caused by the MIM resistor.

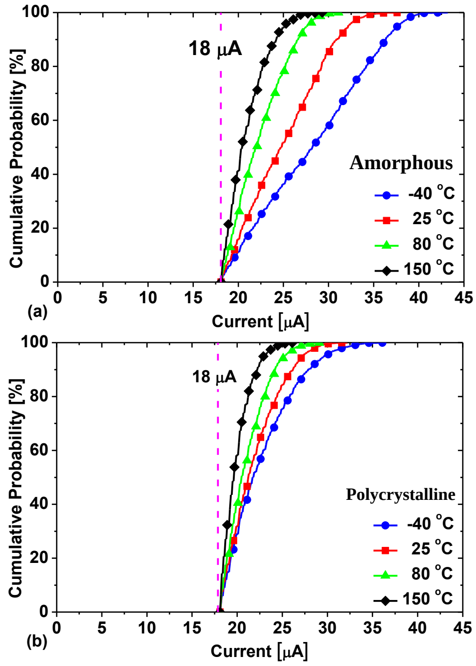

Fig.4: Current cumulative probabilities just after forming at the selected temperature values in A-array (a) and P-array (b).

Fig. 5 illustrates the cumulative distributions of the forming voltages. The voltages required to form the cells in A-array decrease with temperature, but independently of the temperature these distributions remain between 3 and 5 V. A similar temperature trend is shown in P-array below 80 ºC. In contrast to the A-array, at 80 ºC the number of cells formed achieves almost 100 % using voltages lower than 3 V.

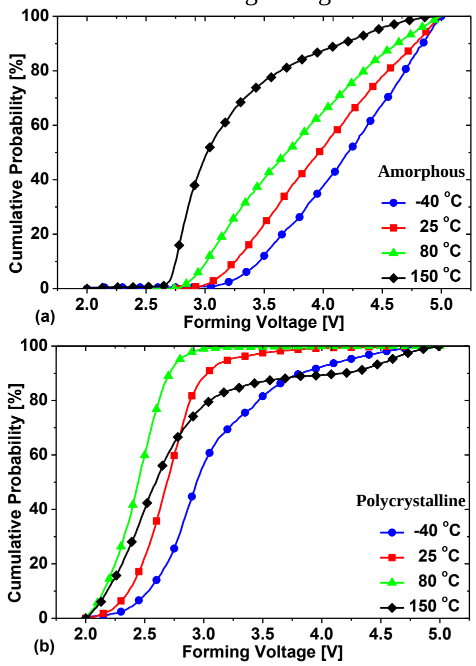

Fig.5: Forming voltage cumulative probabilities at the selected temperature values in A-array (a) and P-array (b).

Increasing the temperature during the forming step supports the CF formation (especially in P-array) and reduces the cell-to-cell variability leading to narrower current distributions [10].

However, as shown in Fig. 6 and 7, the temperature dependencies found in forming operation disappear after the first reset/set operation at room temperature. Current and voltage distributions are essentially the same regardless of the forming temperature. Therefore, the time consumption of forming operation can be strongly reduced increasing the temperature with no impact in the subsequent cells performance. The optimal conditions for the forming operation were found in P-Array at 80 ºC, with the best forming yield and the strongest reduction of forming voltages.

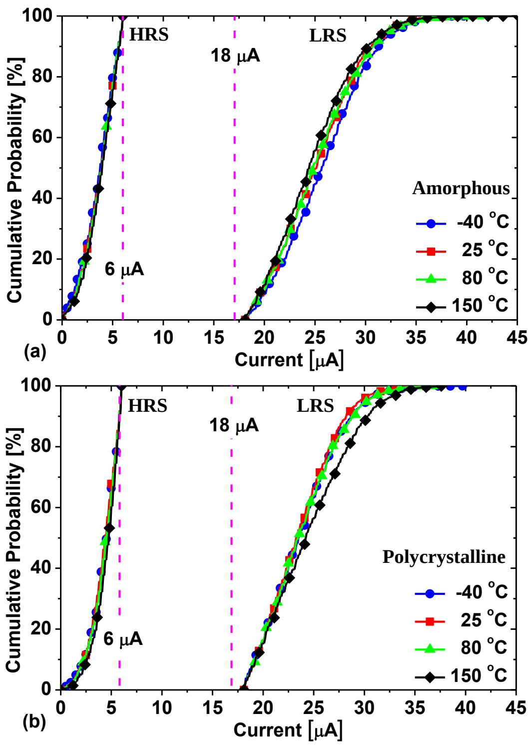

Fig.6: HRS and LRS current cumulative probabilities after reset and set operations, respectively, in A-array (a) and P-array (b).

In order to evaluate the post-programming stability, a read-out operation is performed at the end of the ISPVA in forming, reset and set operations [11]. The current distributions in forming are illustrated in Fig. 8. In both A-array and P-array a few so-called cross-bit cells (cells which current values shifted beyond the threshold value) are detected. The number of cross-bit cells is more impacted by temperature in A-array than in P-array. This result is in line with the temperature dependence of current distributions previously reported.

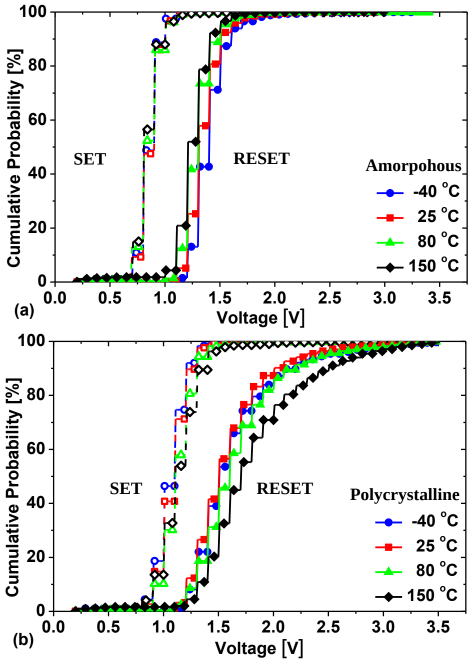

Fig.7: Reset and set voltage cumulative probabilities at the selected temperature, respectively, in A-array (a) and P-array (b).

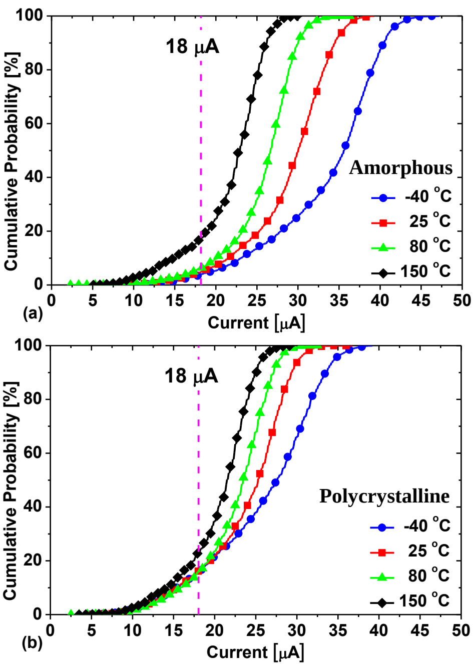

Fig.8: Current cumulative probabilities at the end of ISPVA forming operation, respectively, in A-array (a) and P-array (b).

However, these ISPVA perturbations in LRS current distributions almost disappear after the first reset/set operation at room temperature, as shown in Fig. 9. For instance, a reduction of about 15 % takes place in P-array. In the HRS this value remains always below 5 %. Therefore, post-programming ISPVA pulses applied on the cells do not have any remarkable impact in the performance.

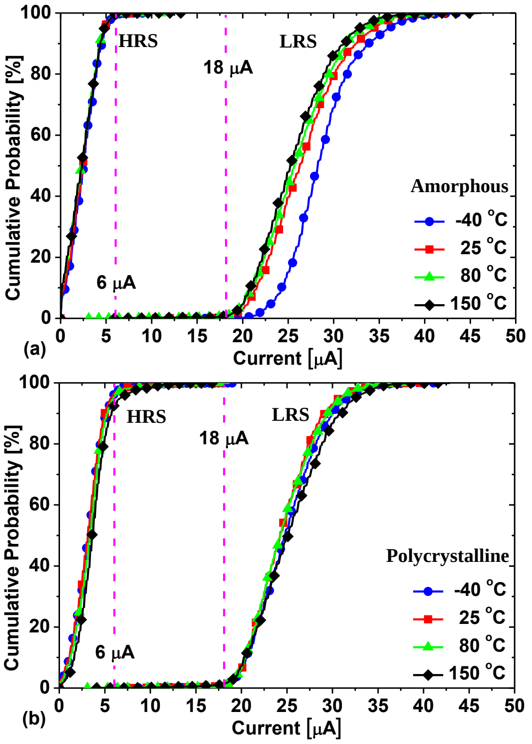

Fig.9: HRS and LRS current cumulative probabilities at the end of ISPVA reset and set operation, respectively, in A-array (a) and P-array (b).

4. Conclusions

The impact of temperature on the electrical cell performance during the forming operation has been investigated in 4kbits HfO_2-based arrays. Increasing the temperature, the forming yield is improved, the cell-to-cell variability reduced and the voltage values required to create the CF are lower. After the first reset/set operation the impact of temperature and post-programmed current shift disappears, namely cells performance is not effectively impacted by the temperature used during the forming operation. Therefore, the time required by the forming can be reduced raising temperature with no impact in the cells performance. P-array shows the best results achieved at 80 ºC.

Acknowledgements

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