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Multispectral Terahertz and Visible Imaging in CMOS Technology

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Declaration of originality

The work described in this thesis is original and result of my own activity or joint efforts performed in the IRIS research team of FBK. In particular:

- The FET modeling has been carried out completely by myself, while validating measurements have been taken together with former PhD student Muhammad Ali;
- The multispectral imaging device has been conceived by myself, simulated and designed together with former PhD student Moustafa Khatib, while measurements and the data processing have been completely performed by myself;
- The SEBAT THz detector has been conceived, designed and tested entirely by myself, with the suggestions and guidance of prof. Lucio Pancheri, with the latest THz measurements taken by PhD student Gabriele Quarta;
- The graphene THz detectors have been implemented within the Graphene Flagship, where the chips have been designed and tested by myself and FBK researcher Luca Parmesan, while the graphene processing has been realized by the colleagues of Pisa.

Parts of this work have been published in the scientific literature:

M. Khatib, *M. Perenzoni*, “A Low-Noise Direct Incremental A/D Converter for FET-Based THz Imaging Detectors,” Sensors. 2018; 18(6):1867.

M. Khatib and *M. Perenzoni*, “Response Optimization of Antenna-Coupled FET Detectors for 0.85-to-1-THz Imaging,” in IEEE Microwave and Wireless Components Letters, vol. 28, no. 10, pp. 903-905, Oct. 2018, doi: 10.1109/LMWC.2018.2860794.

M. Ali, and *M. Perenzoni*, “A Readout Channel Optimized for Minimum NEP of a FET-Based THz Pixel.” Journal of Infrared, Millimeter, and Terahertz Waves 39.12 (2018): 1221-1235.

M. Perenzoni, and M. Khatib, “A CMOS Multispectral Imager with Terahertz and Visible Pixels,” 2019 44th International Conference on Infrared, Millimeter, and Terahertz Waves (IRMMW-THz), Paris, France, 2019, pp. 1-1, doi: 10.1109/IRMMW-THz.2019.8874565.

F. Bianco, V. Mišeikis, D. Perenzoni, C. Coletti, *M. Perenzoni* and A. Tredicucci, "Antenna-Coupled Graphene Field-Effect Transistors as a Terahertz Imaging Array," in IEEE Transactions on Terahertz Science and Technology, vol. 11, no. 1, pp. 70-78, Jan. 2021, doi: 10.1109/TTHZ.2020.3021353.

M. Perenzoni, M. Ali, G. Pepponi and V. Guidi, "A Compact Current- and Voltage-Mode Model of Antenna-Coupled FET Terahertz Detectors," in IEEE Transactions on Electron Devices, vol. 68, no. 2, pp. 471-478, Feb. 2021, doi: 10.1109/TED.2020.3042450.

1 INTRODUCTION

Among the five senses, sight is often considered as the most important and the most used by human beings: indeed, since the beginning of civilization there have been trials and efforts to represent and somehow “store” images, painted on stones, on paper, on whatever allowed it. For long time, the “sensor” for this task has been just the human eye, or at least until the advent of photography.

While the principle of the *camera obscura* was well known since the 16th century, it was only somewhen between 1826 and 1827, that Nicéphore Niépce took the first photograph able to arrive to today (now at the Harry Ransom Center in Austin, Texas: Figure 1.1 shows a manually enhanced version). In Saint-Loup-de-Varennes, France, he used a 20×25 cm oil-treated bitumen coated plate taking an approximately 8-hour long exposure.

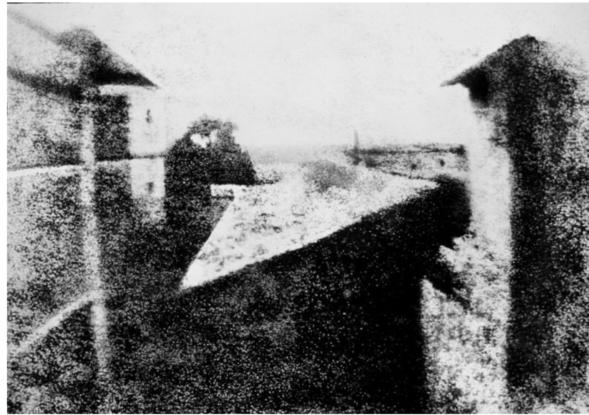


Figure 1.1. First photograph ever taken (circa 1827), named “View from the Window at Le Gras”

Since then, it has been a continuous turbulent imaging revolution, with new features and improvements, and photography experienced a progressively increased popularity, up to nowadays: images dominate our lives. We have not one, but from two to five imaging sensors in our mobile phone and it has been estimated that 1.4 trillions of images will be shot in 2020, with this number growing at an incredible rate in the coming years.

Nevertheless, all these images have one thing in common: they – more or less – precisely reproduce what our eyes see. While these photographs can be beautiful, useful, informative, actually some potentiality is lost. We all know that visible light makes part of the electromagnetic spectrum, and that there is more than that: for example, bees use ultraviolet light to detect spots where to find nectar, or snakes possess some kind of infrared sensors to seek their prey. Our imaging technology evolved too, and today we have image sensors able to detect different ranges of wavelengths. There is one portion of the electromagnetic spectrum, in particular, that is still of difficult approach: the terahertz range. While interesting properties lie in this region, there are additional difficulties in the realization of devices and still

it remains poorly explored in the imaging domain: shooting images is not as easy as for the visible light.

Sensors for visible light are made using low-cost high-production silicon technologies like CMOS (Complementary Metal-Oxide Semiconductor), that makes up the majority of the integrated circuits in our appliances, gadgets, cars and tools. However, other wavelengths are hardly or not accessible with silicon, and the terahertz domain was for long time unreachable. Costly, complex and hard to manage materials are needed, ending up with specialized products that cover only niche markets; moreover, their use is also reserved to specialists, because interpreting a terahertz or infrared image is not the same as looking at a nicely shot photograph. To this end, combining interesting wavelengths with visible light by realizing accessible and low-cost multispectral imaging sensors would open up a wide range of possibilities, spanning from checking the ripeness of fruits the market, verifying skin hydration during outdoor activities under the sun, understanding where to act to improve the thermal insulation of your house, and much more.

The objective of this thesis is to study and develop a fully CMOS multispectral visible and terahertz image sensor, operating in real-time and of compact size. The aim is to contribute to the sensing technology with the perspective of bringing multispectral cameras use to every day’s life, as happened about 200 years ago with the first photograph.

The thesis starts with an overview of sensing and imaging techniques for multispectral imaging in Chapter 2, with some additional emphasis on the terahertz field. Then, it digs into the modeling issues in Chapter 3, by realizing a compact analytical model and validating it with measurements. With these tools, in Chapter 4 the multispectral CMOS THz-VIS camera is designed and fabricated, and first multispectral measurements are taken in Chapter 5. Novel approaches for future directions are then described in Chapter 6, investigating the direct sensing of detected current with a single-electron bipolar avalanche transistor and the use of graphene-based detectors.

Chapter 7 closes the dissertation with conclusions on the conducted activity and an outlook for future works, elaborating on the findings of this thesis.

2 IMAGING IN THE ELECTROMAGNETIC SPECTRUM

The most known way of taking images is in the visible light range, because of our eyes that start grabbing images since the very first days of life; however, it is possible to shoot photographs at almost every wavelength, provided that a proper detector is available. Moreover, not only electromagnetic (EM) radiations can be used, but also other physical quantities like sound (ultrasound imaging) or particles (electron microscopy or positron-emission tomography): nevertheless, in this thesis and specifically in this chapter, the focus will be on the electromagnetic waves.

This chapter introduces the different regions of the EM spectrum and the techniques that can be used to perform detection and where possible imaging. It does not claim to be comprehensive but to give a meaningful overview of the heterogeneous landscape. Afterwards, it gives some further details on the two targeted regions, the terahertz (THz) and the visible (VIS), how multiple spectral regions are typically combined, and eventually it describes the concepts of imaging in the THz domain with CMOS technologies.

2.1 IMAGING AND THE ELECTROMAGNETIC SPECTRUM

One of the fundamental properties needed to perform imaging is the use of a propagating wave: this is what makes electromagnetic waves particularly suitable for it.

2.1.1 Electromagnetic Spectrum Regions

Figure 2.1 shows the electromagnetic spectrum from the microwave region (centimeters wavelength, gigahertz frequency) to the X-ray region (nanometer wavelength, petahertz frequency).

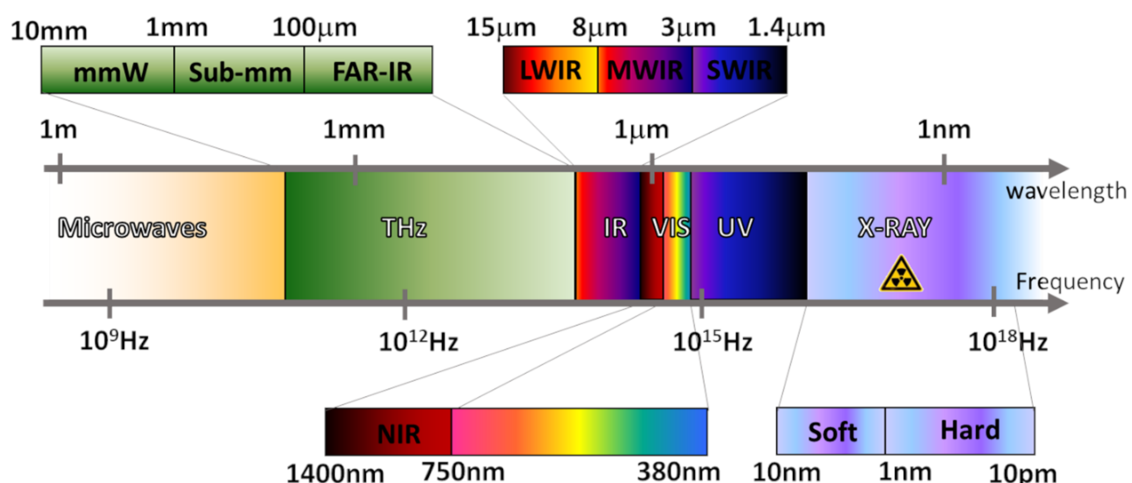


Figure 2.1. Electromagnetic spectrum from microwaves to X-rays

As soon as wavelength becomes smaller and smaller, the preferred representation shifts from the wave description to the particle – i.e., the photon – that better describes interaction with matter. Nevertheless, the duality remains and it is always possible to choose the appropriate description.

Many of these regions are divided into subregions, because of different regulations, properties and behaviors. In particular:

- Microwaves are divided into bands because of their licensing and allocation with government regulations. Bands are named with letters by IEEE standards, for example the L-Band (1-2GHz) is used by GPS (Global Navigation System), or the X-Band (8-12GHz) is used for radars and communications.
- THz waves are divided into mm-waves, sub-mm waves and far infrared (FIR), on one side due to their wavelength, on the other side due to the vicinity of the infrared region.
- Infrared (IR) is divided into long-wave infrared (LWIR, 8-15μm), medium-wave infrared (MWIR, 3-5μm) and short-wave infrared (SWIR, 1-3μm). The LWIR is also called thermal infrared because the peak of black body radiation spectrum at room temperature falls within that region.
- Visible light is commonly known by colours, that are the same we perceive, while there is a specific part towards the IR where our eye stops to work that is named near infrared (NIR).
- Ultraviolet (UV) is divided into UVA (400–315 nm), UVB (315–280 nm), and UVC (280–100 nm), basically grouped by its type of interaction with biological materials. At UVC wavelengths the radiation starts to be ionizing, i.e. energetic enough to free electrons from atoms or molecules.
- X-rays are divided into soft X-rays and hard X-rays, whereas the latter show strong capability of penetrating materials and have a wavelength that is in the order of atoms diameter. For X-rays, more than wavelength or frequency, the energy of the photon is used to identify them.

Although very known relations, it is worth recalling the link between frequency, wavelength, wavenumber, and energy. In particular, wavelength and wavenumber are related to the propagation of the wave and they are linked to the speed of light in the medium:

$$\lambda = \frac{\lambda_0}{n(\lambda_0)} = \frac{c}{n(\lambda_0)f} \tag{2.1}$$

$$k = \frac{2\pi n(\lambda_0)}{\lambda_0} = \frac{2\pi n(\lambda_0)f}{c} \tag{2.2}$$

Where c is the speed of light in vacuum, λ_0 is the wavelength in vacuum and $n(\lambda_0)$ is the refractive index of the material at that wavelength.

Frequency and energy are instead properties that do not depend on the material, and in particular the energy relates to the photon energy, therefore to the particle representation of the EM wave:

$$E = hf = h\nu \tag{2.3}$$

Where h is the Planck's constant of $6.626 \cdot 10^{-34}$ J·s and ν is how frequency is commonly addressed in optical engineering. Typically, particle energy is expressed in electronVolt that is obtained dividing eq.(2.3) by $1.6 \cdot 10^{-19}$ J.

Let's make some example, that relates to the use of radiation and the related detectors in the following paragraph:

- mm-waves f = 300GHz : λ_0 = 1mm, E = 1.24meV
- thermal infrared f = 30THz : λ_0 = 10μm, E = 124meV
- visible f = 545THz : λ_0 = 550nm, E = 2.25eV
- hard X-ray f = 4835PHz : λ_0 = 62pm, E = 20keV

2.1.2 Imaging and Detectors

In almost all these regions there have been attempts to do imaging or at least sensing, as shown in Figure 2.2, beyond the visible range. Imaging has been performed from the radar (radio detection and ranging) in the microwave region, to the mm-waves scanners that can be found in airports; from the thermal imaging that visualizes temperature, to remote sensing and night vision of the infrared band; from radiography, to nuclear medicine exploiting the penetration properties of hard X-rays and gamma-rays.

Some of these require scanning, some employ arrays of detectors, but it is possible to say that basically the whole EM spectrum from microwaves and above can be used for imaging, with each band providing a particular information about the observed scene or sample. Several kinds of detectors and techniques can be used, but here we are interested on those devices that can be miniaturized and integrated, preferably if using mainstream silicon technologies. Figure 2.3 gives an overview of some of the interesting detectors for the different regions.

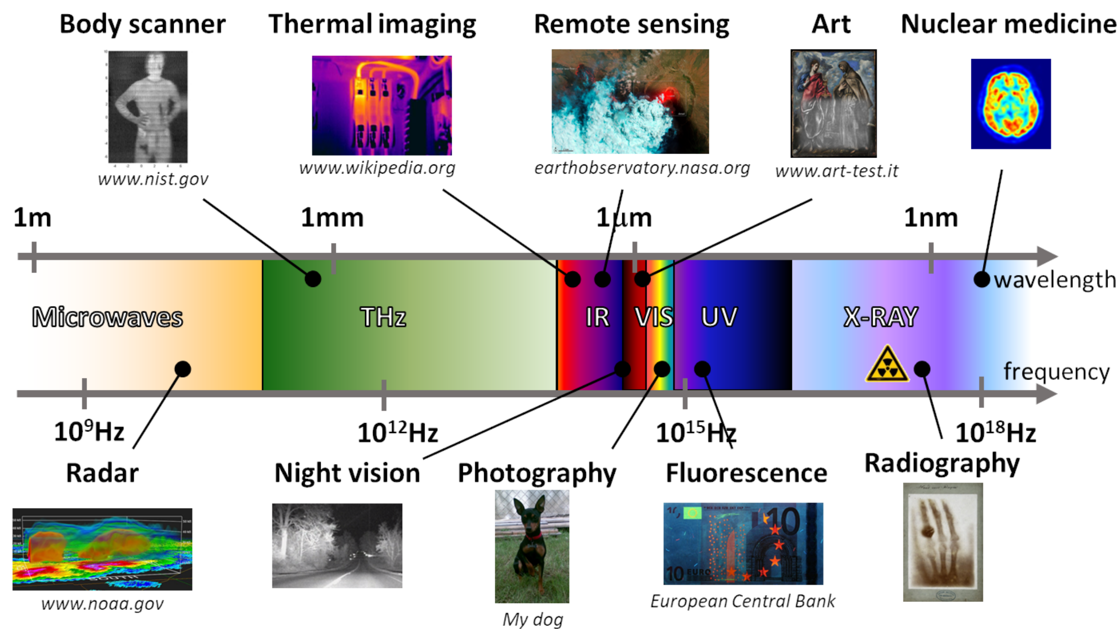


Figure 2.2. Imaging applications in the whole electromagnetic spectrum

The microwave region has been for a long time prerogative of high-speed semiconductors, using HEMT (high-electron mobility transistors) in III-V materials (InP, GaAs, etc) but in the recent years, CMOS deep submicron technology nodes allowed reaching up to tens or hundreds of GHz operating frequencies, for example enabling low cost radar devices [Wambaq2019]. Similarly, the terahertz region is seeing a flourishing research by making use of CMOS technologies [Hillger2019], that are able to reach THz frequencies thanks to the so-called selfmixing rectification effect. In the far-infrared and infrared range it is necessary to divert to less mainstream technologies, like quantum-well photodetectors or micromachined bolometers, that anyway make use of CMOS readout circuits. The visible range, on the other hand, is dominated by a wide number of variants of image sensors in CMOS technologies [Ohta2020], such that specific CIS process (CMOS image sensor) foundries are devoted just to their fabrication. Towards higher energy photons, again exotic materials with a higher stopping power are employed, but still some application is left for monolithic active pixel sensors (MAPS) realized fully in CMOS technologies for high-energy physics experiments [Snoeys2019].

Among these possibilities with CMOS technologies, the THz range and the visible range have some features that makes them extremely interesting to work together: both can be focused and steered with optical elements (i.e. lenses and mirrors), imaging can be performed with arrays of pixels, the resolution – determined by the wavelength – is acceptable, and it does not use harmful radiation. Moreover, as THz images can be of difficult interpretation, adding the visible image information brings an important feature to an image sensor.

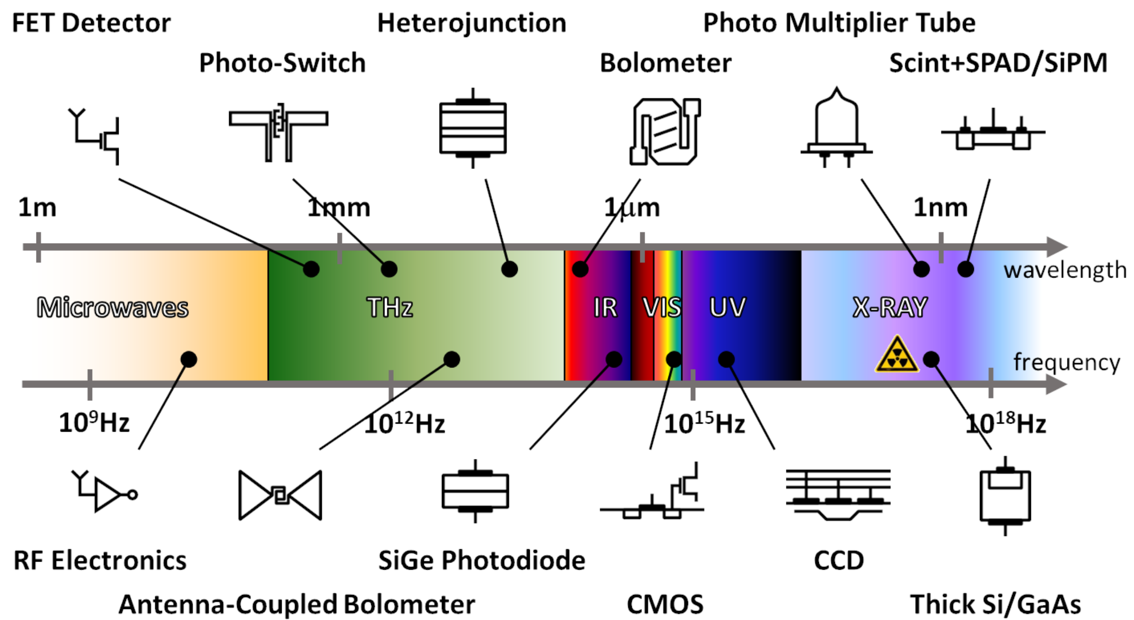


Figure 2.3. The landscape of some of the main detectors in the electromagnetic spectrum

2.2 Visible Image Sensors

CMOS image sensors are based on arrays of photodiodes, realized in the chip substrate, and very simple (from the principle point of view) circuitry to read them out. One of the most common type of pixel is the famous Active Pixel Sensor (APS), that overcame the limitations of previous architectures and set the basis for the scaling of pixel size [Fossum1997].

The basic pixel structures are shown in Figure 2.4, where APS made with 3 and 4 transistors are shown (commonly called 3T and 4T APS). Pixels include a photodiode, typically realized with a n-doped region over a p-substrate, that is the element sensitive to light: photogenerated charges produce a current I_{ph}.

The 3T APS operates by resetting the photodiode bringing its cathode to $VDD\text{-}V_{th}$ (due to the use of an NMOS for M_r), and then releasing the reset, thus starting the integration time. During the integration, the photogenerated charges cause the voltage on the cathode to decrease linearly with the light intensity, discharging to the parasitic capacitance of the photodiode.

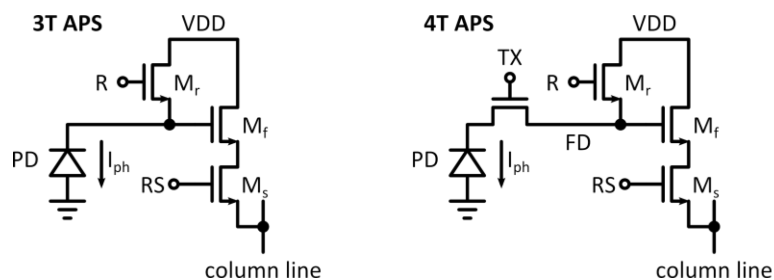


Figure 2.4. APS schematic: 3-transistor pixel (left) and 4-transistor pixel (right)

At the end of the integration time, the final voltage can be read out by the follower M_f and selector M_s to the column line, that is typically biased with a sinking current.

The 4T APS differs by the use of a transfer gate driven by TX, that despite the symbol is not a transistor but a device designed to perform efficient charge transfer from the photodiode to the floating diffusion FD, where the charge is converted into a voltage. This enables low-noise, high-gain image sensor with superior quality. The most popular pixel to do this operation, which is included in the majority of high-performance image sensors, is based on the pinned-photodiode. Specific CMOS process add-ons are needed for its realization.

When realizing pixel arrays, that nowadays can reach several tens of millions of pixels, it is necessary to rely on a scalable and addressable architecture. Figure 2.5 depicts the typical architecture of an image sensor, that implements the addressing by means of a row and a column decoder. In particular, the row decoder selects a specific row, with the possibility to deliver the reset/tx and row select RS signals: the latter, in particular, when activated it connects all the pixels in the addressed row to common column lines. These vertical lines are typically biased with a current, thus completing the source follower realized by M_f. The pixel voltage, buffered on the column lines is then amplified and/or converted to digital, and eventually serialized on a single or multiple output lines for readout. There exist many variants to this architecture in order to improve performance or add features, such as the implementation of 2x2 shared source followers, addressing of region of interest, smart functionality in the pixel, etc. Recently, 3D stacking technologies are becoming standard, with one silicon chip realizing the photodiode and pixel array, and a stacked chip implementing analog to digital conversion and processing: the most advanced processes include a third tier for memory [Tsugawa2017].

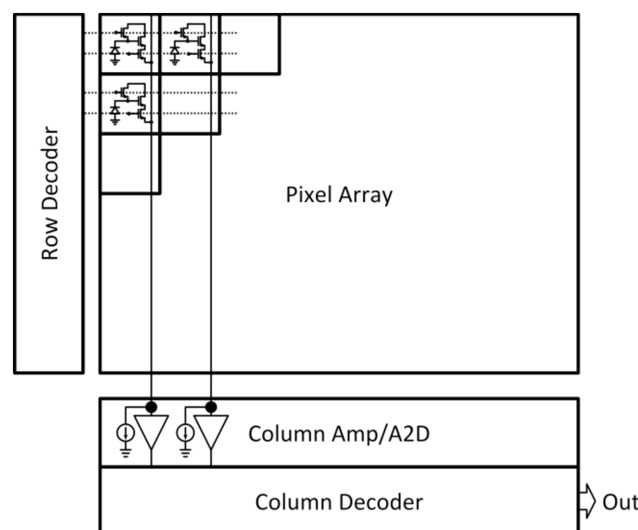


Figure 2.5. Typical architecture of an image sensor

2.3 Terahertz Imaging

Imaging with THz radiation is much more challenging than visible imaging: nevertheless, since the first known far-infrared imaging experiment in 1976 [Hartwick1976], there has been a broad and intense effort in research, with a large variety of methods and techniques [Mittleman2018], and the development of sources, detectors, and components for its manipulation [Perenzoni2013].

First of all, natural sources of THz radiation (i.e. blackbody radiation from objects at room temperature or reflected/diffused radiation from the sun) are extremely weak. This makes necessary a first important distinction, between *passive imaging*, making use of the natural blackbody radiation to produce an image, and *active imaging*, with the help of artificial sources of THz waves. The difference is substantial, as for passive imaging very sensitive detectors are needed (able to detect changes in emitted power much lower than 1 picoWatt). This in turn brings to another distinction, between *cooled detectors* and *uncooled detectors*: indeed, noise generated by thermal sources is often dominant, especially when sensing passively emitted radiation by a body. Cooled detectors (down to cryogenic temperatures) like transition-edge microbolometers or superconducting kinetic inductive detectors can achieve noise performance good enough to perform passive sensing. However, the following review of imaging detectors will be limited to *active imaging devices operating at room temperature*, in order to accomplish the vision described in the introduction of an accessible, real-time, compact multispectral THz and visible camera.

The main techniques that, to date, resulted able to reliably produce real-time room-temperature THz images are limited to a bunch of approaches:

THz time-domain spectroscopy (THz-TDS). This technique employs electrooptical sampling through very short laser pulses: the laser is split in two beams and focused on two optically gated devices, a transmitter and a receiver, realized for example with narrowly spaced antenna electrodes on a high-mobility semiconductor. The transmitter is biased with a DC voltage and the laser-induced charge generation shortly closes a conductive path, obtaining an impulsive current radiating a wide band THz pulse. The receiver works similarly, except that the received THz EM field plays the role of the applied voltage, thus a current is generated and sensed by a current amplifier. The relative delay of the rx-tx laser pulses is adjusted with an optical delay line thus realizing a time-domain fine sampling of the electrical field. This is how the first THz-TDS image in [Hu1995] was scanned and acquired: since then, there has been a continuous improvement of the THz-TDS systems, that are now commercially sold. Still, their operating principle requires expensive femtosecond lasers and sample scanning.

Antenna-coupled microbolometer arrays. Infrared imaging detectors can be realized with microbolometers, i.e. thermal detectors realized with suspended bridges of materials having a high temperature coefficient of resistance. They are typically realized in imaging arrays with a post-processing step over CMOS wafers and encapsulated in vacuum; they show a very high sensitivity, such that when relatively high-power quantum cascade lasers (QCL) became available in the THz range, it was possible to directly acquire images [Lee2006]. This spun research for tailored pixels, for example by designing special antennae coupled to the membrane, such as in [Oden2013] where a 320x240 pixels array enabled real-time THz imaging. However, the fabrication process remains complex and expensive and it can not be tailored to any wavelength because of mechanical limitation of the microbolometers' bridge.

Pyroelectric cameras. Pyroelectric materials, like for example $LiTaO_3$ or PZT, have the property of possessing an intrinsic polarization, and therefore of reacting to absorbed power with a current flow that balances the charge. As the system relaxes down, the crystal returns in the rest state and therefore it can detect only changes in the incident power, while being extremely broadband. Thanks to these properties, with a proper bandpass filter it is possible to use commercial pyroelectric cameras (e.g. Pyrocam III from Spiricon – Ophir Photonics) to perform THz imaging [Han2009]. However, their slow response and low sensitivity (minimum detectable power of hundreds of nW) prevented the technology to become largely employed in THz imaging, while their main use is in the characterization of laser beams.

CMOS self-mixing imaging detectors. As explained in detail in the following (paragraph 2.5), field-effect transistors (FET) can be exploited as power detectors well beyond their cut-off frequency thanks to a distributed self-mixing phenomenon. The big advantage of this technology is its cheap realization and integration with circuits, and therefore a large number of attempts has been made to realize THz imagers: the first remarkable THz imager able to operate at video rate has been presented in [Hadi2012], a 32x32 pixels focal plane working in real time. To date, still resolution remains limited to few pixels due to the size of antennas that overall determine a large chip area.

Overall, the best candidate for low-cost real-time THz imaging seems to be the one based on CMOS FET detection: the potential of the technology is huge, as CMOS-based technologies often demonstrated, in the long run, to be winning over other alternatives. Furthermore, the possibility to integrate processing electronics and to rely on continuous technology advancements, constitutes a fundamental advantage.

2.4 MULTISPECTRAL IMAGE SENSORS

As shown in Figure 2.2, imaging can be done almost throughout the whole EM spectrum: it is therefore natural to consider the chance to widen the possible sensed wavelengths in order to get more information on the captured scene. There may be many ways of realizing multispectral imaging: some of these are depicted in Figure 2.6. When the detector is broadband across the wavelengths of interest, it is possible to act on *filtering* the required bands, or on actively *illuminating* the target with monochromatic sources. It is also possible to exploit *dispersive* elements, that separate the spectral components in space, thus allowing also different detection principles to be combined, or to realize a real *multispectral detection* at the pixel level, in the focal plane.

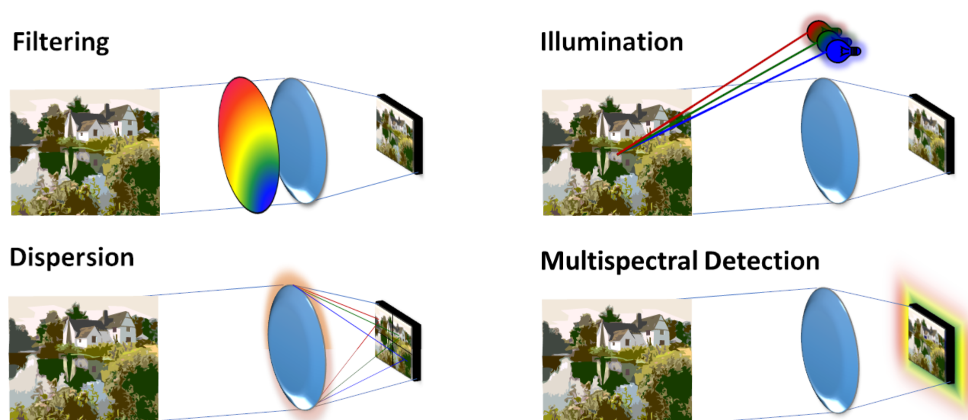


Figure 2.6. Possible schemes of a multispectral camera system

The most common *multispectral imaging* is the one performed by color cameras, that typically use red-green-blue (RGB) color filters, the famous Bayer pattern [Bayer1976], to separate the three base colors. Additional filters or different active illumination can be used with a relatively broadband sensor in order to realize acquisitions in different spectral bands. However, all is done with a single sensor.

Similarly, the term *hyperspectral imaging* typically refers to the capability of capturing images with narrow wavelength bands and with a very fine resolution [Lambrechts2014], for example in the visible range, therefore again using a single detection mechanism.

Going beyond a single detection mechanism, other problems arise, for example the optics, that has to be capable of focusing very different wavelengths. Because of this, typically multispectral sensors and cameras include nearby wavelengths, like visible plus near infrared or ultra-violet. Moreover, as for example in multispectral sensors for satellites, different sensors are assembled in a pushbroom configuration (scanning in the movement direction) or as separate cameras [Jenal2019]. Recent development in organic and quantum-dot films

enabled enhancing the capabilities of CMOS with a dedicated postprocessing [Georgitzikis2019], however only for wavelengths close to the visible spectrum.

In the terahertz region, the spectral resolved imaging is intrinsically implemented in scanning THz-TDS, where both the source and the detector are very wideband, and the spectra is recovered by the Fourier transform of the time-domain waveform. Multiple CMOS FET detectors spanning several frequencies and realized on the same chip, can realize multispectral imaging by using tunable narrowband electronic sources [Bauer2014]: the drawback is its non-scalability to imaging arrays and the need of switching between detectors. A remarkably large bandwidth, from 160GHz to 1THz, can be achieved with high-speed SiGe BiCMOS harmonic mixer sources and heterodyne detectors [Statnikov2015], however again with single pixel, requiring x-y scanning and frequency sweeping. Other approaches have been used, for example the use of "reconfigurable metasurfaces", or in other words wideband antennae probed in several specific spots showing different spectral resonance [Wu2018] giving rise to a weak modulation of the frequency response with some spectral resolution.

Concerning the combination of visible and terahertz regions in a single imaging system, a considerably smaller number of works can be found in literature. The use of separate sensors, with the use of system-level optics and sensor fusion techniques have been used in [Kowalski2014] for a multispectral terahertz, infrared and visible imaging system: while the good performance of single cameras can be exploited, the overall camera is bulky and expensive. A complete integration in a monolithic image sensor for a terahertz, infrared and visible image sensor has been realized exploiting photodiodes in the CMOS substrate, and bolometers for terahertz and infrared, respectively coupled to antenna and made with an absorber [Perenzoni2012]. The scalability is demonstrated by the 160x160 pixel resolution obtained, although the imager is divided into THz-VIS and IR-VIS separate regions. Another monolithic solution using vertically integrated detectors and layers of metamaterials for filtering and capturing terahertz and visible radiation has been implemented in [Carranza2017]. The pixels have been realized with CMOS-compatible processing, but still requiring customized materials (e.g. vanadium oxide for bolometers) and patterning, complicating the scalability and integration perspective.

2.4.1 Applications of terahertz and visible imaging

The potential applications of terahertz imaging are thoroughly listed in literature ([Perenzoni2013], [Mittleman2018], [Hillger2019]) and span several fields, owing to the properties of THz wavelengths:

- Safety and security. Inspection of post mail, luggage, detection of hidden threats exploiting the relative transparency of paper and cloths. Detection of chemical

substances/drugs/explosives by relying on spectral fingerprints of molecules in the THz range;

- Production technology. Online inspection of defects, non-destructive testing, quality control, detection of voids/cracks in composite materials, packaging checks thanks to the terahertz penetration capabilities. Monitoring of layers (paint) thanks to the similar wavelength dimensions;
- Biomedical. Detection of the hydration of tissues/vegetables, monitoring of skin cancer, analysis of the protein dynamics, thanks to the characteristic fingerprints and absorption lines in the terahertz region;
- Cultural heritage. Analysis of paintings, findings such as amphorae, manuscripts and artifacts, exploiting the THz penetration together with the depth resolution given by the time-domain techniques and/or the wavelength dimensions.

All these applications, however, suffer from the difficult interpretation of the acquired terahertz images. For example, this complicates identification of the correct position of the acquired image, and prevents cross-checking by means of additional information. Multispectral imaging adding a one-to-one visible image superimposed with the terahertz image can bring relevant improvements in all the above-mentioned fields.

2.5 CMOS FET Terahertz Detectors

THz detectors implemented with CMOS FETs deserve a separate mention and introduction. The 1996 seminal paper [Dyakonov1996] showed that FET devices could detect and downconvert to DC also frequencies well above the cut-off limit of the transistor. This was explained by the fact that the RF wave couples, via the gate-source port, to the electrons in the channels; their density oscillates in time and propagates in space (plasma waves), and depending on the mobility of the carriers, a resonant (narrowband) or non-resonant (broadband) condition could occur, ending up in a DC detected signal at the drain with intensity proportional to the power of the incoming RF wave. Resonant operation requires high mobility devices – such as HEMTs – and typically also low temperatures, while in every kind of transistor the non-resonant operation is possible. In other words, *any CMOS transistor can operate as a power detector for terahertz radiation*.

This result initiated a wide and diverse investigation in the scientific community, first pioneered by the group lead by Wojciech Knap, CNRS, France verifying on discrete silicon FET components the validity of the assumptions and models [Knap2002][Knap2004]. These studies were immediately followed by several successful attempts using CMOS single detectors by the same group in France, but also in Germany at Goethe University Frankfurt, prof. Hartmut Roskos, and at University of Wuppertal, prof. Ulrich Pfeiffer [Ojefors2009]

[Schuster2011][Boppel2012]. These confirmations of the validity of the approach allowed a number of scientific studies perfecting the understanding of the phenomena.

2.5.1 Principle of THz FET Detection

Although there are several ways and methods to explain the detection mechanism, the one allowing also an intuitive explanation is called *self-mixing*. When a RF signal is applied at the gate-source port of a "cold" (zero drain current) FET biased at a certain V_{GS}, it causes a modulation of the channel conductance g_{DS}. If the RF signal is also coupled to the drain, let's say with a gate-drain capacitance to avoid bias currents flowing into the channel, the resulting current i_{DS} is also modulated, therefore producing a harmonic of twice the frequency, and a DC component that is proportional to the squared amplitude of the RF voltage, or also proportional to the incoming RF power.

In symbolic terms, the applied RF voltage to the FET gate-source port of amplitude V_{RFfet} and frequency f, and the coupling to the drain can be expressed as:

$$\begin{aligned} V_{gs}(t) &= V_G + v_{gs}(t) = V_G + V_{RFfet} sin(2\pi f t) \\ V_{ds}(t) &\approx v_{gs}(t) = V_{RFfet} sin(2\pi f t) \end{aligned} \tag{2.4}$$

The level-1 MOSFET model in strong inversion but linear region (i.e. $V_G > V_{th}$ and small V_{DS}) gives the following expression for the drain-source conductance, that can be expressed in terms of the applied RF signal:

$$\begin{aligned} g_{ds}(t) &= \frac{k_n}{2}\frac{W}{L}\left[2\left(V_{gs}(t) - V_{th}\right) - V_{ds}(t)\right] \\ &= \frac{k_n}{2}\frac{W}{L}\left[2(V_G - V_{th}) + V_{RFfet} sin(2\pi f t)\right] \end{aligned} \tag{2.5}$$

The conductance g_{ds} is therefore the sum of a DC value fixed by V_G-V_{th} with a superimposed small-signal variation modulated by the RF signal. Reusing the eq.(2.4) hypothesis it is possible to calculate the small-signal current flowing into the channel:

$$I_{ds}(t) = V_{ds}(t) g_{ds}(t) = \frac{k_n}{2}\frac{W}{L}\left[2V_{RFfet} sin(2\pi f t)(V_G - V_{th}) + \boldsymbol{V_{RFfet}^2 sin^2(2\pi f t)}\right] \tag{2.6}$$

The part highlighted in bold is the important one, arising from the device non-linearity that is responsible for the detection mechanism. It is worth recalling that $sin^2(x)=[1-cos(2x)]/2$, and therefore from eq.(2.6) it is possible to see that the current I_{ds} has several components: two variable contributions, at frequency f and 2f that are of no interest, plus a DC component. This constant contribution leads directly to the detected current:

$$I_{DS} = k_n \frac{W}{L}\frac{V_{RFfet}^2}{4} \tag{2.7}$$

This extremely simple result, although approximated for strong inversion conditions, proves the capability of the FET device to work as a detector for THz radiation. More detailed models exist, that make use of distributed representation of the FET [Lisauskas2009]. These works anyway yield results in line with eq.(2.7), while giving a better explanation and representation of the plasma-wave propagation in the channel, and of the requirements in terms of gate length and the drain coupling effect.

2.5.2 THz FET Detector Structures

In literature, CMOS FET detectors are mainly found in three configurations, which can be named *gate-driven* [Schuster2011] (the one considered in the analysis above), *source-driven* [Lisauskas2009], and *drain-driven* [Boppel2012]. The schematic connection with respect to the antenna and therefore the incoming radiation is shown on Figure 2.7, where V_G and V_S are always connected respectively to the bias voltage and the DC ground, while V_D provides the output signal. Overall, the simple modeling described before and therefore the response of eq.(2.7) still holds for all configurations:

- The gate-driven configuration is characterized by the use of a single FET, where the THz signal is applied between its gate and source, and the rectified signal appears typically as a small negative DC voltage or sinking DC current at the drain terminal.
- The source-driven configuration makes use of two transistors and the design of the drain and gate terminals as an AC ground allows to exploit a symmetrical structure, again delivering the DC signal at the drain.
- The drain-driven configuration extracts the rectified signal from the antenna terminals, by forcing the middle point of FETs instead of the antenna ones. Indeed, in the drain-driven configuration the expected DC signal is positive.

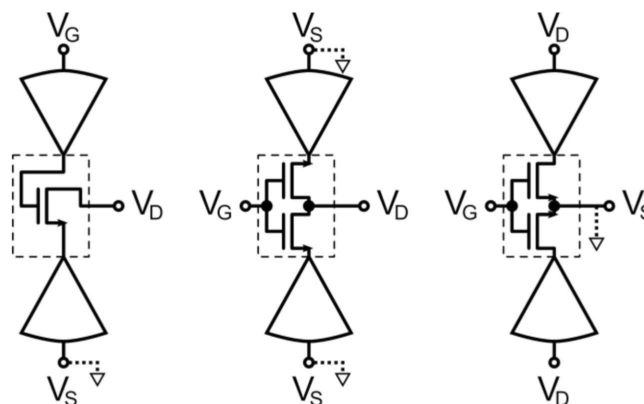


Figure 2.7. FET detectors configurations with respect to the antenna connection and signal extraction, from left to right: gate-driven, source-driven, drain-driven.

Strictly speaking, source-driven and drain-driven structures are topologically equivalent, there is just a change in the DC reference terminal. It is worth noting that for their topology, source-

driven and drain-driven configurations are well suited for differentially driven antennae (like loop or patch), whereas the gate-driven structure needs antennae allowing to keep gate and source terminals physically disconnected.

2.5.3 Figures of Merit for THz Detectors

In this paragraph, some of the main figures of merit typically used for terahertz detectors are introduced. In particular, the responsivity and the noise-equivalent power NEP.

The responsivity of a detector is defined as the output electrical signal in relation to an impinging EM wave power, and therefore it can be separately defined for voltage and current readout:

$$R_V = \frac{V_{det}}{P_{in}} \quad \left[\frac{V}{W}\right] \qquad\qquad R_I = \frac{I_{det}}{P_{in}} \quad \left[\frac{A}{W}\right] \tag{2.8}$$

where V_{det} and I_{det} are respectively the detector output voltage and current, while P_{in} is the terahertz power impinging onto the detector.

The NEP is instead the input referred noise of the detector and it is therefore expressed in terms of power noise spectral density. Considering a flat output noise spectrum (white noise), the output noise in voltage and current can be simply expressed by the value of the noise spectral density V_n^2 [V^2/Hz] and I_n^2 [A^2/Hz]:

$$NEP_V = \frac{V_n}{R_V} \quad \left[\frac{W}{\sqrt{Hz}}\right] \qquad\qquad NEP_I = \frac{I_n}{R_I} \quad \left[\frac{W}{\sqrt{Hz}}\right] \tag{2.9}$$

In case the hypothesis of the flat spectrum does not hold, or in any general case, the NEP is better expressed as a function of the detector’s output frequency: it is worth noting that this frequency is not the one of the input terahertz signal, but it refers to the variations of the rectified low-frequency output. The NEP can also be expressed in [W_{rms}] if integrated in the band of the detector or detection system (typically referred to as *integrated NEP*).

2.5.4 THz imaging with CMOS FETs

The first CMOS THz real imager based of FET detection was [Hadi2012], where a 32×32-pixel sensor with integrated amplifier has been realized in a 65nm technology. A basic pixel with a filtering capacitor and a half differential pair, completed at the column level upon row selection, was implemented, achieving a value of 12nW of integrated NEP (100pW/√Hz) at the frequency of 856GHz.

[Lisauskas2014] showed a 12×12 array of FET detectors realized in 150nm technology, operating at 590GHz with an integrated NEP of 15.2nW. The implemented pixels are simple detectors scanned, selected electronically and externally amplified.

In [Kim2016] the FET detector was employed in a different way, using a diode-connected FET and therefore requiring a current bias to operate. The 8×8 array in 130nm CMOS technology, operating at 820GHz, requires 1MHz source modulation to overcome the bias-introduced 1/f noise, achieving a mean NEP of 36.2pW/√Hz with simple row amplifiers.

Another approach was followed in [Boukhayma2016], where a 31×31 array operating at 270GHz with a 0.6nW integrated NEP was demonstrated (18.7pW/√Hz) in 130nm CMOS. The pixel integrated an active amplifier and a passive high-Q bandpass filter to remove the noise around the source modulation frequency.

In [Liu2017] a 8x8-pixel array is multiplexed on an integrated chopper-stabilized amplifier and a ΣΔ converter. The sensor, realized in 180nm technology, reaches a NEP of 106pW/√Hz at 860GHz. The pixels are basic, with just the detectors and a selection switch.

Per-pixel analog-to-digital converters have been implemented in [Yokoyama2019], in a 32×32 array. Despite this, the VCO-based ADCs are not integrated in the pixel but in the periphery, connected through a complex and not-scalable routing. Nevertheless, 91pW/√Hz was achieved at 930GHz source frequency.

In [Hassanalieragh2020] a 10×10-pixel array of FET detectors operated with bias current is presented. The particular feature of this work is the integration of a method for the compensation of the non-uniformities by a calibration of the detectors biasing conditions. The array achieves a NEP of 216nW/√Hz at 200GHz.

Overall, it is possible to notice how heterogenous are the solutions proposed in literature, with each of the mentioned ones having some specific feature. Nevertheless, the clear trend is from very simple pixels to focal plane arrays integrating more and more functions, firstly amplification but also pre-processing like non-uniformity calibration, and digitization of the signal for more robust operation.

2.6 Chapter Summary

Among the various portions of the EM spectrum that can be employed to perform imaging, the terahertz and visible regions share a peculiarity: both can be sensed using mainstream, low-cost CMOS technology. This makes a multispectral approach potentially very attractive thanks to the established technology.

While visible imaging is extremely developed, imaging in the terahertz range is much more challenging. A large number of techniques exist, but these can be boiled down to a few approaches if the requirements for multipixel, room-temperature, and real-time imaging are

fixed. Eventually, the CMOS solution results to be the most promising and with more possibilities thanks to the electronics integration.

Specifically, the use of a simple FET as a detector can be the key towards the democratization of terahertz imaging.

3 COMPACT EKV MODEL OF FET THZ DETECTOR

Historically, research on FET THz detectors started using off-the-shelf III-V or silicon discrete transistors. Thus, most of the modeling did not care about typical parameters exposed by process design kits of CMOS foundries, while relying on particular characteristics that could be extracted by measurement. However, measuring and characterizing a FET in CMOS technology is not straightforward.

On the other hand, there exist many models suitable for circuit simulations, relying on numerical methods, that provide reliable results. The drawback of using these models is the computation time (simulating a THz wave on a time-domain simulator requires time and resources) and the impossibility to have a direct feeling of the role of the available design parameters.

In this chapter, an analytical model is developed, with the objective of keeping the equations simple and compact, parametrizing them with the available data from usual process design kits. A subsequent validation of the model is performed on real samples.

3.1 FET THZ DETECTOR MODELS: FEATURES AND LIMITATIONS

As mentioned in paragraph 2.5, the first models developed to describe the FET detection mechanism were based on the hydrodynamic analogy of *electrons plasma waves*, by solving the equations of the carrier density in the channel under specific boundary conditions [Knap2002]. Although correctly describing the device physics, these models have the disadvantage of often requiring a precise knowledge of several parameters of difficult access (such as the momentum relaxation time or the effective mass of electrons in the semiconductor); this is especially true when the devices are fabricated by third party foundries. Moreover, as advanced deep-submicron technologies became of common use in FET-based THz detectors, these models could not take into account all the peculiarities introduced in transistors' structure to make them small, fast and reliable.

Thus, soon a different approach has been followed in literature, that was based on elaborating the existing models of the FET transistors that implicitly contained the needed non-linearities to explain at least part of the detection. This brought first to the simple and intuitive *square-law model*, that was then elaborated it into more accurate variants, for example the *non-quasi static model* [Lisauskas2009][Ojefors2009]: the FET is sectioned into segments, all of them performing the self-mixing operation, allowing to better reconstruct the distributed nature of the detection mechanism. While enabling the use of CMOS foundry parameters, the

disadvantage of these models was their limitation in describing the operation near the subthreshold region, that accidentally is where the performance achieves its optimum.

An approach in between was introduced in [Boppel2012] where a detailed physical model has been proposed, while using as much as possible known parameters, however still needing some tuning. It showed a good accuracy ranging from GHz to THz frequencies, but its formulation is given only for the drain-coupled specific detector configuration, lacks a circuital interpretation, and requires also calibration measurements and parameters estimation by data fitting. In the meantime, it was found out that the Spice BSIM3v3 model of the transistor could be used to simulate the detector response [Gutin2012], at the expense of time-consuming simulations.

As it became clear that it was necessary to describe correctly the detector in the weak inversion operating region, the EKV model [Enz1995] resulted the option of choice for many works. Indeed, the EKV model of FET transistors relies on seamless interpolation of the different operating regions in a single working equation. However, this comes at a cost: indeed, expanding and solving these equations is often difficult if not impossible.

A first approach has been published by the author of this thesis in [Perenzoni2010]: however, the model was not validated with measurements and at the same time there was still a relevant discrepancy around the threshold voltage of the FET, i.e. in the weak inversion region.

In [Földesy2013] the EKV model is used as a starting point to obtain a generalized equation including also the detector bias current. On the other hand, equations remain function of the EKV model forward current; in addition, no detailed electromagnetic coupling model is included, thus requiring calibration by measurement. Another approach has been to evaluate the nonlinearity coefficients giving rise to the rectification, extracting them from the EKV model equations; as realized in [Khan2018], these require second order derivatives that again, due to their complexity are not extracted in a closed form. Recently [Liu2019] developed a Verilog-a compatible model from the EKV equations, still without expanding the forward/reverse current expressions. Overall, while accurately describing the detection phenomena, these models do not provide a compact, closed-form equation: the insight of the detector operation is lost, because of the impossibility to look exactly at how single design parameters are involved in the determination of the crucial quantities, namely the voltage or current responsivity R_V or R_I, and the noise-equivalent power *NEP*.

Additionally, in the determination of R_V or R_I and *NEP*, there are other components of the detector subsystem which have to be considered in a comprehensive way and that are often treated differently in distinct papers: the electromagnetic coupling on one side – from the THz wave – and the electrical coupling on the other side – to the signal readout.

The electromagnetic coupling is of paramount importance for the capture and delivery of the THz signal to the detector; it involves primarily the antenna and the matching conditions. Joint design of antenna and detector have been described in [Grzyb2012] but without including its effects in the overall evaluation of the detector model. In [Domingues2013] the influence of the FET width parameter only has been investigated in a specific case, while [Ali2014] compared the differences between the different detector topologies of source-coupled and gate-coupled radiation.

The electrical coupling, on the other end of the detector, determines how the detector can be properly operated and read-out. In [Stillman2007] the drop of responsivity for lower gate voltage bias has been related to the electrical time constant and the resistive loading of the read-out electronics, occurring when the output FET impedance becomes comparable with the instrumentation. Moreover, often the connection of an integrated amplifier led to worse NEP performance with respect to the expected value, such as in [Ojefors2009]. All these cases could be explained by a correct and unified model, that is properly considering all the electrical effects at the detector output; additionally, it could also be applied to evaluate the real noise performance of the whole measurement system.

The work described in this chapter aims at addressing the listed weaknesses and lacking parts of the existing models, in order to build a complete model working for both operating modes, in current and in voltage, from weak to strong inversion, for the main detector configurations explored in current literature. The starting point for the model is the EKV description of the FET transistor, and the preliminary model developed in [Perenzoni2010]: the main goal is to obtain a handy analytical equation that does not require any numerical tool to be evaluated.

3.2 Detector Analytical Model

The developed analytical model starts from the necessity of modeling correctly the detector when it is biased near the threshold voltage, i.e. in the weak inversion region. This is relevant because exactly in these conditions, FET detectors exhibit the best performance in terms of NEP and therefore it is important to understand which quantities are involved in determining response and noise.

Typical simple FET models use disjoint equations to model subthreshold and strong inversion operation, thus jeopardizing the possibility to use a unified model; however, as briefly introduced, in the EKV model [Enz1995] one single equation connects all FET operating regions. The following calculations implement several approximations which assume that the detected signal is negligible with respect to the other DC quantities: this allows the assignment of the steady state values $V_S \to 0$, and $V_D \to 0$ and to consider infinitesimal variations around

that condition. Moreover, the model is valid for gate lengths long enough to generate the detected voltage, i.e. for a gate length longer than the critical length of the plasma wave damping. However, this is not a real limitation of the model: this length as a function of the detection frequency is known [Lisauskas2009], and it is enough – and desirable – to design an efficient detector above the minimum length, such that it is able to fully develop the detected voltage.

The equivalent electrical circuit containing all the relevant components of the model is shown in Figure 3.1.

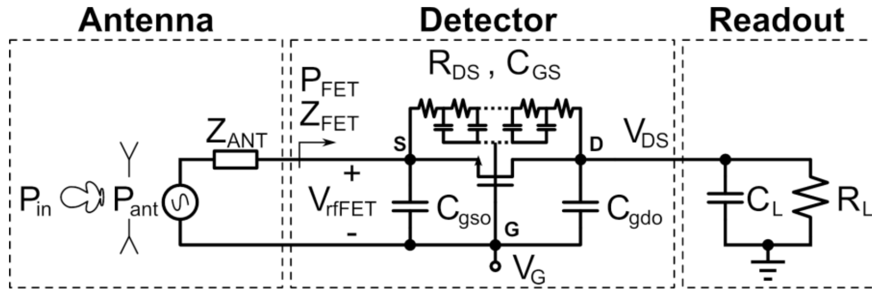


Figure 3.1. Comprehensive equivalent schematic of the detector model for the gate-driven configuration. The antenna with the matching components and the readout are also included.

The antenna part considers that the incident power P_{in} gets converted into a received power P_{ant} depending on efficiency and aperture, and then transferred to the detector depending on the respective impedances Z_{ANT} and Z_{FET}. The detector is a FET with its parasitics, the most relevant being the overlap capacitances between gate and drain/source C_{gdo} and C_{gso}. The channel rectifies the signal through self-mixing thanks to the modulation of the channel resistance R_{DS}, giving rise to a detected voltage V_{DS}. The output signal is read-out by an instrumentation (e.g. lock-in amplifier) having its own input impedance R_L and C_L, acting as a load for the FET detector.

For the sake of simplicity, the schematic represents only the gate-driven configuration, but it is easy to adjust the schematic model to work with the other topologies.

3.2.1 Detector EKV-based modeling

The EKV model considers the FET a completely symmetrical device, having the current between drain and source described by the superposition of two currents flowing in opposite directions, namely the *normalized forward and reverse currents* i_f *and* i_r:

$$I_{ds} = 2k_n V_T^2 \eta \frac{W}{L} \left(i_f - i_r\right) \tag{3.1}$$

Here, k_n is the FET conductivity constant, V_T is the thermal voltage, η is the ideality factor and W, L are the physical size of the transistor. The normalized currents i_f and i_r are expressed with an interpolation function that make them valid in all the FET operating regions:

$$i_{f/r} = \left[ln\left(1 + e^{\frac{V_g - V_{th} - \eta V_{s/d}}{2\eta V_T}}\right)\right]^2 \qquad (3.2)$$

In this equation V_g is the gate voltage, V_{th} is the transistor threshold voltage, while $V_{s/d}$ are the source and drain voltages. The method to extract a closed form of the detection model implies expressing the current as a function of the drain-source voltage itself with the hypothesis that the THz radiation leaks towards the drain, giving rise to the self-mixing effect. This implies setting, on the left-hand side of eq.(3.1), $I_{ds} = f(V_{DS})$, thus yielding an equation of the type $f(x)=ln^2(1+e^{g(x)})$ to be solved for x. As this is not feasible analytically, one possible approach is to find an approximation of the terms *inside the square brackets* of eq.(3.2), thus keeping the square that gives rise to the nonlinear terms necessary for the detection mechanism.

It is sufficient to use the first-order Taylor expansion to obtain an approximate expression of I_{ds}, with the hypothesis of small variations on top of a constant V_{GS}, and constant V_D and V_S:

$$I_{ds} \approx 2k_n V_T^2 \eta \frac{W}{L}\left[\left(\frac{d\sqrt{i_f}}{dV_{gs}}V_{gs}\right)^2 - \left(\frac{d\sqrt{i_r}}{dV_{gs}}V_{gs}\right)^2\right] \qquad (3.3)$$

With this result, it is possible to introduce a gate-source sinusoidal perturbation $V_{rfFET} \cdot sin(\omega t)$ (i.e. the incident radiation) and the small-signal boundary conditions $v_s = 0$ and $v_d = v_g$: in other words, this describes the high frequency coupling between the RF signal at the gate and the drain, thanks to the capacitive nature of the gate-drain parasitics. The result is that in eq.(3.3) it is possible to substitute are easy-to-expand second order terms that eventually bring to the detected DC component I_{DS} described by

$$I_{DS-approx} = k_n \frac{(2-\eta)}{8}\frac{W}{L}\frac{e^{\frac{V_G - V_{th}}{2\eta V_T}}}{cosh^2\left(\frac{V_G - V_{th}}{4\eta V_T}\right)} {V_{rfFET}}^2 \qquad (3.4)$$

This model, although incomplete because both the electromagnetic coupling from the antenna and the electrical coupling towards the measuring instrumentation are missing, describes in a simple and compact way the role of technological and design parameters in the detection mechanism [Perenzoni2010]. However, if compared to a more accurate numerical simulation of the FET using the original EKV model, it also shows a relevant discrepancy around the $V_G \approx V_{th}$ subthreshold region.

In particular, there is a 1x to 2x factor depending on the detector voltage bias: the motivation of this has to be found in the squared terms of eq.(3.3), that have been individually approximated with a Taylor expansion, thus being both infinitesimally small. The subtraction of two approximated and very small quantities can indeed bring to relevant errors, as it is the case.

Nevertheless, both eqs.(3.3) and (3.4) see the term $\frac{V_G - V_{th}}{2\eta V_T}$ as a common variable function of V_G, while all the other parameters act as multiplicative factor. Therefore, the found discrepancy can be easily represented with a good approximation by a reversed sigmoid shape:

$$\varepsilon_{corr} = 1 + \frac{1}{1 + 0.5e^{\frac{V_G - V_{th}}{2\eta V_T}}} \tag{3.5}$$

This corrective factor ε_{corr} can be multiplied by eq.(3.4) in order to obtain a better representation of the detected current:

$$I_{DS} = k_n \frac{(2-\eta)}{8} \frac{W}{L} \frac{\varepsilon_{corr} e^{\frac{V_G - V_{th}}{2\eta V_T}}}{cosh^2\left(\frac{V_G - V_{th}}{4\eta V_T}\right)} V_{rfFET}{}^2 \tag{3.6}$$

Figure 3.2 depicts, at varying gate voltages, the analytical model of the detected current, its corrected version, and the results of the numerical simulation on the EKV complete equation of a hypothetical transistor having a threshold at 0.5V: the correction recovers a large part of the discrepancy.

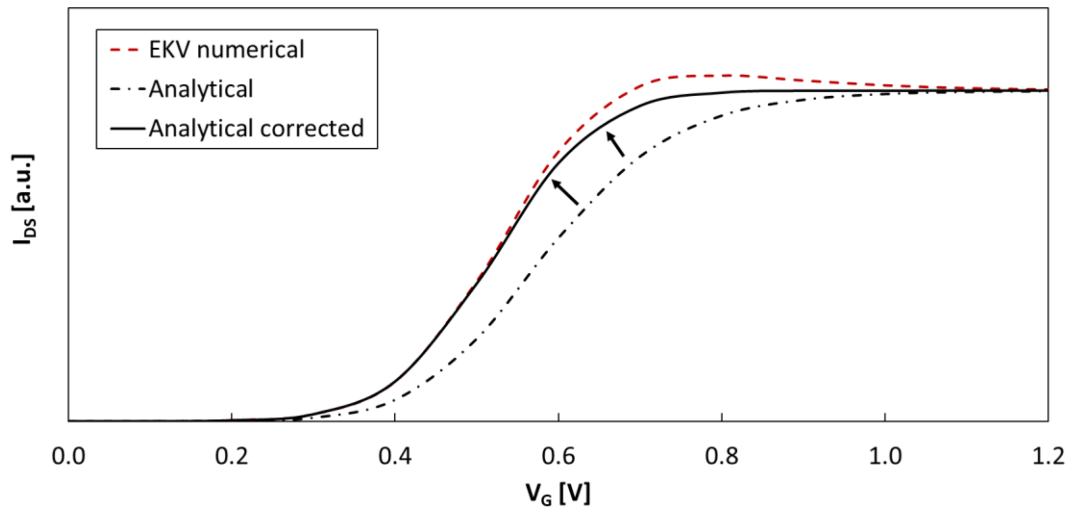


Figure 3.2. Improvement of the approximated analytical model compared to the non-approximated numerical model when considering the correction factor ε_{corr}.

With this improved representation of the current generated by the device in virtue of the detection mechanism, it is possible to extract the detector generated voltage. The conductance in parallel with the current generator is given by the EKV model, with no need of approximation because it contains only the steady-state values of the biasing conditions:

$$G_{DS} = 4k_n V_T \frac{W}{L} \frac{e^{\frac{V_G - V_{th}}{2\eta V_T}}}{1 + e^{\frac{V_G - V_{th}}{2\eta V_T}}} \cdot ln\left(1 + e^{\frac{V_G - V_{th}}{2\eta V_T}}\right) \tag{3.7}$$

The Thevenin equivalent of the current representation is therefore easily extracted by dividing eq. (3.6) by the conductance, which leads to

$$V_{DS} = \frac{1}{16V_T}\frac{2-\eta}{\eta}\frac{\varepsilon_{corr}e^{\frac{V_G-V_{th}}{4\eta V_T}}}{cosh\left(\frac{V_G-V_{th}}{4V_T\eta}\right)ln\left(1+e^{\frac{V_G-V_{th}}{2\eta V_T}}\right)}{V_{rfFET}}^2 \tag{3.8}$$

These equations are extracted with the hypothesis that the RF wave is coupled between the gate and source terminals, and that it propagates with negligible attenuation to the drain terminal. This happens thanks both to the distributed RC line of the channel and also to the gate-drain parasitic overlap capacitance, that acts as a short at very high frequencies. However, the relevant overlap capacitance in CMOS technologies together with R_{DS} forms a high-pass filter which is potentially attenuating the amount of signal reaching the drain for lower frequencies. Calling C_{gdo} the overlap capacitance per FET unit width, an attenuation term based on the high-pass frequency response must be considered:

$$|H_{HP}(\omega)|^2 = \frac{\left(\omega R_{DS}WC_{gdo}\right)^2}{1+\left(\omega R_{DS}WC_{gdo}\right)^2} \tag{3.9}$$

It is interesting to show that this filtering effect depends partly on the FET biasing conditions through R_{DS}. In the case of source-driven structures, both gate and drain terminals are designed such as they are at AC ground: this reflects in having, by design, an equivalently very large capacitance between them. The result is that the term (3.9) in the drain-coupled structures can be neglected and therefore they experience a slightly slower drop in response for higher FET bias voltages, whereas in gate-driven structures the channel resistance decreases and the high-pass pole moves towards higher frequencies.

Another limitation towards high frequencies is represented by the FET parasitics preventing proper coupling of the THz radiation to the channel, in particular the presence of shunting unwanted parallel capacitance as described in [Boppel2012]. While the detection mechanism continues to work with increasing frequencies, a roll-off is expected beyond 1THz due to this effect, that can be introduced in the model by properly calculating the FET impedance, as shown in the next paragraph.

3.2.2 Antenna and Electromagnetic Coupling Model

The phenomena of radiating and receiving antennae is a very broad and complex topic: however, it is possible to divide the problem in some smaller steps, although a detailed general modeling of the antenna is not feasible and requires proper numerical simulations.

Typically, when considering a receiving (or radiating, that is equivalent for the reciprocity theorem) antenna, it is necessary to consider the directivity properties of the antenna itself:

indeed, considering a radiating antenna, P_{ant} would be the integral of the power radiated in all direction. Radiation with normal incidence is used while characterizing detectors, even if, depending on the focusing system, actual applications may deliver a given field-of-view to the detector. If a plane wave with normal incidence hits the detector, the directivity must be used to define the effective detector area in order to calculate a correct value of received power with respect to the incident one. The effective detector area is also fundamental for the characterization, because it allows to quantify the power distribution at the detector plane. In order to give a general-purpose model, here it has been decided to define the area of the detector as the physical aperture, if applicable (e.g. aperture antennas, or pixels in imaging detectors), otherwise as the maximum effective area of the antenna in the frequency range of interest.

Usually directivity is a function of the frequency and can determine in a relevant way the envelope of the response, by means of the so-called aperture efficiency: the ratio between the physical aperture (size) of the detector and the effective area. Therefore, the power captured by the antenna P_{ant} can be expressed as follows:

$$P_{ant} = \frac{A_{eff}}{A_{det}} P_{in} = \frac{\lambda^2 D(\lambda)}{4\pi A_{det}} P_{in} \quad (3.10)$$

where A_{det} is the detector area defined as the physical aperture, pixel size, or maximum effective area, P_{in} is the incident power on the detector area, λ is the wavelength and $D(\lambda)$ is the directivity. By definition, the ratio A_{eff}/A_{det} is the antenna aperture efficiency.

The captured power is then transferred to the load, i.e. the detector, with some losses and a given impedance match/mismatch. Each antenna is indeed characterized by a frequency dependent impedance value Z_{ANT}, which determines the amount of power that can be delivered to the load based on the matching conditions. The load is here represented by the FET impedance Z_{FET} seen from the gate-source port and it is function of the technology parameters, of the geometry of the device, and of the specific connections and passives (e.g. impedance matching elements).

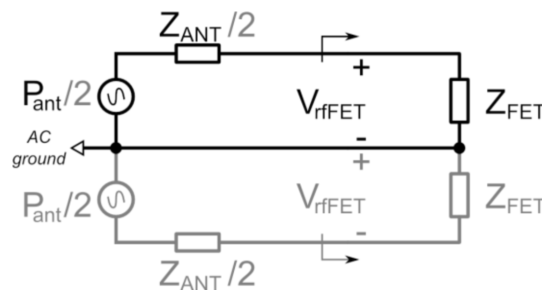


Figure 3.3. Equivalent circuit of the antenna and detector. Valid generally for the gate-driven configuration, by adding the shaded part also the source- and drain-driven configurations can be modeled.

By solving the circuit of Figure 3.3, it is possible to extract the voltage at the FET terminals, whereas the source-driven configuration differs only by replacing Z_{ANT} with $Z_{ANT}/2$ and P_{ant} with $P_{ant}/2$. The two differential configurations are equal because the induced voltage on the detection side is supposed to be electrically infinitesimal: the transistors operate in a region where they are substantially symmetric, the only difference being the reference point for the signal readout. The power delivered to the load is converted into a sinusoidal voltage with squared peak amplitude of

$$V_{rfFET}^2 = R_{eq}P_{ant} = \begin{cases} 4\varepsilon\, Re(Z_{ANT}) \left|\dfrac{Z_{FET}}{Z_{FET}+Z_{ANT}}\right|^2 P_{ant} & GD \\ \varepsilon\, Re(Z_{ANT}) \left|\dfrac{2Z_{FET}}{2Z_{FET}+Z_{ANT}}\right|^2 P_{ant} & SD \end{cases} \tag{3.11}$$

where R_{eq} is a constant that dimensionally is a resistance (Ohm). It can be named “equivalent resistance” and it aggregates the parameters that transform the input power into output voltage [Perenzoni2015]. In eq.(3.11), the efficiency term ε accounts for the losses in the antenna.

Due to the fact that at high frequency the geometry and layout of the devices influence dramatically the impedance, the proper way to evaluate Z_{FET} is to employ high-frequency simulators, but a good analytical estimate can be obtained for the sake of completeness of the modeling. As shown in Figure 3.1, the channel acts as a distributed RC transmission line, with the distributed resistance of the channel capacitively coupled to the gate, which in turn is considered to be equipotential in this approximation. Additionally, the plasma wave in non-resonant detection dampens to zero [Knap2004] before the drain terminal (i.e. no standing wave); therefore, the impedance seen by the antenna is the *characteristic impedance* of the channel transmission line. Moreover, other parasitics have to be added: the most relevant is the gate-source overlap capacitance, bringing eventually to the expression

$$Z_{FET} = \sqrt{\frac{R_{DS}}{j\omega WLC_{ox}}} \,||\, \frac{1}{j\omega WC_{gso}} \tag{3.12}$$

where C_{gso} is the gate-source overlap capacitance per unit width, and C_{ox} is the gate oxide capacitance per unit area. However, as already mentioned, this simplified expression is not enough to evaluate the exact impedance seen by the antenna: it is necessary to add a further contribution considering the implemented geometry, which is layout-dependent and cannot be expressed here in a general way. Moreover, this calculation assumes that the connection towards the readout circuit is designed in such a way that the latter does not influence the antenna impedance.

3.2.3 Electrical Loading Model

In order to measure the detected voltage or current, the detector is typically connected to high-impedance circuits for voltage readout, while low-impedance circuits are used for current readout. Due to the finite output resistance of the detector itself, their input resistance R_L and capacitance C_L form a low-pass filter with a DC attenuation given by the ratio of the detector and instrument resistances:

$$|H_{VM}(\omega_{MOD})| = \frac{V_{out}}{V_{DS}} = \frac{R_L}{R_{DS} + R_L} \cdot \frac{1}{\sqrt{1 + (\omega_{MOD} C_L \cdot R_{DS} \| R_L)^2}} \tag{3.13}$$

$$|H_{CM}(\omega_{MOD})| = \frac{I_{out}}{I_{DS}} = \frac{R_{DS}}{R_{DS} + R_L} \cdot \frac{1}{\sqrt{1 + (\omega_{MOD} C_L \cdot R_{DS} \| R_L)^2}} \tag{3.14}$$

While R_L and C_L are typically constant, the value of R_{DS} depends instead on the FET bias conditions and can be modeled using eq.(3.7). When the source- and drain-driven structures are used, the output resistance of the detector must be divided by 2 because, in the equivalent DC circuit, two transistors are in parallel. This can be considered by substituting R_{DS} with $R_{DS}/2$ in eqs.(3.13) and (3.14).

3.2.4 Noise Model

FET devices, in conditions of zero current bias, generate thermal noise in the channel with a power density proportional to its conductance. Even if reading out the detector in current mode, it is possible to assume negligible 1/f noise because of the very low current levels and the hypothesis of a cold detector (i.e. zero bias). The typical sensitivity of FET detectors allows to neglect other noise sources (e.g. blackbody radiation). Therefore, only thermal noise can be included in the model, with its white spectral power density amounting to:

$$v_{nDS}^2 = 4kTR_{DS} \tag{3.15}$$

$$i_{nDS}^2 = \frac{4kT}{R_{DS}} \tag{3.16}$$

However, when considering the whole chain, also the noise spectral density is modified by the electrical coupling calculated in (8) and (9), in terms of both amplitude and bandwidth. It is easy to calculate the output noise spectral density and bandwidth by combining eqs. (3.13), (3.14), (3.15), and (3.16):

$$v_{nOUT}^2 = 4kTR_{DS} \cdot \left(\frac{R_L}{R_{DS} + R_L}\right)^2 \tag{3.17}$$

$$i_{nOUT}^2 = \frac{4kT}{R_{DS}} \cdot \left(\frac{R_{DS}}{R_{DS} + R_L}\right)^2 \tag{3.18}$$

$$f_{BW} = \frac{1}{2\pi(C_L \cdot R_{DS}||R_L)} \tag{3.19}$$

Similarly as before, when the source- and drain-driven structures are considered, the channel resistance generating the noise must be divided by 2. This can be considered by substituting R_{DS} with $R_{DS}/2$ in eqs. (3.17), (3.18), and (3.19).

3.2.5 Overall Detector Model

In the previous paragraphs all the single components of the detector *responsivity* have been extracted; therefore, it is calculated by dividing the output signal (voltage or current) by the input power, eventually obtaining the final eqs. (3.20) and (3.21).

As far as the *NEP* is of concern, it is obtained dividing the output noise spectral density by the responsivity, therefore obtaining the input-referred noise power spectral density. If the responsivity contains the term calculated in eqs. (3.13) or (3.14), then to have a coherent calculation also the noise should include the electrical loading effect: this correctly makes this factor cancel out and disappear in the NEP expression. Therefore, it is quite obvious that the final detector NEP of eq. (3.22) results to be independent from the current or voltage readout mode, as it is determined only by the detector characteristics that do not change with the measurement which is performed.

$$R_I = k_n \frac{(2-\eta)}{8} \frac{W}{L} \frac{\varepsilon_{corr} e^{\frac{V_G - V_{th}}{2\eta V_T}}}{cosh^2\left(\frac{V_G - V_{th}}{4\eta V_T}\right)} \cdot |H_{HP}(\omega)|^2 \cdot \frac{R_{eq}\lambda^2 D(\lambda)}{4\pi A_{det}} \cdot |H_{CM}(\omega_{MOD})| \tag{3.20}$$

$$R_V = \frac{2-\eta}{16 V_T \eta} \frac{\varepsilon_{corr} e^{\frac{V_G - V_{th}}{4\eta V_T}}}{cosh\left(\frac{V_G - V_{th}}{4\eta V_T}\right) ln\left(1 + e^{\frac{V_G - V_{th}}{2\eta V_T}}\right)} \cdot |H_{HP}(\omega)|^2 \cdot \frac{R_{eq}\lambda^2 D(\lambda)}{4\pi A_{det}} \cdot |H_{VM}(\omega_{MOD})| \tag{3.21}$$

$$NEP = \frac{16 \frac{\eta}{2-\eta} cosh^2\left(\frac{V_G - V_{th}}{4\eta V_T}\right)}{|H_{HP}(\omega)|^2 \cdot \varepsilon_{corr} e^{\frac{V_G - V_{th}}{2\eta V_T}} \frac{R_{eq}\lambda^2 D(\lambda)}{4\pi A_{det}}} \sqrt{\frac{8 k_B T_0 V_T}{k_n \frac{W}{L}} \cdot ln\left[1 + e^{\frac{V_G - V_{th}}{4\eta V_T}}\right] \cdot \frac{e^{\frac{V_G - V_{th}}{2\eta V_T}}}{1 + e^{\frac{V_G - V_{th}}{2\eta V_T}}}} \tag{3.22}$$

3.3 Experimental Results and Model Validation

The model should be validated against measurements in order to assess its coherence with the real device. In order to do so, it would be valuable to investigate the variations with respect to some of the design parameters, for example the transistor size.

For this purpose, a previously designed test chip in a 0.18μm CMOS technology was available [Ali2014], containing several detectors with different width and driving scheme. For this design,

also accurate device impedance simulations have been performed in order to properly match the antenna coupling conditions.

3.3.1 Implemented Devices

One single bow-tie antenna was designed to be replicated and connected to all detectors. In order to decrease the losses, all the metal levels are connected together through conductive vias and a surrounding border is grounded in order to decrease cross-talk between neighboring devices. As in all CMOS technologies, the metals are immersed in a silicon oxide layer. The structure lies on the low-resistivity silicon substrate, which will introduce some losses: however, it will also act as a resonant cavity to enhance response in the frequency of interest.

Antenna impedance, efficiency and directivity have been simulated considering the real silicon chip size and the presence of a metal plate on the package. On the four lateral sides, absorbing boundary conditions were set. While the antenna optimization was not one of the requirements for the purpose of this analysis, the center frequency was designed in order to match the range of the available measurement setup at about 320GHz with a directivity of about 9.5dB, mainly contributed by the substrate resonance.

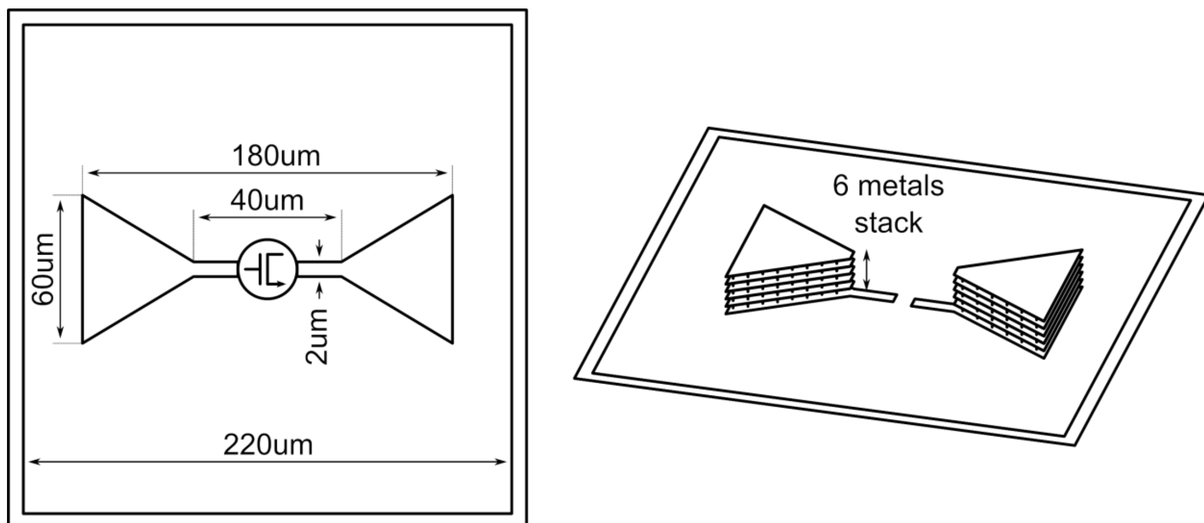


Figure 3.4. Dimensions of the antenna and 3d sketch of its realization in a 6-metal 0.18um CMOS technology

The chip contains 4 detector variants, with a different configuration (gate-driven and source-driven) and size (2μm and 5μm width). Electromagnetic simulations for the extraction of the FET impedance have been performed, in order to include additional parasitic capacitance using the real geometries. The process features needed for the simulations have been extracted from the foundry design kit by relying on geometrical parameters (layers thickness, spacing, sheet resistance, permittivity constant, etc). A sketch of the realized geometries is shown in Figure 3.5.

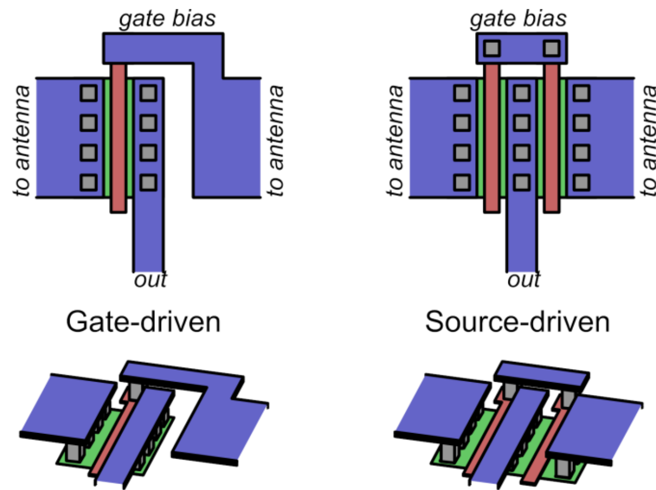


Figure 3.5. Simulated FET structures for the extraction of the additional parasitic capacitances for the gate-driven (left) and source-driven (right) configurations.

3.3.2 FET measurements and comparison

The fabricated devices (Figure 3.6) have been characterized in a THz setup, using a VDI (Virginia Diodes Inc.) source composed by a frequency synthesizer and a frequency multiplier, to cover approximately the range 265-370 GHz with <1mW of power. The source is modulated at 100Hz for removal of correlated noise as shown in the measurement setup Figure 3.7. The multiplier output is coupled to free-space by means of a horn antenna with 25dB gain.

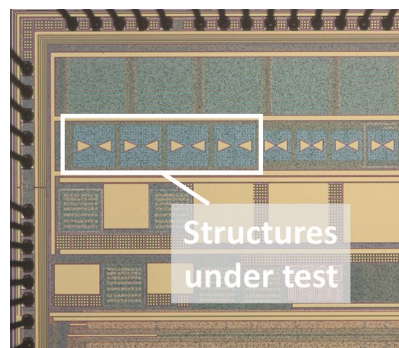


Figure 3.6. Microphotograph of the 0.18μm CMOS technology test chip, with highlighted the structures under investigation.

Several preliminary measurements have been done, like calibrating the impinging power density on the detector plane with a pyroelectric reference detector, and characterizing the antennas directivity in the E- and H-plane for effective area measurements; these are of paramount importance for a correct evaluation of the device performance parameters [Ali2016]. The detector was placed 15cm away from the horn antenna of the source, thus guaranteeing the far-field operation. The acquired spectra were partly affected by multiple reflections which have been smoothed by a 3-pts moving average on the acquired data.

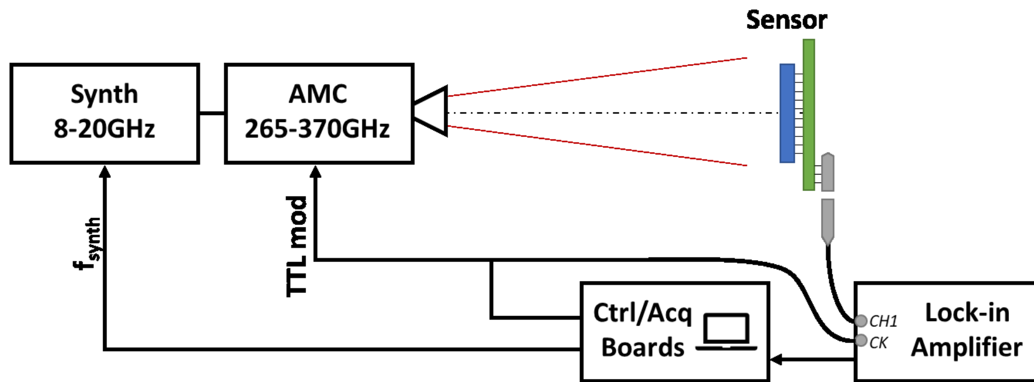


Figure 3.7. Measurement setup for the characterization of the FET detector.

Both source frequency and detector voltage bias have been swept, while acquiring the output voltage with a lock-in amplifier having 10MΩ//30pF input impedance, and eventually responsivity and NEP have been calculated. Their values have also been evaluated with the model, but using only parameters from the foundry, antenna simulation results, and detector parasitic simulations: no fitting from measurement has been used, so as to validate the capability of the model to work as a design tool for predicting performance with commonly available data.

The measurements and the model predicted values for the responsivity over source frequency are plotted in Figure 3.8 and Figure 3.9, while Figure 3.10 to Figure 3.13 show the responsivity and NEP obtained at a fixed frequency of 320GHz and varying gate voltage bias. Overall, the measurements show a good agreement with the modeled performance, correctly reproducing the behavior with respect to the parameters variation, i.e. transistor size, detector scheme, and biasing conditions. Due to the limitation of the measuring equipment, it was not possible to measure the current responsivity: nevertheless, relative correctness of voltage responsivity and channel resistance implicitly means correct current responsivity.

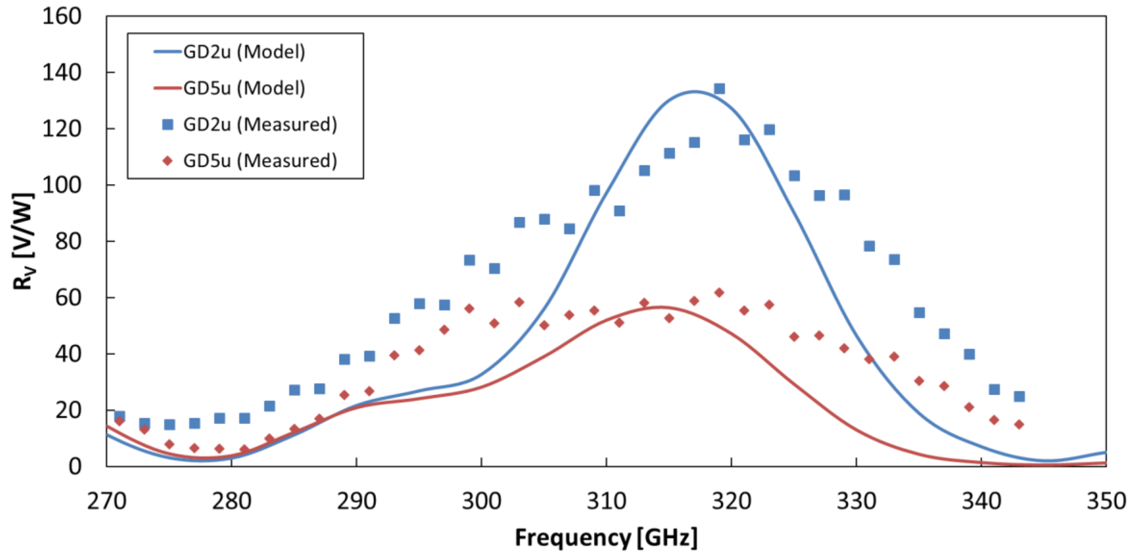


Figure 3.8. Modeled (solid line) and measured (dots) FET detector responsivity R_V over source frequency for the gate-driven structures at V_G=0.35V.

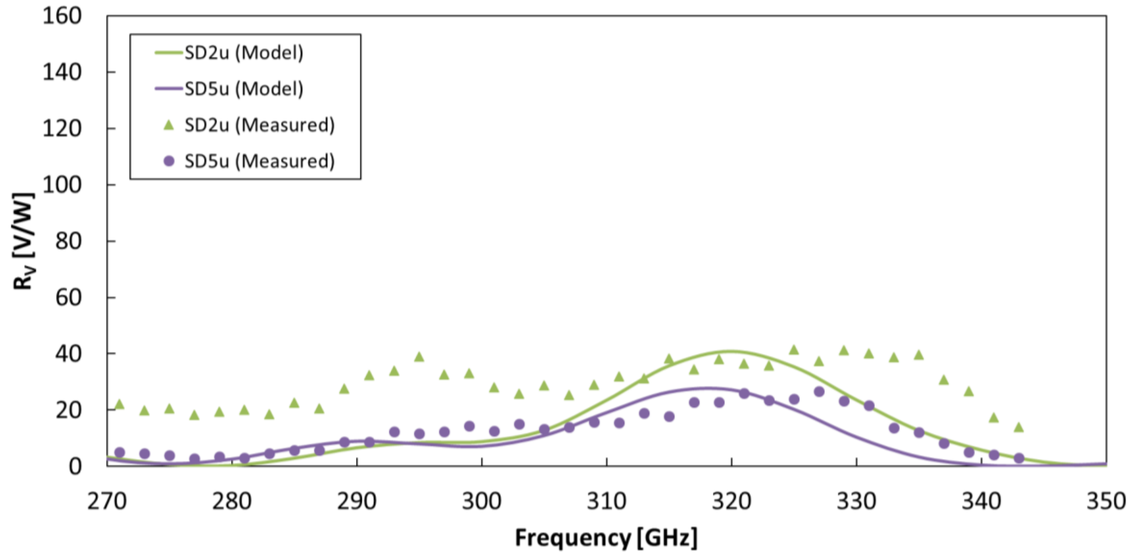


Figure 3.9. Modeled (solid line) and measured (dots) FET detector responsivity R_V over source frequency for the source-driven structures at V_G=0.35V.

The overall good agreement of the responsivity behavior in the frequency response of Figure 3.9 and Figure 3.10 highlights a fairly accurate prediction of the impedance matching conditions, thanks to the finite element simulations of the FET impedance, giving a better modeling with respect to eq. (3.12). A slightly larger bandwidth can be observed and it can be accounted to the complex boundary conditions, not completely included in the antenna model.

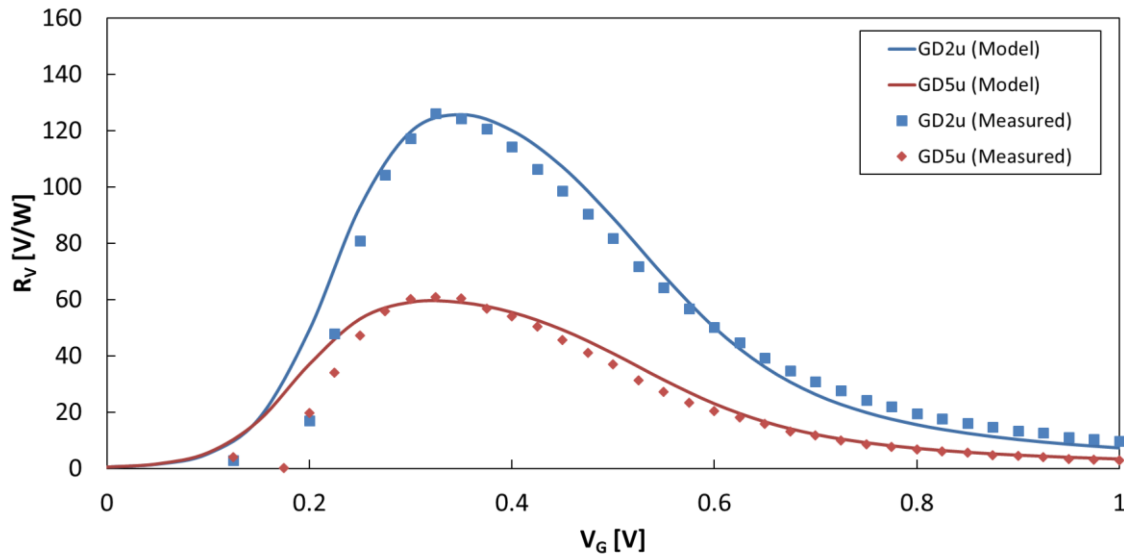


Figure 3.10. Modeled (solid line) and measured (dots) FET detector responsivity R_V over gate bias voltage V_G for the gate-driven structures at 320GHz frequency.

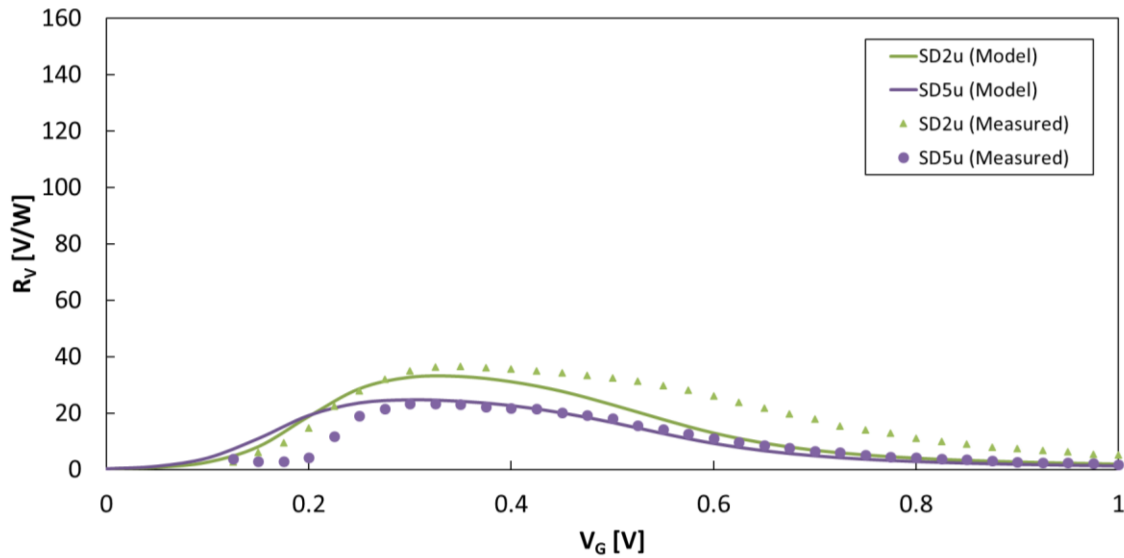


Figure 3.11. Modeled (solid line) and measured (dots) FET detector responsivity R_V over gate bias voltage V_G for the source-driven structures at 320GHz frequency.

A very good matching is achieved in Figure 3.10 and Figure 3.11 for the responsivity bias sweep behavior. The 2μm source-driven structure makes an exception for large bias values, showing an unexpectedly high responsivity that may be due to a slower decrease of the drain-source resistance, i.e. due to mismatches with respect to nominal MOSFET parameters. All structures highlight a steeper drop of responsivity at decreasing gate bias: this is probably due to a discrepancy of the resistance modeling. The effective channel resistance could be higher than expected, and this causes an early effect of the low-pass cut due to the source modulation.

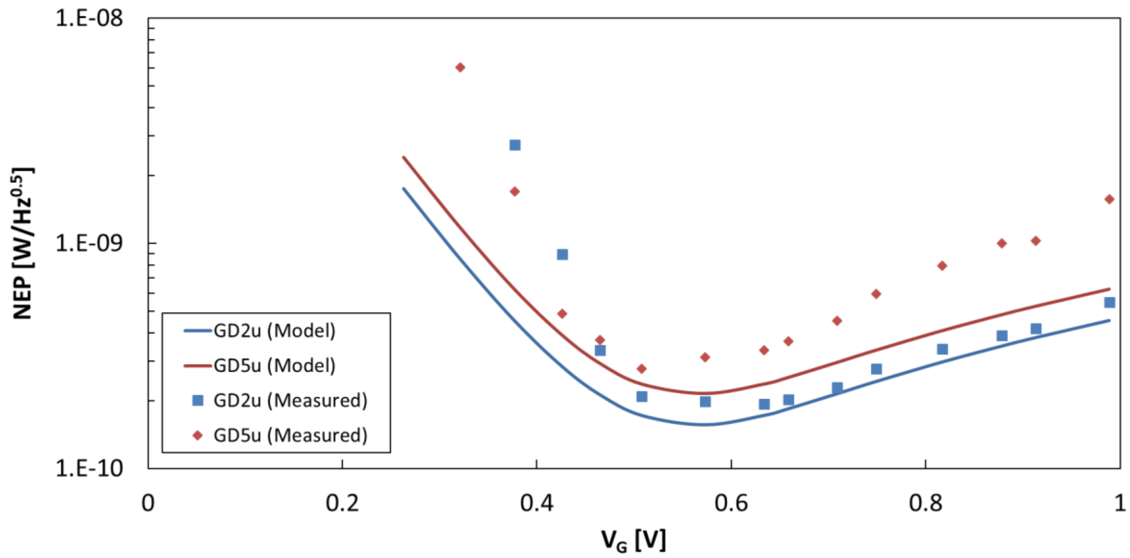


Figure 3.12. Modeled (solid line) and measured (dots) FET detector NEP over gate bias voltage V_G for the gate-driven structures at 320GHz frequency.

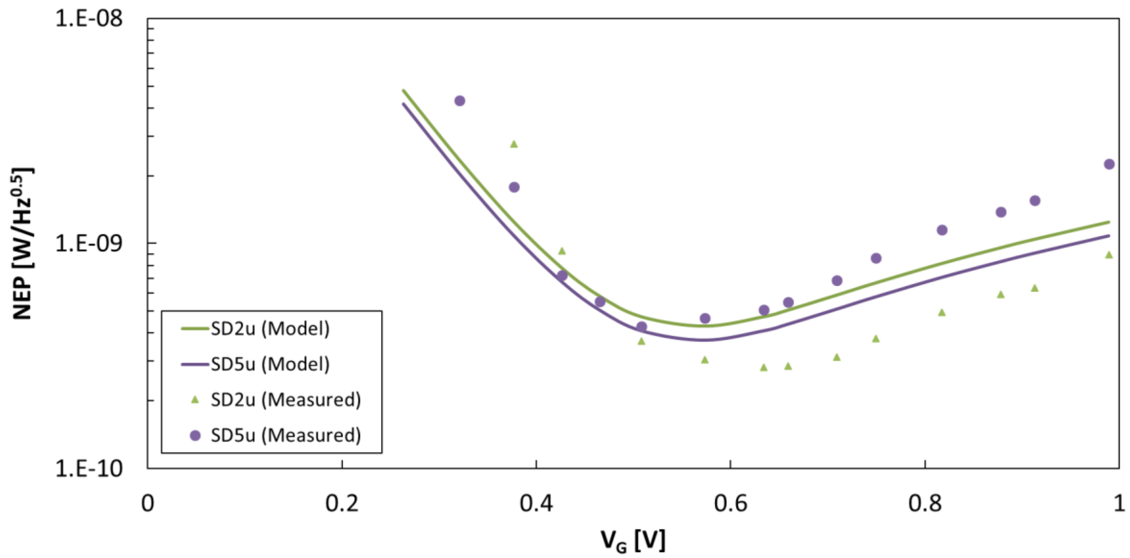


Figure 3.13. Modeled (solid line) and measured (dots) FET detector NEP over gate bias voltage V_G for the gate-driven structures at 320GHz frequency.

The former hypothesis on higher effective resistance is partly confirmed by the NEP graphs of Figure 3.12 and Figure 3.13, showing higher measured noise for low bias; a good agreement is obtained in proximity of the threshold voltage, while a generally lower noise is predicted for higher bias, that again suggests a discrepancy in the resistance modeling or a mismatch with respect to nominal transistor parameters. As it was noted for the responsivity of the 2μm source-driven structure, there remain a relevant discrepancy between the modeled and measured NEP, that is a direct consequence of the R_V difference.

Overall, both measurements and modeling confirm the better performance in terms of both responsivity and NEP of the small, gate-driven structure, that stems mainly from the matching

conditions with the antenna: a larger gate shows a higher capacitive component that shorts the input voltage reducing its magnitude and therefore the self-mixing result.

3.4 Performance Analysis Using the Model as a Tool

The good agreement obtained with the measured data allows to explore with confidence the effect of the technology and design parameters in eqs. (3.20), (3.21), and (3.22) in order to gather additional insight on the FET detector performance, and possibly optimize. The very same FET detector parameters used for the model validation are taken as a starting point.

3.4.1 Optimization of Antenna Coupling

One of the degrees of freedom that allows a large performance improvement is the antenna coupling, that is fully described by eq. (3.11). It is almost impossible to make general assumptions here, because each antenna design can have very specific behavior in terms of impedance, directivity, etc. However, usually known techniques such as conjugate impedance matching is used to maximize power transfer, and although it results in a 50% efficiency, it can be used as a valid benchmark. Therefore, by setting $Z_{ANT} = Z_{FET}^*$ (or $2 \cdot Z_{FET}^*$ for the source-driven case) and ε=0.5, eq. (5) becomes:

$$R_{eq-match} = \begin{cases} 2\dfrac{|Z_{FET}|^2}{Re(Z_{FET})} & GD \\ \dfrac{|Z_{FET}|^2}{2Re(Z_{FET})} & SD \end{cases} \tag{3.23}$$

This result contributes to explore a potentially maximum achievable performance in relation to the detector impedance, with the hypothesis of a matched antenna. By using this idealized and maximized R_{eq}, a minimum sized 0.4μm/0.18μm FET detector results to be able to achieve, at the frequency where this condition occurs, up to 35.4kV/W responsivity and NEP down to 1.5pW/√Hz. These values are compatible with findings in literature, where the best detectors with similar configurations reach noise-equivalent power values of about 12pW/√Hz [Jain2018].

3.4.2 Performance of submicron technology nodes

Many circuits and sensors take advantage of the scaling of CMOS technology. One possible question to address could be: can CMOS THz FET detectors benefit from technology scaling towards smaller nodes? There is a first point to consider, that has been already mentioned when evaluating the development of the rectified DC voltage along the channel: there is need for a minimal gate length in order to reach the full detected value [Lisauskas2009]. Moreover, the optimal gate length has been studied in [Andersson2016], with the outcome that in all practical cases the optimum goes towards the smaller realizable length.

In this analysis, with the help of the developed model, the intention is to focus on the dependence of the performance on the technology node, therefore on a set of foundry-specific C_{ox}, k_n, minimum W, L, etc. The parameters of four CMOS technologies at different nodes have been considered: 0.35 μm, 0.18 μm, 0.15 μm, and 0.13 μm. By using eq. (3.12), the detector impedance has been evaluated for minimum sized MOSFETs and the responsivity and NEP have been calculated with eqs.(3.21) and (3.22) for conditions similar to the measurements of paragraph 3.3.2.

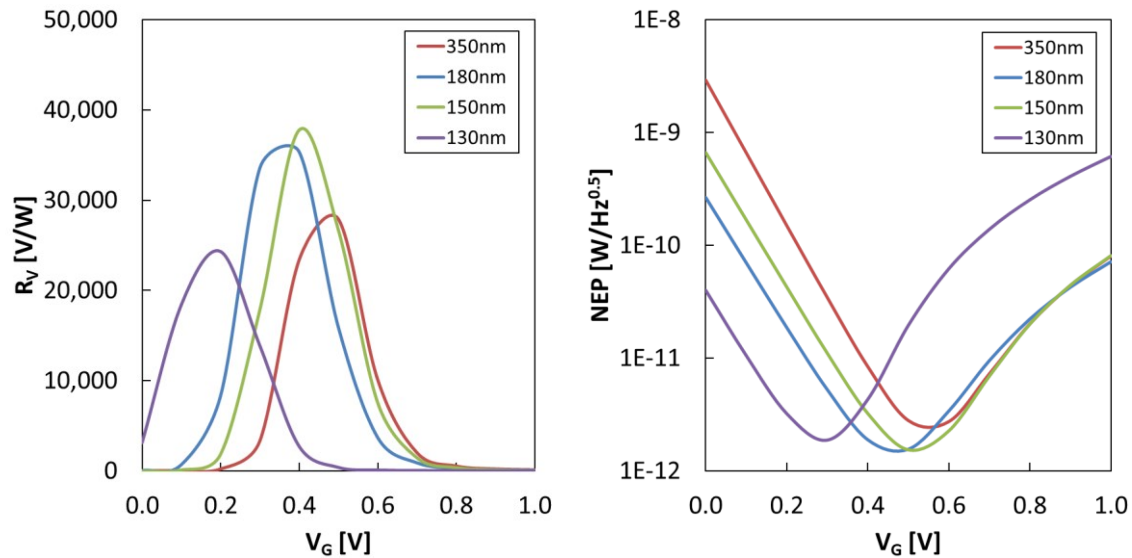


Figure 3.14. Best responsivity and NEP with ideal antenna matching, parametrized with several technology nodes at 320 GHz.

The graphs of Figure 3.14 show a relevant different of the optimum bias point, due to the different threshold voltages of the examined technology nodes. However, despite some differences between the technology nodes, there is no clear trend towards the choice of a deep-submicron technology. Overall, the model gives similar values of minimum achievable NEP, between 1.5 and 2.7 pW/√Hz. This is consistent with measurements reported in literature: Figure 3.15 compares the minimum NEP obtained from the model with the best NEP of several works in literature, depending of the technology node. It can be noted that in both cases there is no trend depending on the node of the selected technology, meaning that the detection principle does not seem to take advantage from process scaling. This is a relevant result as the relatively large size of antennae brings to large integrated circuits, thus increasing the cost of the sensor: if cheaper technologies can achieve anyway high performance, a cost-effective device can be realized.

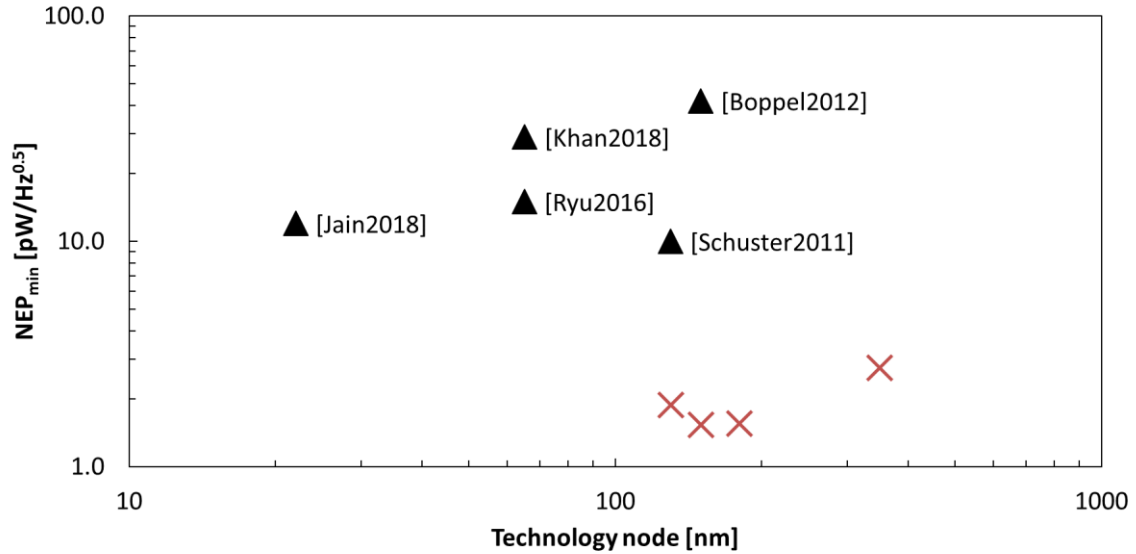


Figure 3.15. Simulated minimum theoretical NEP (crosses) and best NEP of some high-performing references in literature (triangles) with respect to the used CMOS technology node

3.4.3 Impact of Other Design Parameters

The analysis of the role of the different parameters is complex and must be applied case by case. Indeed, those variables often are involved in more than one aspect of the equations (electrical response of the detector, antenna matching conditions, etc.). Therefore, there is a tight correlation with the design of other components like the antenna or the readout circuit.

Neglecting the coupling with the instrumentation, the responsivity of eq. (3.21) results to be influenced only by V_t (thus temperature), V_G-V_{th} (bias point), ideality factor η, conductance k_n and aspect ratio *W/L*.

It is evident that the main "knob" for the designer is *the aspect ratio W/L*, that however plays at least a double role: it contributes to the antenna matching expressions, and it determines the amount of noise generated by the channel. As it has already been noted in Section 3.2.2 and proven by the measurements, the effect on the impedance matching is dominant and it brings often to the choice of minimum-sized transistors, unless differently required by the coupling with the antenna.

Another aspect that the model predicts, interestingly very recently published and realized in [Shaulov2020], is about the factor $2-\eta$, amounting typically to ≈0.5: this term stems from the subtraction of the approximations of forward and reverse currents. Indeed, it depends on the equations boundary conditions of coupling the RF wave to the drain with zero phase difference, i.e. $v_d = v_g$: alternatively, the RF wave can be coupled with 180° shift as in [Shaulov2020], so to obtain $v_d = -v_g$. The mentioned factor therefore changes to $2+\eta$, bringing this multiplicative term from $2-\eta \approx 0.5$ to $2+\eta \approx 3.5$, boosting the responsivity in the same way.

This explains the remarkable NEP of 3.5 pW/√Hz that is ~4x better than any other work in literature.

Another example are detectors with reduced parasitics or increased asymmetry such as in [Ryu2016]. By examining the role of W in R_V and NEP, it has been found that it is better to keep minimum width for better coupling, reducing the capacitive load, but at the same time a larger width would bring a lower channel noise. The capacitive component is seen from the gate-source side, while there is no disadvantage in setting a wider gate and therefore a larger capacitance at the drain side: in [Perenzoni2016] and [Khatib2018] this has been addressed by designing a trapezoidal gate to achieve higher response and lower noise.

These results show that there is still freedom left to investigate between the lines of the equations to find clever improvements and optimizations.

3.5 Chapter Summary

The modeling and understanding of the THz FET detector is of paramount importance, but at the same time models should be accessible, easy to use, and should require just available parameters, typically the ones made available by the foundry process design kits.

With these requirements in mind, starting from an approximation of the EKV MOSFET model, a complete and handy description of the detector operation has been extracted, including all relevant contributions: antenna coupling, rectification, measuring instrumentation. The advantage of the model is its completely analytical structure, enabling direct observation of the roles of variables. Nevertheless, accuracy can be improved by numerically addressing the most critical parts: for example, the modeling of the FET impedance requires to consider also the surrounding geometry that is best addressed with finite elements high-frequency simulations.

The model equations have been validated: structures implementing variations of several conditions, like the topology or the FET width, have been measured and compared against predicted values, with good agreement.

The capability of the model to extract the performance upfront has been exploited to perform some analysis, for example concerning the dependence on the technology node and the best achievable responsivity and NEP. One of the results is that the main improvements come from an optimal antenna coupling (bringing potentially to a NEP<2.7 pW/√Hz). By working in between the details of the equations it is possible to find ways to improve the detector, modifying for example the phase of the drain coupling, or the device structure (i.e. asymmetry).

The obtained model is therefore an important tool, both for learning the detector operation thanks to its simplicity, and for designing optimized devices and predict their performance.

4 MULTISPECTRAL THZ-VIS IMAGE SENSOR DESIGN

Several attempts have been done in literature concerning multispectral imaging including the terahertz spectral range, either employing different detector technologies of trying to monolithically integrate different detection principles.

The main objective of this thesis is to achieve simultaneous real-time acquisition of terahertz and visible images with a single integrated CMOS image sensor, without any need for customizing the fabrication process, i.e. using only standard CMOS by exploiting the FET detection scheme described in the previous sections. Driven by the already proven FET detectors and antennae, together with the availability of a laboratory source, a target frequency of about 325GHz is chosen.

In this chapter the concept, design and realization of the multispectral camera will be described.

4.1 MULTISPECTRAL TERAHERTZ AND VISIBLE IMAGING CONCEPT

As anticipated in paragraph 2.4, there may be several ways to implement multispectral imaging. The approach here adopted is to realize true multispectral detection at focal plane array level, with specific pixel structures.

4.1.1 The System

The camera system, therefore, is composed by the focal plane array of pixels and an imaging optics that creates the focused image of the object under observation onto the sensor. Passive terahertz imaging is out of reach, and therefore active illumination is foreseen.

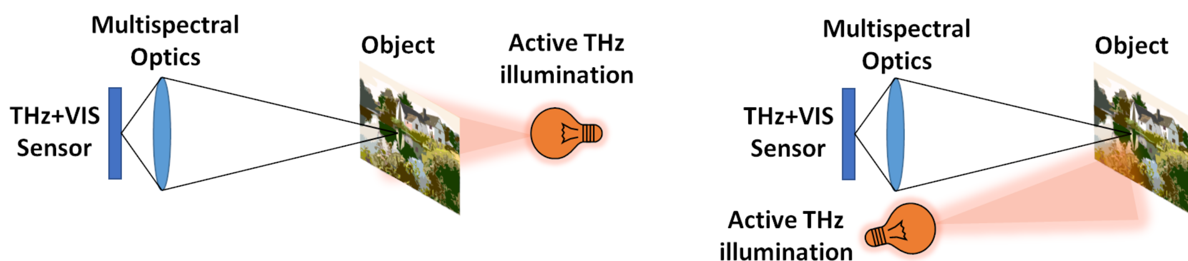


Figure 4.1. Concept of terahertz and visible camera, with visible ambient illumination and active terahertz imaging, possible in transmission mode (left) or in reflection mode (right)

Figure 4.1 shows two possible configurations, where the active THz illumination can respectively realize:

- *Transmission terahertz imaging*: in this case, the overall power budget is optimized as the source points directly towards the sensor. In this configuration only relatively thin

and transmissive objects can be observed. The setup is overall not operating as a standalone camera, but the object has to be somehow “inside” the optical setup.

- *Reflection terahertz imaging*: the power budget is here affected by two important losses, namely the path loss due to the spread in distance of the power density, and reflections that in the terahertz range are often specular and do not provide return into the camera optics. This setup is viable for thick objects where the interface layers have to be observed, and provides potentially a standalone camera pointing at an external object.

In terms of power budget, the reflection setup is much more challenging and although very interesting, still difficult to achieve in real operating conditions. Therefore, the operation in transmission is considered.

4.1.2 The Optics

The optics is another important point: it has to be capable of focusing in the same way both visible and terahertz radiation [Brundermann2012]. To this end, two options can be envisaged, as pictorially indicated in Figure 4.2:

- *Refractive optics* making use of lenses having similar refractive index in both visible and terahertz range. There exist a number of polymers that have this property: for example Tsurupica (or Picarin) having a n = 1.56 (THz) – 1.55 (VIS), and Poly-4-methylpentene-1 PMT (commercial name TPX) with n = 1.46 (THz and VIS). The disadvantage of refractive optics are the losses for absorption in the bulk material of at least ~0.1cm^{-1}, that cannot be considered negligible and account for typically 10% losses at sub-THz frequencies for a single lens.
- *Reflective optics* uses metallic mirrors, that typically possess a very broadband operating range. Usually mirrors are made of coated metals, like aluminum coated with quartz. This kind of imaging optics is slightly more complex than the refractive counterpart, and it may lose aperture due to the baffles needed to keep the mirrors in place. Typical simple schemes are for example the Newton telescope that needs only a spherical and a flat mirror, either in coaxial or orthogonal configurations.

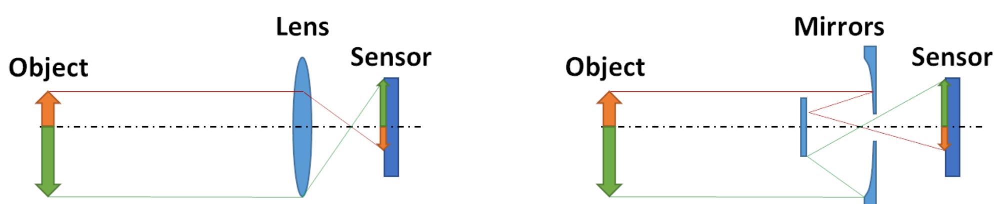


Figure 4.2. Simple imaging optics: single lens refractive optics (left) and Newton telescope reflective optics (right).

In both cases, the optics is characterized by a focal length *f* and an aperture *d* (diameter of lens/mirror) that together lead to the F-number $F_{\#}$:

$$F_{\#} = \frac{f}{d} \quad (4.1)$$

These quantities enclose several properties of the imaging optics: they determine the "brightness" (the lower the $F_{\#}$, the brighter the optics is), the field of view, the minimum resolvable details. This latter point is important in terahertz as the relatively large wavelength brings to relevant limitations.

It can be shown that, being the lens (or mirror) effectively a circular aperture, it causes diffraction: therefore, a point source projects a pattern on the focal plane (the Airy disk) that is the point-spread function (PSF), equivalent to the square modulus of the Fourier transform of the aperture. It therefore limits the minimum resolvable distance when two distinct point sources are imaged, because the Airy disks at a certain point start to merge in the focal plane, thus relating the optics characteristics to the minimum pixel size.

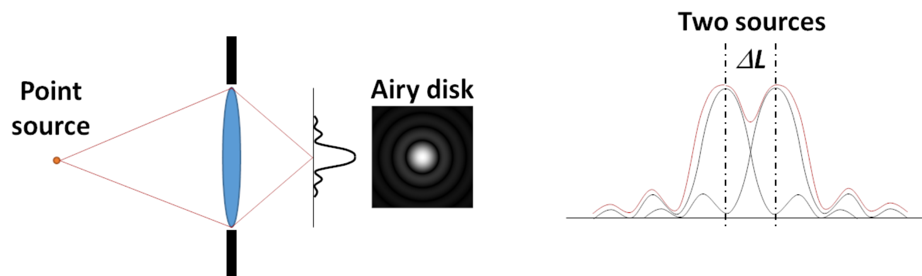


Figure 4.3. Airy pattern projection by a lens seen as an aperture and Rayleigh limit for resolving two objects

The Rayleigh criterion defines this minimum value when the two PSFs align their first zero with the peak of the other (see Figure 4.3):

$$\Delta L = 1.22\lambda F_{\#} \quad (4.2)$$

In the considered sub-terahertz range (~325GHz), the wavelength is in the order of the millimeter, which means that in the focal plane the Airy disk has a diameter of 1.22mm with unitary F-number. Of course, in the visible range this limit is much lower and does not currently represent a limitation.

From these considerations, it is possible to understand how to sample the focal plane in order to reconstruct two separated point sources. In [VanBerkel2017] the focal plane sampling has been analyzed and traded off with several other imaging parameters, showing that a pitch of $0.5F_{\#}\lambda$ defines the boundary between spatially under- and over-sampled focal plane. For our example at 325GHz and $F_{\#}$=1 this corresponds to approximately 500μm.

4.1.3 The Sensor

The sensor must be able to sense, on the same plane, the visible and terahertz radiation with properly designed pixels. The terahertz radiation has to be captured by an antenna for each pixel, that typically has dimensions in the order of magnitude of the wavelength. Together with eq.(4.2) this is another factor that is involved in determining the pixel size: the wavelength and the antenna effective area. Indeed, the receiving antenna is characterized by an equivalent extension that determines the area of interaction with the electromagnetic field (see paragraph 3.2.2 and eq.(3.10) of the model). The effective area depends on the wavelength λ, but also on the antenna directivity $D(\lambda)$ as:

$$A_{eff} = \frac{\lambda^2 D(\lambda)}{4\pi} \quad (4.3)$$

Highly directive antennae have therefore large effective area, but in turn they also require large physical size. Indeed, again the antenna can also be seen as an aperture: the smaller the aperture, the stronger the diffraction leading to a low directivity. The effective area of an idealized isotropic radiator, with $D(\lambda)=1$, is equivalent to a circle of radius $\lambda/2\pi$. For a ~325GHz radiation, the effective area can be seen as a circle having at least >300μm of diameter. While this is an advantage for the available per-pixel area for electronics, it is also a cost in terms of silicon area: slightly smaller pixels can be designed exploiting the shrinking of the wavelength in the silicon by realizing illumination from the back side.

State-of-the-art visible pixels instead have been designed with size below 1μm, almost reaching the diffraction limit. As shown in 2.2, very little electronics is required for reading out the signal, with the result that there is a huge discrepancy between the desired THz and visible pixel dimensions, a factor >100x.

In order to cope with this large difference, the decision has been to fit more visible pixels within one terahertz pixel, in order not to waste the available higher resolution in the visible domain. This, in perspective, also could enable the use of smart algorithms or machine learning techniques in order to improve the resolution in the THz while exploiting the additional features in the visible. Figure 4.4 depicts the multispectral pixel concept.

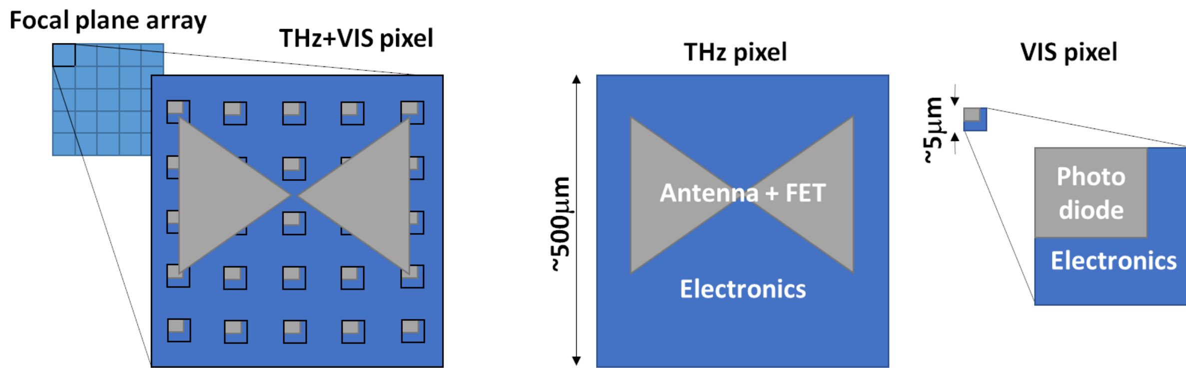


Figure 4.4. Concept of the multispectral pixel, with one terahertz pixel containing multiple visible pixels.

Another important aspect to consider during the definition of the multispectral image sensor, and in particular of the terahertz sensing part, is the capability of performing *simultaneous acquisition and integration over the whole focal plane array*: in contrast with a sequential integration, it allows to reduce the bandwidth of the noise asymptotically down to the frame rate, while strengthening the signal amplitude. Therefore, the terahertz pixel shall contain integrating readout channels able to operate in parallel, that are read-out only at the end of the integration period, in a global shutter fashion.

A 150nm standard CMOS technology has been chosen for the realization of the multispectral image sensor, having 1.8V transistors, 6 metal levels, metal-insulator-metal (MIM) capacitor option, and a thick metal option.

4.2 Terahertz and Visible Imager Design

In order to realize the concept described in the previous section, several choices have been made.

An antenna-coupled FET detector is the heart of the terahertz pixel, while for the integrating electronics an approach involving direct analog-to-digital conversion has been pursued. In particular a ΣΔ first-order incremental converter has been designed. Incremental converters [Markus2004] are particular types on analog-to-digital converters, belonging to the family of ΣΔ converters, that by oversampling well beyond the Nyquist frequency actually realize an integrating function and a quantization noise reduction (called noise shaping), progressively refining the conversion by repeatedly looking at the input. In addition, continuous-time ΣΔ incremental converters have the additional advantage of integrating also during the clock intervals, thus really optimizing the signal to noise ratio. The pixels produce a digital output, that is therefore addressed in the focal plane and streamed out via digital pads.

The visible pixels are chosen to be simple 3T pixels, with a full analog readout chain; given the size of the terahertz pixel of about ~500µm and the need to have both wavelengths readout

electronics coexist, it has been decided to fit 5x5 visible pixels inside a terahertz pixel. With the available chip area for the design of the imager, this brings to an array size of 10x10 THz and 50x50 VIS pixels.

In the following, the main blocks of the chip are described, highlighting the design tradeoffs and choices.

4.2.1 The FET-based THz detector

A 325GHz bow-tie antenna has been designed by making use of the thick metal option of the technology. In contrast with the design of paragraph 3.3.1, in order to reduce the substrate waves and decrease the associated losses, a shield (ground plane) has been designed with the first metal level. The other known technique in literature, the backside illumination with substrate lens, has been discarded because it would have blocked the visible light contribution. Due to the chosen technique, designing the antenna with all remaining metal levels would have decreased considerable the efficiency because of the very small distance antenna-ground plane. Therefore, to limit the losses in the metal, a 6-μm thick metal option available in the chosen technology has been exploited: this reduces the sheet resistivity of the antenna and keeps at maximum the thickness of the dielectrics in the cavity. In order to guarantee manufacturability, a minimum density on 30% on all metal layers is needed, and therefore properly placed dummy fillers have been added. The contacting to the FET detector is ensured by a stack of 2x2 VIAs running through all metal levels. Figure 4.5 shows a 3D view of the model that has been used for antenna simulation and tuning.

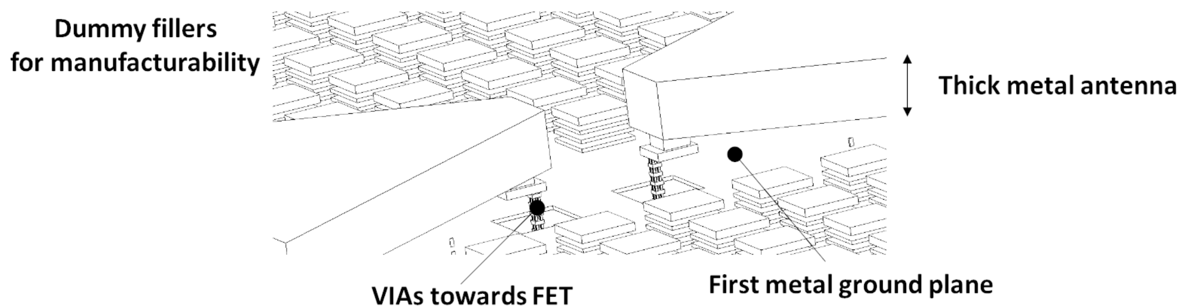


Figure 4.5. 3D view of the implemented antenna with highlighted the main features.

The FET detector is realized in the gate-driven configuration, exploiting the extended source improved geometry: responsivity and NEP characterization of single standalone pixels of size 456x456μm^2 are reported in [Perenzoni2016], giving $R_V=279V/W$ and $NEP=192pW/\sqrt{Hz}$ at a bias of $V_G=0.45V$, in the proximity of threshold voltage $V_{th}=0.485V$.

4.2.2 The THz readout electronics

The operating principle of the 1st order continuous-time ΣΔ converter implemented in the pixel can be seen in Figure 4.6. A first order structure has been chosen for the simplicity of the decimator, that can be implemented as a simple counter and therefore fitting the limited pixel area. The converter has been realized in a fully-differential structure, thus requiring a dummy input that is provided from a FET not connected to any antenna. The transconductance blocks G_m (direct) and G_{mf} (feedback) are chopped in order to reduce the 1/f noise contribution and the decimator is implemented through an up-down counter, which enables realizing a digital modulation that can be used to operate the pixel in "lock-in mode" with a modulated source. Detailed insight on the realization of the single blocks is given in [Khatib2017] and [Khatib2018b], together with simulations and performance data.

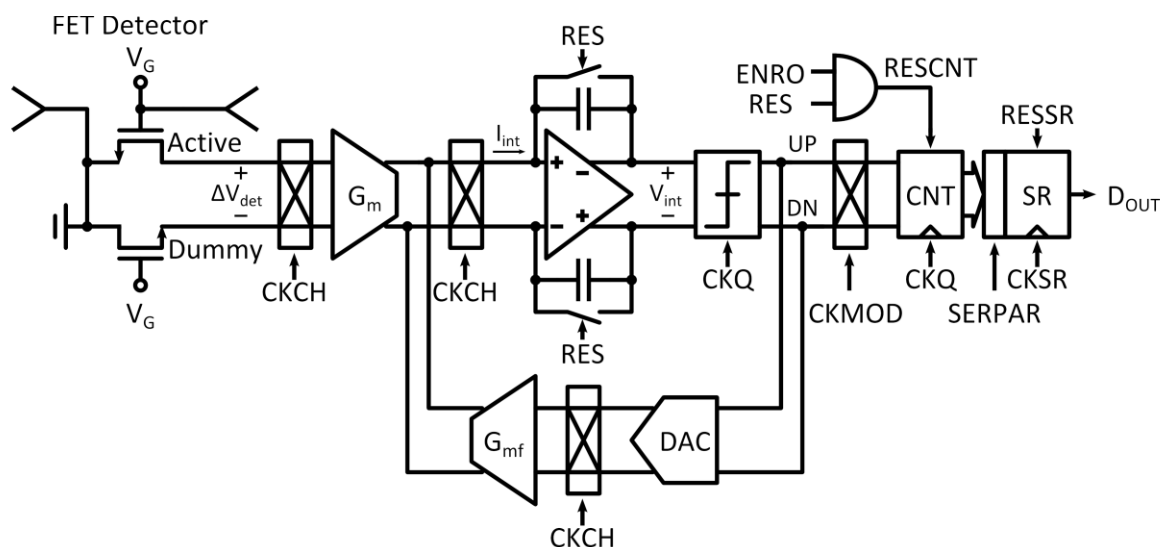


Figure 4.6. Principle schematic of the 1st order ΣΔ incremental converter realized inside each pixel, having at its inputs an active and a dummy detector

The detailed operation is represented in the diagram of Figure 4.7: at the beginning of the conversion (also referred here as integration time T_{int}) both the integrator and the counter are reset and then released. The input signal ΔV_{det} between the active and dummy detectors is converted into a current by the input transconductor. The quantizer clock *CKQ* runs at the oversampling rate and periodically determines whether the feedback transconductor should sum or subtract a fixed current I_{ref}, depending on the state of the integrator's output V_{int}. The feedback and the fact that the integrator is never reset again, determines the so-called noise shaping, typical of ΣΔ converters: the integrator stores the residual quantization error that is continuously fed back, and reduced in the long run. The chopping clock *CKCH* modulates any 1/f noise and offsets introduced by the transconductors at multiples of its frequency f_{ch}: these are in turn filtered by the integrator and substantially reduced.

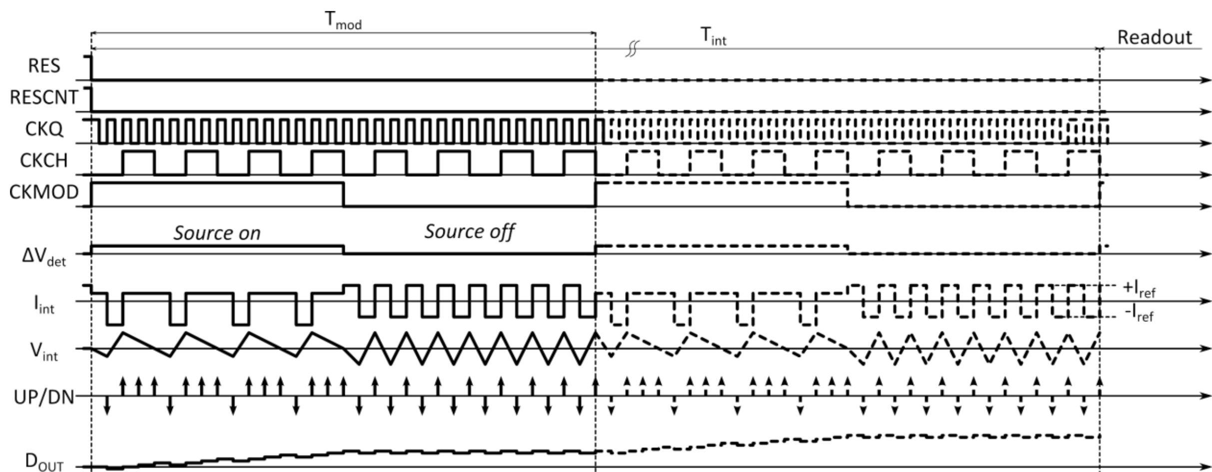


Figure 4.7. Driving waveforms of the terahertz readout channel and pictorial representation of the signals in the incremental conversion operation.

An additional digital modulation *CKMOD*, not usually present in ΣΔ incremental converters, allows inverting the counting direction synchronously with the terahertz source modulation: this causes, after the period T_{mod}, a subtraction of residual offsets or slowly varying disturbances superimposed with the weak detected signal, effectively implementing an in-pixel lock-in operation. After several source modulation periods (i.e. at the end of the integration time) the accumulated counts effectively represent the digital representation of the signal and can be read-out by means of a parallel-to-serial converter.

The key parameters for the sizing of the converter have been extracted and optimized with detailed simulations and are listed in Table 4-1.

Table 4-1. Key parameters of the terahertz readout channel based on a 1st order ΣΔ incremental converter

Parameter	Symbol	Value
Input transconductance	G_m	20μS
Feedback transconductance	G_{mf}	3.2μS
Integration capacitance	C_{int}	1.0-1.5-2.0 pF
Nominal DAC outputs	ΔV_{ref}	40mV
Oversampling frequency	f_q	1MHz
Chopping frequency	f_{ch}	100kHz
Modulation frequency	f_{mod}	<1kHz
Counter depth	N_{ADC}	12bit

Some quantitative consideration can be made on the main driving specifications. In terms of signal, it is expected to have a full-scale input of ~1mV and, based on the FET detector results in [Perenzoni2016] reported in paragraph 4.2.1, to sense a minimum detectable signal equal

to $V_{LSB} = R_V \cdot NEP \cdot \sqrt{\Delta f} = 279V/W \cdot 192pW/\sqrt{Hz} \cdot \sqrt{1kHz} = 1.7\mu V$. Optimally, this would need 10bit of dynamic range or effective resolution.

The available terahertz source has a maximum modulation frequency of 1kHz, which brings to a minimum integration time of $T_{int}=1ms$. At the same time, the 1/f corner frequency results to be at ~10kHz, which fixes the chopping frequency a decade higher, $f_{ch}=100kHz$, to ensure proper noise rejection. With the previously extracted goal of 10bits of effective resolution, due to the unknown offsets, the counter is reset at mid-range 2^{NADC-1} and its depth is tuned in order to avoid saturation or wrapping even with 500Hz of modulation frequency: this brings to the counter depth of $N_{ADC}=12bit$.

In presence of the minimum signal and no offsets, it is desirable that the gain of the ADC is enough to enable switching at least 1 bit, therefore the increase of the integrator output introduced by the detected signal $V_{LSB} \cdot G_m \cdot T_{int}/C_{int}$ should be higher than the value $V_{ref} \cdot G_{mf} \cdot (T_{int}/2^{NADC})/C_{int}$ compensated during the maximum 2^{NADC} cycles by the feedback. This constraint sets $\Delta V_{ref} \approx 40mV$: the smaller this value, the higher the "gain" of the ADC in terms of digital numbers per unit voltage:

$$G_{ADC} = \frac{1}{V_{LSB}} = \frac{2^{N_{ADC}} G_m}{\Delta V_{ref} G_{mf}} \quad (4.4)$$

With these numbers, the expected gain is $G_{ADC}=0.64LSB/\mu V$. The integration capacitor value and the transconductances are chosen with tradeoffs that consider the area occupation and noise, as well as some margin for the saturation. Indeed, the $\Delta V_{ref}=40mV$ is converted to a current $\Delta V_{ref} \cdot G_{mf} = 40mV \cdot 3.2\mu S = 128nA$, that into the smaller $C_{int}=1pF$ capacitance in two clock periods (in certain conditions two periods at maximum slope can happen) $2T_{CKq}=2\mu s$ brings to $256mV$ swing, still small enough to keep the integrator into the correct dynamics. Additionally, the feedback transconductance is intentionally made smaller than the input transconductance to bring the formerly extracted ΔV_{ref} value into a practical range.

A similar single readout ADC channel has been characterized in a former work, achieving satisfactory performance as described in [Khatib2017], while the described circuit presents some minor changes in the design with the aim to decrease the variability in a large array (i.e. larger critical devices, smaller gain – transconductance – of the input stage).

4.2.3 Visible Pixels and Readout

The visible pixel and the whole readout channel until the signal delivery out of the chip is shown in Figure 4.8.

A 3T APS is chosen as pixel architecture, as the technology did not provide pinned photodiodes or transfer gates. The 2D array is connected vertically through common lines, to

which the pixels are sequentially connected by a row decoder. The vertical bitlines are biased by a constant current and provide the input of the column amplifier. An operational transconductance amplifier (OTA) is configured in order to perform a subtraction operation for a correlated double sampling (CDS) at the column level, reducing the offsets between the response of the different pixels. The outputs of the column amplifiers are sequentially selected through an analog switch driven by a column decoder, and delivered to the output buffer that eventually drives the output pad with an analog voltage.

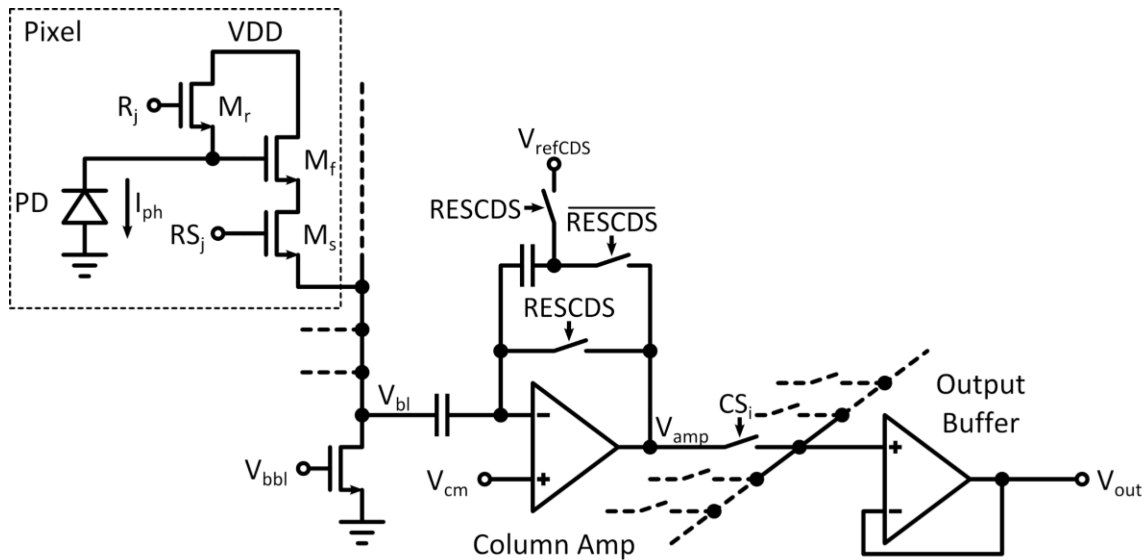


Figure 4.8. Schematic of the visible imager readout chain, comprising the pixel in the array, the column amplifier, and the output buffer

Figure 4.9 depicts the detailed operation: the architecture is designed to operate in rolling shutter mode, i.e. integration of one row occurs while all other rows are being read out, sequentially. Therefore, there is a continuous rolling selection of rows through the row decoder. One frame begins when the reset signal R_0 is released at the first row and all pixels of that row begin the integration, with the photocurrent discharging the photodiode parasitic capacitance by $I_{ph}T_{int}$. Before the end of the integration time the row selector RS_0 is activated, forming a voltage follower (of gain $A_{sf}<1$, typically ≈0.7) transferring $A_{sf}(V_{PD}-V_{GSMf})$ on V_{bl}, with V_{GSMf} the gate-source bias voltage of M_f; simultaneously, *RESCDS* goes high to reset the column amplifier to V_{refCDS} and store on the input capacitor the value $A_{sf}(V_{PD}-V_{GSMf})-V_{cm}$.

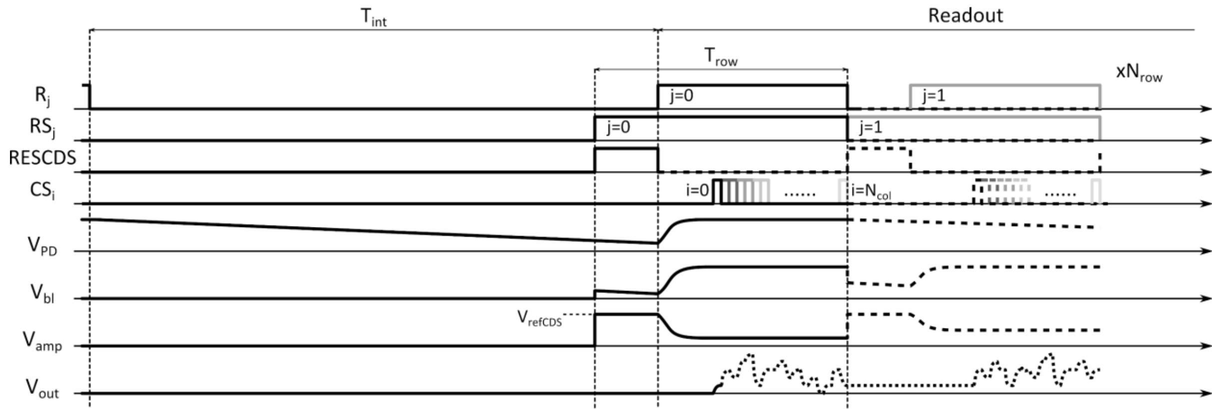


Figure 4.9. Driving waveforms of the visible pixel and column amplifier, and pictorial representation of the signals in the readout chain.

After a short settling time, *RESCDS* is turned off and the pixel row is reset, forcing the photodiode to $V_{res}=V_{DD}-V_{thMr}$: this is called *soft-reset* because the node is charged to V_{DD} by a nmos, with an advantage in terms of reset noise and use of only n-type transistors, but with a drawback on the voltage dynamic range. During this phase the output of the column amplifier follows only the difference of the input with respect to the previously sampled value, therefore settling to $V_{refCDS}-A_{sf}[(V_{res}-V_{thMf})-(V_{res}-V_{thMf}-I_{ph}T_{int})]=V_{refCDS}-A_{sf}I_{ph}T_{int}$. Without considering further non-idealities, the subtraction removes uncertainties due to both V_{GSMf} and V_{thMr} , expected to vary across the array due to mismatches. After a determined reset time, the value at the output of the amplifier is considered to be settled and the column decoder scans all column amplifiers sequentially, producing at the output of the final buffer a stream of analog values representing the gray scale of the acquired image.

4.2.4 Overall imager architecture

Assembling together the two pixels is a challenging task and some aspects have to be sacrificed. For example, in order to keep a regular pitch, there are several visible pixels that result to be behind the antenna, thus resulting partially or totally blind. Also the terahertz readout has to make room for the 8x8μm^2 slots for the visible photodiodes falling within that area. The overall result is shown in Figure 4.10: the pixel layout is a modular component that can be easily arrayed, with all control signals, biases, supplies and outputs running vertically and horizontally. The peripheral circuits will have to be connected to the external boundary of the array and will be able to access every single THz and VIS pixel by using x-y addressing.

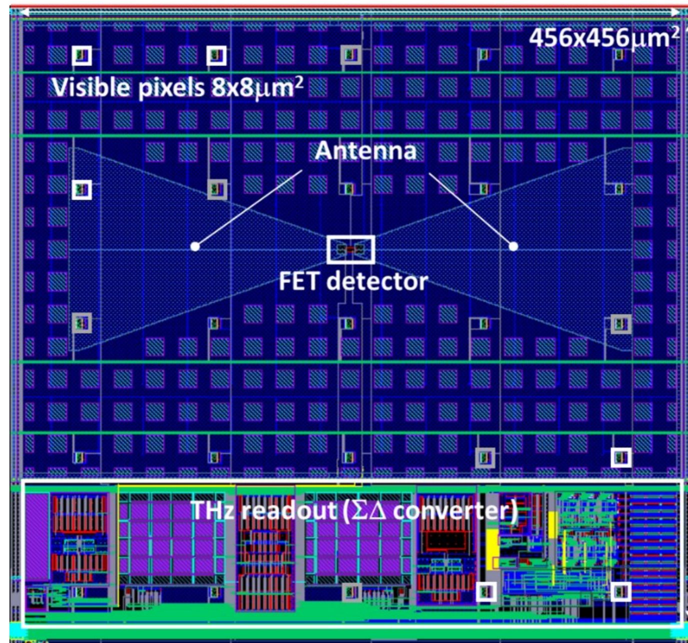


Figure 4.10. Final layout of the multispectral THz-VIS pixel with highlighted the main parts.

The previously developed blocks are assembled together in the architecture depicted in Figure 4.11, where also the ancillary components, i.e. decoders, bias generators, clock drivers, are included. The 10x10 THz and 50x50 VIS pixel arrays are addressed row by row, by means of two dedicated row decoders. At the column level the serialized THz value, already converted in the digital domain, is rerouted through the logic to a digital output pad. On the other hand, the VIS signal performs a last processing at the column level (as described in 4.2.3) and then serialized in analog format on a single analog voltage output. Digital control signals are conditioned (e.g. generation of non-overlapping phases) and delivered to the array and column circuits by a digital control block, while gate voltages for currents in the pixel and in the column amplifiers are generated and delivered by a bias block for the whole array. A test mode allows monitoring the analog output of the incremental converter integrator.

As can be guessed from the drawing, the two overlapped imagers are totally independent, which means that they could be independently managed: for example, the VIS imager could run at twice the framerate with respect to the THz imager, or the VIS light integration could occur also during the THz readout, to optimize timing. However, optics with large aperture will be used, driven by the small THz intensity: this will collect a large amount of visible light too, therefore it is not expected to require long integration time. Therefore, a sequential THz-VIS acquisition is devised.

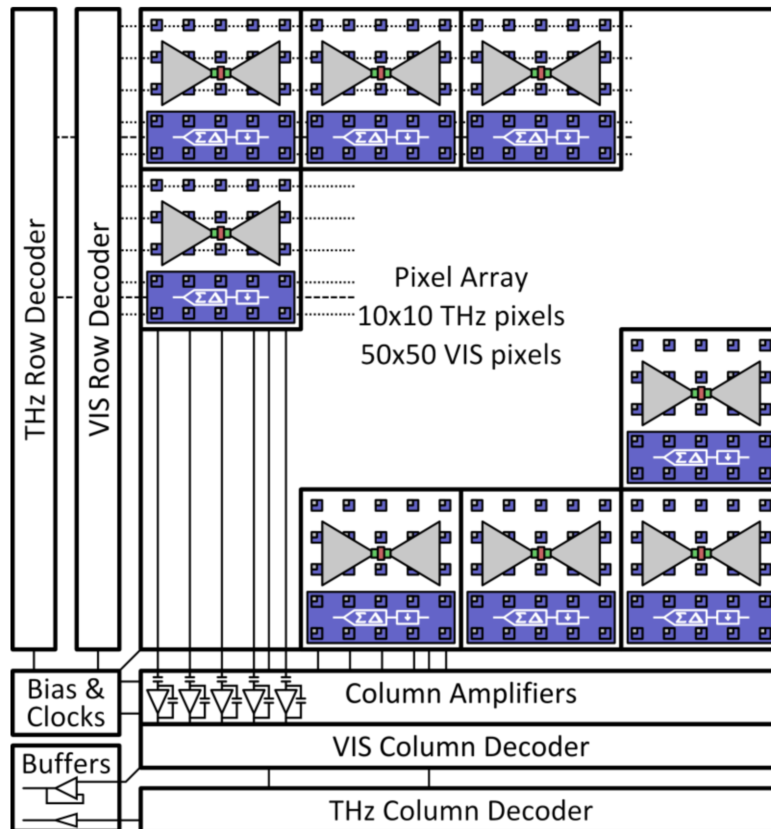


Figure 4.11. Architecture of the THz-VIS multispectral imager.

The multispectral THz+VIS image sensor has been fabricated in a 150nm standard CMOS technology: the micrograph of the device is shown in Figure 4.12. As noticeable, the pads are positioned only on one side: this will allow stitching multiple chips in the future, in order to enable acquisition of higher resolution images.

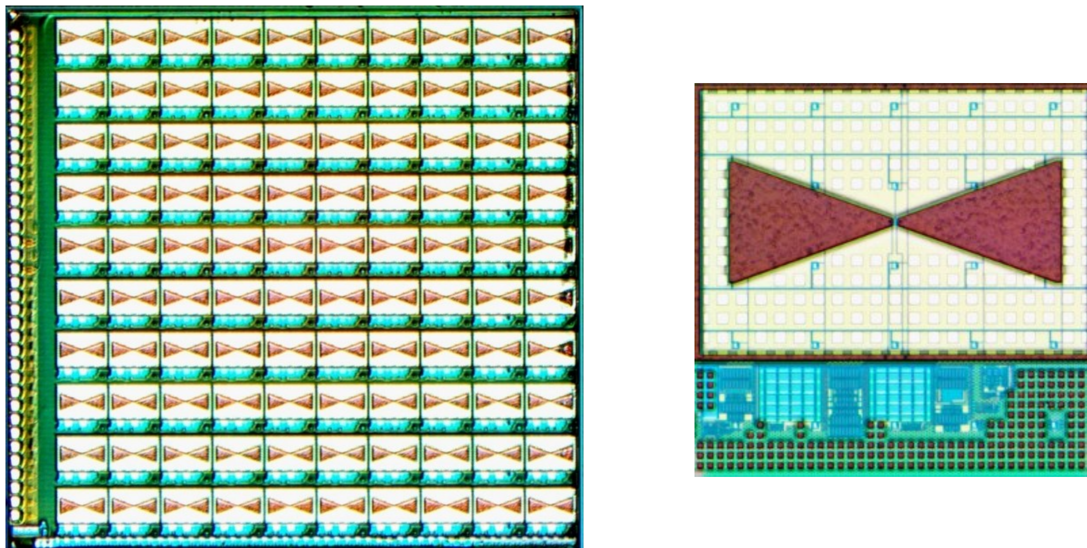


Figure 4.12. Chip micrograph of the fabricated 10x10 THz and 50x50 VIS multispectral image sensor in 150nm CMOS technology and zoom on one THz pixel, where the visible pixels are also recognizable.

The chip can be externally controlled with several digital and analog connections through the 34 pins that are listed in Table 4-2. In order to limit the number of pins, some signals have been shared: for example, the row and column decoders share reset and clock, while a selector signal (*THZVIS*) deviates them to the proper circuitry.

Table 4-2. Pin list of the multispectral imager with description and type

#	Name	Type	Dir.	Description
1	V_{PRE}	ANA	I	CM reset voltage for the Miller integrator, 0.9V
2	V_{biasCG}	ANA	I	Bias voltage for the Miller integrator, 1V
3	V_{CM}	ANA	I	CM voltage for the CDS, 0.9V
4	V_{REF}	ANA	I	Ref. voltage for the CDS and the Miller integrator, 1.3V
5	V_{REFp}	ANA	I	Input positive ref. voltage for the DAC
6	V_{REFn}	ANA	I	Input negative ref. voltage for the DAC
7	INTp	ANA	O	Positive test output of the Miller integrator
8	INTn	ANA	O	Negative test output of the Miller integrator
9	V_G	ANA	I	Input bias voltage for the active FET detector, 0.4V
10	V_{GD}	ANA	I	Input bias voltage for the dummy FET detector, 0.4V
11	V_{out}	ANA	O	Output voltage from the CDS
12	I_{BTHz}	ANA	I	Bias current for the THz channel, 0.4-4μA
13	I_{BVIS}	ANA	I	Bias current for the VIS channel, 10μA
14	I_{bbl}	ANA	I	Line bias current for the APS, 4μA
15	VDD	PWR	IO	Supply voltage (typ 1.8V)
16	VSS	PWR	IO	Ground
17	ENRO	DIG	I	Enable readout
18	SERPAR	DIG	I	Enable input signal for the shift register
19	CKMOD	DIG	I	Clock signal of the digital chopper,1 kHz
20	RESCDS	DIG	I	Reset of the CDS
21	RESSR	DIG	I	Reset of the THz channel shift register
22	RES	DIG	I	General reset for the THz/VIS pixel
23	DOUT	DIG	O	Output signal of the THz channel
24	CKSR	DIG	I	Clock signal of the shift register
25	CKCH	DIG	I	Clock signal of the chopper modulator, 100 kHz
26	CKQ	DIG	I	Clock signal of the quantizer/counter, 1 MHz
27	D1	DIG	I	Gain Control of the integrator
28	D0	DIG	I	Gain Control of the integrator
29	THZVIS	DIG	I	Readout mode control
30	RESROW	DIG	I	Reset signal of row decoder
31	RESCOL	DIG	I	Reset signal of column decoder
32	CKROW	DIG	I	Clock signal of row decoder
33	CKCOL	DIG	I	Clock signal of column decoder
34	CKPAR	DIG	I	Clock for parametric amplifier (not used)

4.3 CHAPTER SUMMARY

The design of a multispectral image sensor working at wavelengths that are orders of magnitude different requires to tackle the design with a holistic methodology, by addressing at the same time all the components and tradeoffs of an imaging system.

Considerations on the optics are important for the definition of image resolution, pixel size and materials to be chosen. The detector for each wavelength also drives many constraints, in particular in terms of detected signal. Indeed, one of the main points addressed in this chapter is the architecture definition and the signal chain from the detector to the output.

Eventually, an antenna-coupled FET detector with $\Sigma\Delta$ incremental converter readout chain has been chosen for the THz channel, while a 3T pixel with conventional column amplifiers and analog readout chain is selected for the VIS channel. An overall 10$\times$10-pixel array for THz and 50$\times$50-pixel array for visible has been implemented in a 150nm standard CMOS technology.

5 THz-VIS Characterization and Imaging Experiments

An image sensor operating in two different wavelengths needs basically to be characterized twice. In this chapter a detailed description of the multispectral imager characterization if given, with identification of issues and the relative fixes or workarounds.

While also the VIS imager is characterized, a stronger focus is reserved to the THz imager, that represents the most challenging and less explored field. In particular, due to weak expected signal, a thorough optimization of the operation is needed. This ensures that the THz imager is working in the best conditions, thus allowing to continue with more complete imaging experiments.

Eventually, a multispectral THz transmission and VIS imaging experiment is realized, acquiring simultaneous different details with two wavelengths.

5.1 Measurement Setup and Sensor Operation

The device has been assembled in a PGA121 package and a dedicated printed circuit board (PCB) has been designed in order to perform a complete characterization. The PCB fits into an established measurement system able to provide, through a motherboard and several National Instruments boards, a set of analog voltages and currents, several power supplies, digital and analog signal acquisition, and digital signal generation.

Since the beginning of the measurements, it was clear that despite the efforts of decreasing the effects on the mismatches, there is still a large non-uniformity between the different THz pixels. In particular, due to the lack of a common mode control at the output of the integrator, that was still working fine enough with one channel [Khatib2018b], the present difficulty is to preserve the channels from erasing the residual voltage with saturation. Several tricks have been applied to mitigate this issue, that partly modified the operation of the incremental conversion.

5.1.1 Issues of the THz channel

The THz channel was designed with in mind the possibility to implement the waveforms of Figure 4.7; however, the channel bias conditions are extremely sensitive to mismatches, bringing to the saturation of the common mode in just few tens of microseconds. The undesired result is that it would be possible to realize only short integration time T_{int} before a readout, thus deteriorating the efficiency of the acquisition: few tens of microseconds dedicated to the integration and milliseconds to the image readout, with an extremely low duty cycle, in the order of 0.1%.

However, a trick has been implemented in order to preserve the integrator from saturating: thanks to the *RES* signal it is possible to periodically apply short pulses, that reset only the integrator and recover its initial common mode value. This partly cancels the residual voltage in the integrator, thus decreasing the noise shaping effect: nevertheless, as the counter is not reset during this operation, it is possible to consider this way of operating the converter as implementing the average of several noise-shaped conversions. The overall integration time can remain of the nominal length, i.e. several milliseconds, with a largely increased readout time efficiency. By tuning the reset pulse to the proper length, it was also probably possible to avoid complete integrator discharge but enough common mode recovery.

5.1.2 Terahertz measurement setup

The measurement setup for the initial tuning and characterization of the terahertz channel parameters is sketched in Figure 5.1. A Tsurupica lens with *f=50mm* and *d=45mm* is used to focus the beam.

The source modulation is controlled by the control and data acquisition boards (DAQ) and it is synchronized with the *CKMOD* signal of the sensor array. Additionally, in order to remove any extra interference, a second and slow modulation is performed by exploiting the User-Controlled Attenuation (UCA) feature of the amplifier and multiplier chain (AMC) that performs a substantial block of the signal with *UCA=5V*, and no attenuation with *UCA=0V*. Differently from the TTL modulation, it is possible to attenuate only partially the signal using analog values at the UCA.

In place of the sensor it is possible to introduce a reference sensor that is needed for power calibration. The detectors are placed on a xy motorized micro-positioning stage to ease finding the terahertz beam.

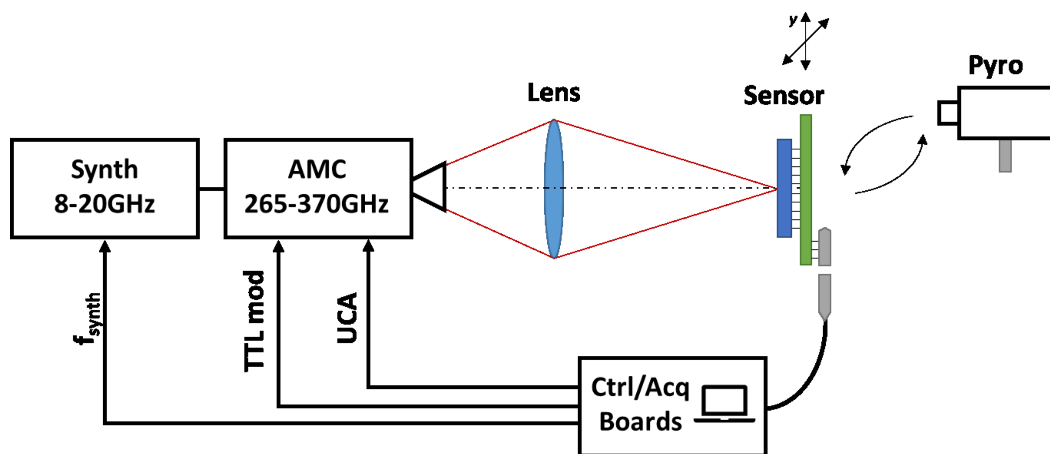


Figure 5.1. Measurement setup for THz channel optimization and characterization.

The DAQs are connected to a PC for data storage, processing, and automated measurements with programmable voltages on the motherboard.

5.1.3 Sensor control and waveforms

The multispectral sensor operation can be divided into smaller elementary and modular phases that can be repeated several times (e.g. the readout of a row) and therefore scripted. Table 5-1 shows the script used to perform all the measurements, where it is possible to change the number of repetitions or the specific waveform to realize different integration time, chopping period, etc.

A multispectral frame is composed by a THz frame and a VIS frame.

Table 5-1. Waveform generation script for the complete operation THz-VIS, integration and readout.

```
repeat forever
  generate ResetDecTHz                 // Reset of decoders and of THz pixels

  repeat 4                             // THz integration phase, 4x:
    repeat 50
      generate IntegrateTHzUpRes       //    Source on, 20μs (50x)
    end repeat
    repeat 50
      generate IntegrateTHzDnRes       //    Source off, 20μs (50x)
    end repeat
  end repeat
                                       // THz readout phase:
  generate Reset                       //    Reset, 1μs
  repeat 10
    generate RowTHz                    //    Readout each row, 15μs (10x)
  end repeat
                                       // VIS integration and readout phase:
  repeat 10
    generate Integrate                 //    Integration, 10μs (10x)
  end repeat
  generate Reset                       //    Reset, 1μs
  repeat 50
    generate RowVis                    //    Readout each row, 42μs (50x)
  end repeat
end repeat
```

The THz frame starts with the reset of the THz pixels (Figure 5.2) and then continues with the integration phase. This portion includes the repetition of two 20μs waveforms, *IntegrateTHzUpRes* and *IntegrateTHzDnRes*: they are identical except for the *CKMOD* signal (Figure 5.3), that indeed is also directly connected to the source modulation and determines whether the source is on or off. By properly repeating these two waveforms it is possible to define the modulation frequency: in the nominal operation of Table 5-1 these are repeated 50 times, for a total of 1ms on and 1ms off, thus reaching 500Hz modulation. Then, the overall modulation period is repeated 4 times to reach the total integration time of 8ms.

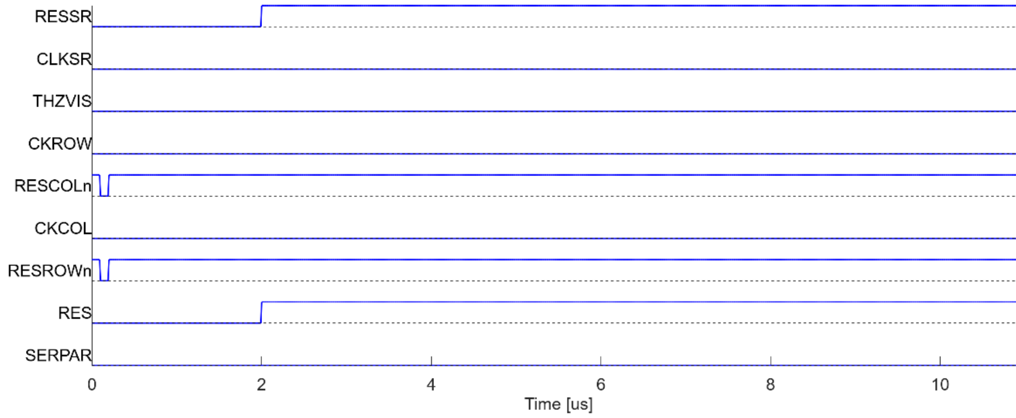
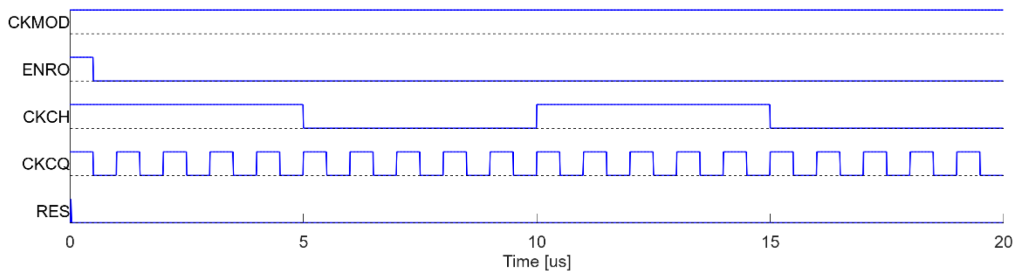


Figure 5.2. ResetDecTHz: reset of THz pixels



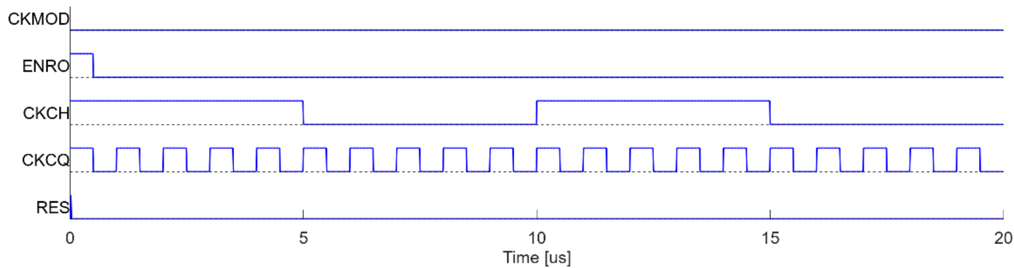


Figure 5.3. IntegrateTHzUpRes (top) and IntegrateTHzDnRes (bottom): elementary 20-μs THz integration waveform with source on and off, respectively.

The quantizer clock runs at the frequency of 1MHz, thus the counter is clocked up/down 8000 times: a small risk of saturation (counter wrapping) exists, however it requires extremely strong signal or offsets that have not been observed, and in case it is easy to decrease the integration time. The chopping runs at 100kHz and the integrator is reset every 20μs in order to avoid the undesired saturation of the common mode.

The terahertz readout phase begins with the reset of the decoders (Figure 5.4 with *THZVIS*=0) and then continues with the sequential row-by-row readout using 10 repetitions of *RowTHz*: this waveform (Figure 5.5) contains the serialization of the 10 pixels of the selected row, by means of the in-pixel parallel to serial converter. Overall, the readout phase takes 10x15μs of pixel delivery, with a total of 150μs readout time, a very small fraction of the terahertz integration time.

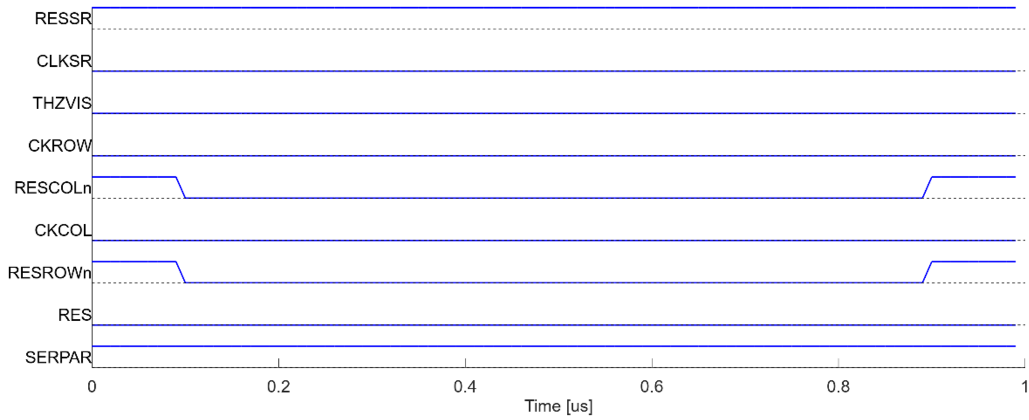


Figure 5.4. Reset: row and column decoders reset, with THZVIS selecting which readout path is being used

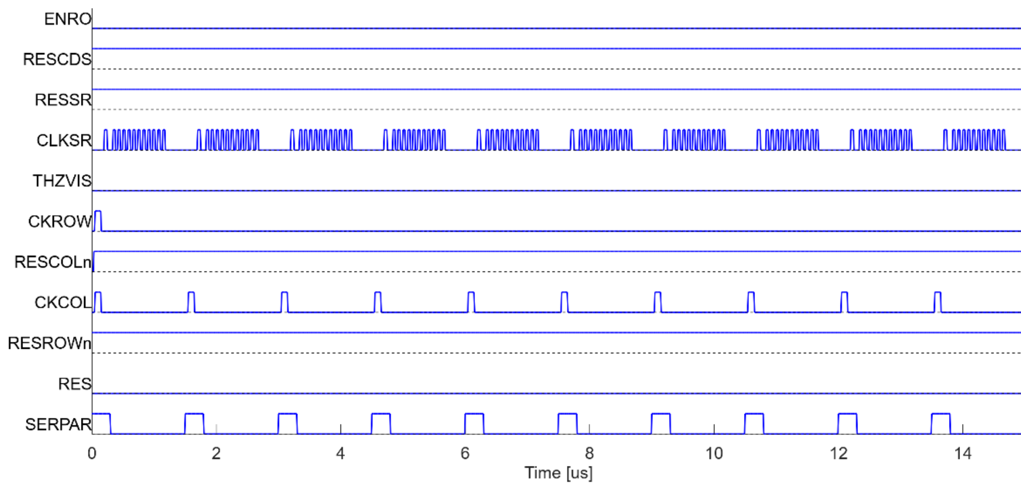


Figure 5.5. RowTHz: serialization of the single bits of 10 THz pixels in the selected row

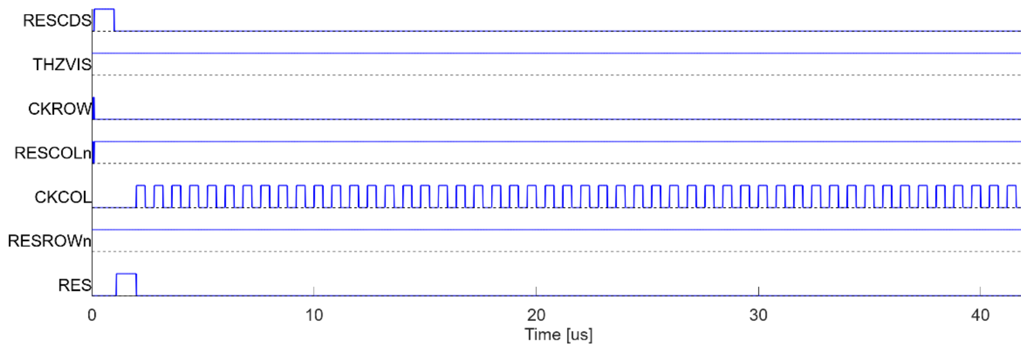


Figure 5.6. RowVis: analog stream-out of the 50 VIS pixels of the selected row.

Eventually, the VIS integration and readout can take place. The reset of the visible pixels is actually performed in a rolling way, therefore at this point in time the integration is already including the time of the THz frame. With a programmable number of repetitions of the *Integrate* waveform (that just keeps the signals in their rest state), it is possible to increase the integration time up to the desired value: in this example, 100μs of extra time is added. VIS

readout is performed similarly to THz, starting with a reset of the decoders with *THZVIS*=1, and then reading out each row, for a total of 50 times. Using waveform *RowVIS*, firstly the column amplifier is operated for CDS operation, that concludes with the pixel reset, and then the analog value of all 50 pixels in the row are streamed out. The row time amounts to 42μs, for an overall VIS readout time of 1μs plus 50×42μs, totaling 2.1ms. The resulting VIS+THz frame lasts then ~10.25ms, or in other words the multispectral imager achieves a 97.5Hz frame rate. Due to the rolling shutter operation, the VIS integration time amounts exactly to the frame time (less the negligible reset time). Whenever a shorter exposure may be needed, the VIS frame integration can be done sequentially with the THz frame rather than in parallel.

The typical sensor timings are summarized in Table 5-2.

Table 5-2. Typical timing of the multispectral image sensor

Parameter	Value
THz integration time	8mS
VIS integration time	10.25mS
Frame rate	97.5Hz
Source modulation	500Hz
THz readout time	150μs
VIS readout time	2.1ms

5.1.4 Optimization of the THz channel operation

There are many parameters that, although fixed in simulation, have to be checked and optimized in order to guarantee a proper operation of the terahertz channel, even more with the modified operation with cyclic resets:

- DAC reference voltages
- Periodicity of cyclic resets
- Chopping frequency
- Dummy and active gate voltages

In this phase it is necessary to produce an approximately uniform THz power distribution in an area as large as the sensor array: this allows evaluating all pixels simultaneously in very similar conditions. In order to do so, it is necessary to tune the lens distance from the source and use the very same (unoptimized) sensor array to evaluate the beam shape. It is not important to know the exact impinging power but only to have reproducible and fairly constant conditions all over the array.

Therefore, the setup of Figure 5.1 has been adapted to work in such conditions, with a 335GHz source frequency which resulted to give the higher response, and a source-lens-detector configuration that allowed a spot at the detector covering almost all the array. In order to produce cleaner output data even with very weak signal, an additional modulation is implemented by using the source UCA and performing an external subtraction, repeating the cycle of Table 5-1. The scheme is illustrated in Figure 5.7: N_{UCA} frames are acquired with UCA off (signal not attenuated) and UCA on (maximum attenuation), averaged and then subtracted to obtain the net frame, thus removing the fixed pattern due to any mismatches across the pixel array. After this, in order to improve the quality of the acquisition, N_{Cycles} net frames are averaged. To be noted that the temporal noise data is extracted from the single original THz frames running at 100Hz, in order to evaluate the real noise in the nominal operating conditions. With $N_{UCA}=10$ and $N_{Cycles}=20$, overall $N_{Cycles}x(N_{UCA}+N_{UCA})$=400 frames are needed, that thanks to the high readout speed are acquired in just 4 seconds. These conditions are used in all the characterizations presented in this section.

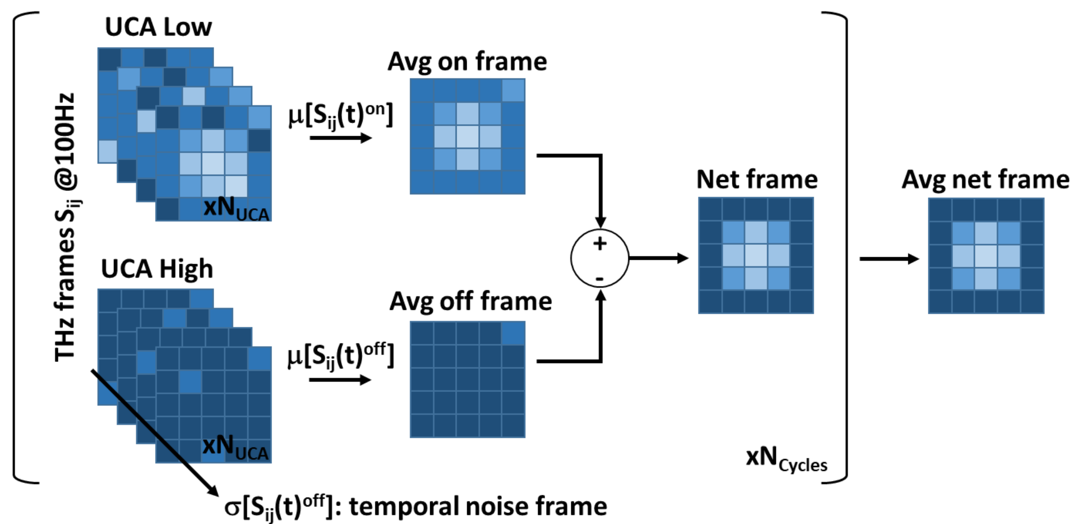


Figure 5.7. Scheme of the statistics acquisition with the additional UCA modulation.

Since a uniform power density is almost impossible to achieve, an upfront characterization of the beam has been made. Figure 5.8 shows the average net image of the beam, with the amplitude expressed in digital numbers (DN), being the channel a direct analog-to-digital converter. This image is used to define the *valid pixels* that receive enough signal and mask the weaker ones that would lead to a very noisy statistics, by means of a simple threshold.

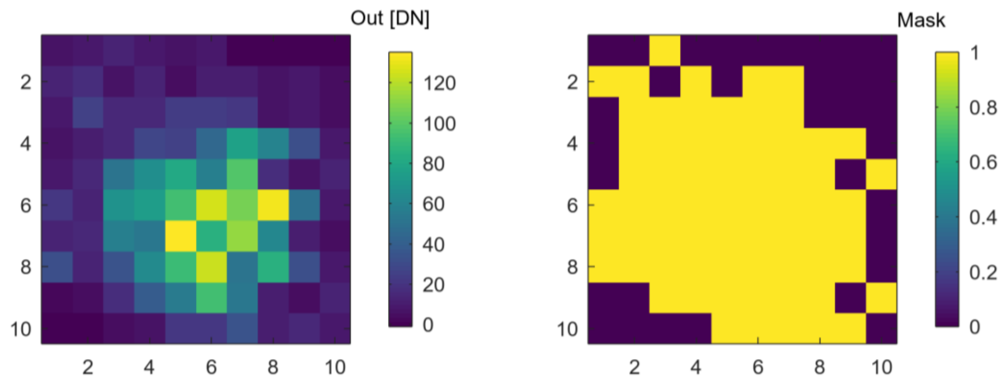


Figure 5.8. Image of the acquired THz beam with the terahertz imager (left) and mask applied to subsequent measurements in order to discard pixels with very low signal (right).

Then, for each parameter sweep, 4 main outputs are observed. These are required to monitor the behavior of the pixels, and in particular:

- The mean value of the valid pixels: used as an indication of the strength of the received and converted signal
- The signal-to-noise ratio: beside the absolute value of signal and noise, their ratio primarily define the quality of the output image
- The relative fixed-pattern noise: as indication of the FPN, the standard deviation of the pixels values over their mean is calculated so to notice the change of non-uniformity
- The number of good pixels: in order to recognize pixels that stop working, a threshold is used to discard pixels that give values below the noise

Unless otherwise specified, the following measurements are taken with $f_{src}=335GHz$, $V_{refn}=40mV$, $V_{refp}=68mV$, and $V_G=V_{GD}=0.35V$. These values were chosen both from the design knowledge and after few qualitative trials as a starting point, and are subject to the optimization hereafter.

DAC reference voltages. The DAC reference voltages, V_{refn} and V_{refp}, are involved in the gain of the incremental ADC: although it is known that lower $\Delta V_{ref}=V_{refp}-V_{refn}$ brings to higher gain as described in eq.(4.4), it is important to track what happens to noise and non-uniformity. In particular higher gain tends to increase non-uniformity and brings to saturated pixels, while lower gain can lead to worse SNR. Moreover, together with ΔV_{ref} also variations of its baseline value, V_{refn}, are evaluated: the differential nature of the circuits should be anyway resistant to these common mode changes.

The results are plotted in Figure 5.9, where the inverse relationship of ΔV_{ref} with respect to the gain is clear. As expected, the relative FPN increases towards the high end values, while the SNR decreases for ΔV_{ref}>60mV. Overall, the best value seems to lie within the 30-60mV range, while there is no relevant tradeoff for the baseline value, which can be freely chosen.

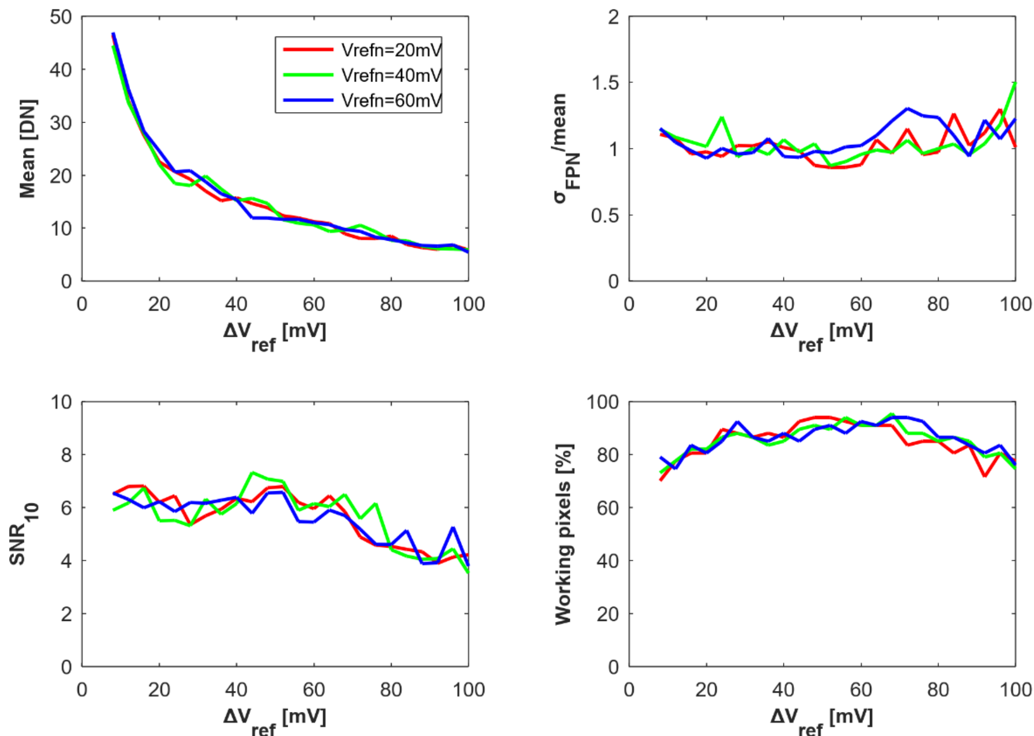


Figure 5.9. Signal, fixed-pattern noise, signal-to-noise ratio, and estimate of working pixels vs. differential DAC reference voltage ΔV_{ref}, at different common mode values.

Periodicity of cyclic resets. The periodic reset of the integrator, implemented to recover the common mode and to avoid saturation, could corrupt the incremental converter operation. For this reason, in this measurement its impact has been evaluated by changing the interval between resets. The period of the reset has been set to 20μs, 40μs, and 80μs. Moreover a measurement without reset has been also evaluated.

From Figure 5.10 it is clear that, while the signal amplitude is not affected, there is a relevant change in the SNR: shorter periods are favoured (20μs). It is worth noting that the sensor continues to work even without the cyclic resets, but at the expense of both a higher noise and response non-uniformity.

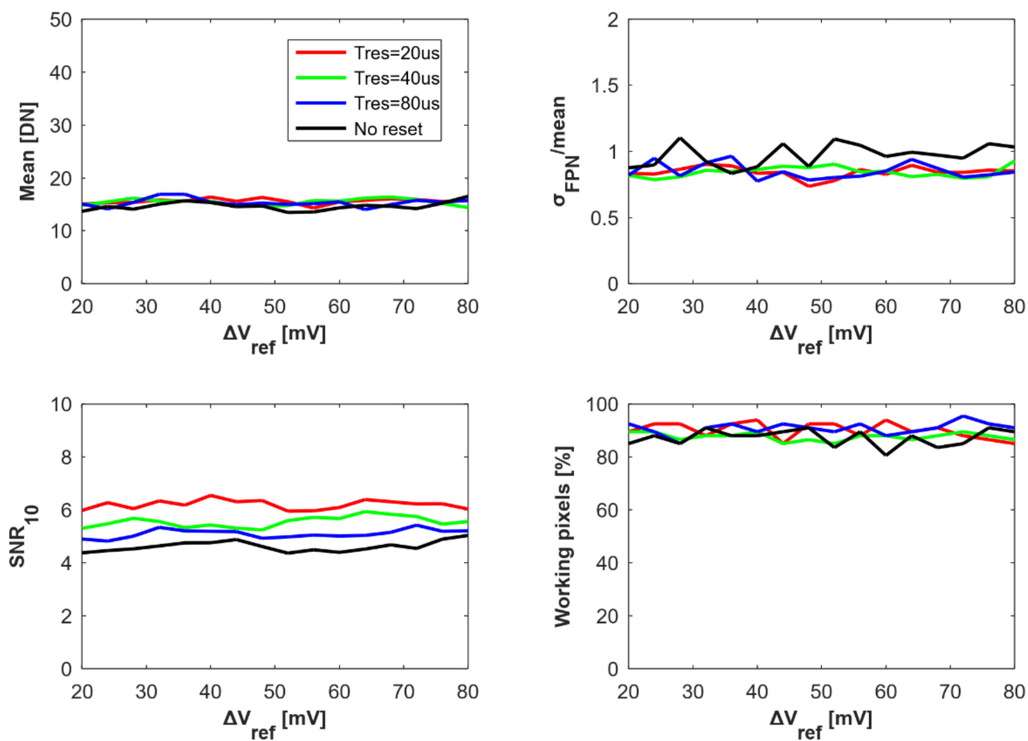


Figure 5.10. Signal, fixed-pattern noise, signal-to-noise ratio, and estimate of working pixels vs. differential DAC reference voltage ΔV_{ref}, at different periodicity of the integrator reset.

Chopping frequency. The nominal chopping frequency was set to 100kHz by design. In this measurement, it has been set to 25kHz, 50kHz, 100kHz, 200kHz, and 500kHz. The swept parameter in this case is the detector gate voltage.

Measurements of Figure 5.11 indicate that higher chopping frequencies exhibit a signal drop: this is the effect of the reduced input impedance of a chopper amplifier [Xu2013] in conjunction with the detector output impedance (loading effect as described in paragraph 3.2.3). This is demonstrated by the fact that this difference vanishes with large bias, i.e. low channel resistance.

It can be seen that up to 100kHz the signal and SNR are preserved, and therefore the design choice can be confirmed.

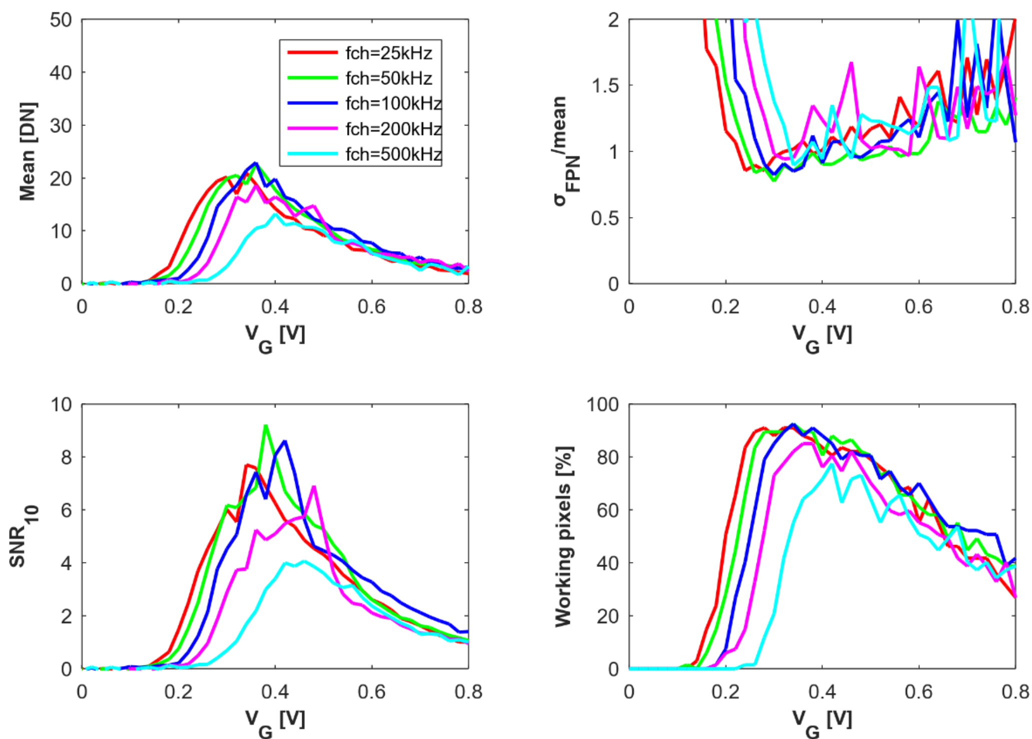


Figure 5.11. Signal, fixed-pattern noise, signal-to-noise ratio, and estimate of working pixels vs. detector bias V_G, at different chopping frequencies.

Dummy and active gate voltages. The high non uniformity and strong drop of working pixels of the previous measurement for low gate bias is due to the mismatch between active and dummy detectors. Indeed, when biased very near to the threshold voltage, small mismatches can determine a large drain-source resistance difference: therefore the differential input of the converter results strongly unbalanced.

To investigate this issue, the active and dummy detectors gate voltages can be independently set. The measurement of Figure 5.12 shows the results in different conditions.

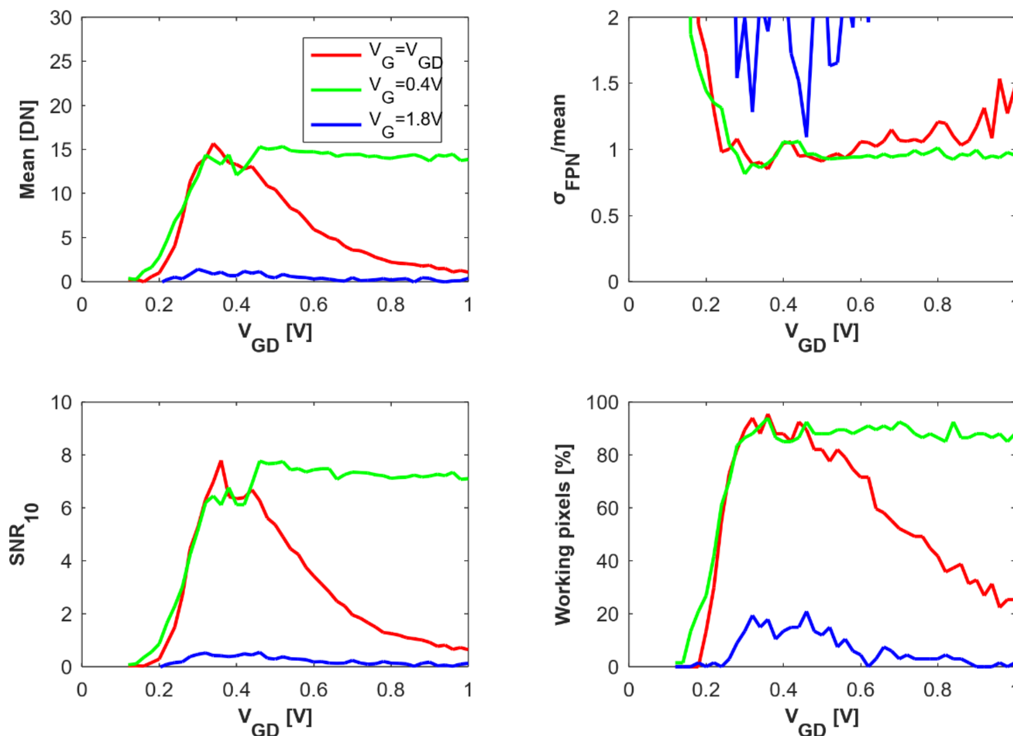


Figure 5.12. Signal, fixed-pattern noise, signal-to-noise ratio, and estimate of working pixels vs. dummy detector bias V_{GD}, at different detector bias V_G. (same, optimal point at 0.4V, attenuated)

As a reference, one measurement sweeps both voltages simultaneously (red curve), highlighting the known behavior as shown in Chapter 3. The second measurement (green curve) sweeps only the dummy voltage, with the active detector constantly biased at 0.4V: in this condition, the active detector is working near it maximum responsivity value, while the dummy detector varies its output resistance. Interestingly, two things can be noted:

- there is a signal drop when $V_G \approx V_{GD}$: this is the effect of the mismatch that causes a strong unbalance of the detector output impedance. The detectors are still producing a signal, but some of the active-dummy pair have a high mismatch and the converter saturates. This reflects also in a higher pattern noise and lower number of valid pixels;

- the resulting unbalance between the inputs is not relevant for dummy gate bias beyond the threshold voltage, for both signal and SNR. In this region all indicators are behaving correctly.

This measurement shows that, even if a setting V_G=V_{GD} can bring to the optimum SNR, the same condition can be more easily achieved by setting V_{GD} to a slightly higher value, thus making the mismatch effects negligible. As the dummy detector is expected to contribute to noise too, setting a high V_{GD} can be beneficial in decreasing its noise contribution: however, currently this cannot be observed because the noise seems dominated by the channel contribution. A last sweep with the active transistor biased to have substantially negligible responsivity (large gate bias), shows a residual detection that can be accounted to the dummy FET: surprisingly, this contribution has the same sign as the active FET. The motivation is currently unknown, however it is not detrimental for the detection.

5.2 IMAGING CHARACTERIZATION

5.2.1 THz imaging characterization: linearity, responsivity and noise

The chosen operating conditions for the THz channel characterization, based on previous measurements, are $f_{src}=335GHz$, $V_{refn}=60mV$, $V_{refp}=92mV$ ($\Delta V_{ref}=32mV$), $f_{ch}=100kHz$ and $V_G=V_{GD}=0.36V$. In the measurements of responsivity and noise, it is important to integrate the whole THz beam: therefore, the mask of Figure 5.8 is not anymore considered, and all pixels participate to the evaluation of the signal.

Thanks to the source capability of progressively attenuating the signal (UCA), it is possible to make an evaluation of the channel linearity. In the scheme of Figure 5.7 it is possible to set the UCA voltage to a range between 0V-5V during the acquisition of the “on frame”, and to correlate the output with the expected variation of impinging power given by the source specifications.

Figure 5.13 plots the result of the UCA voltage sweep superimposed with the normalized power variation of the source, and then correlates this power to the output of the channel. In order to observe how pixels having a different input power behave, the plot is shown for 100%, 68%, 31% of pixels having the largest output.

It is possible to see that, except discrepancies due to the noisy measurement, the linearity is good. It can be noticed that there is a small nonlinearity (like a “dead zone”) of small input power levels that does not give output. One hypothesis is that this is caused by the resets of the integrator that partially cancel the integrator residual voltage every 20μs: a minimum power level is needed for the integrator voltage to overtake the LSB level.

Due to the relatively low power emitted by the available source, it was not possible to evaluate the linearity for very large signals, and therefore to evaluate the overall maximum dynamic range of the imager.

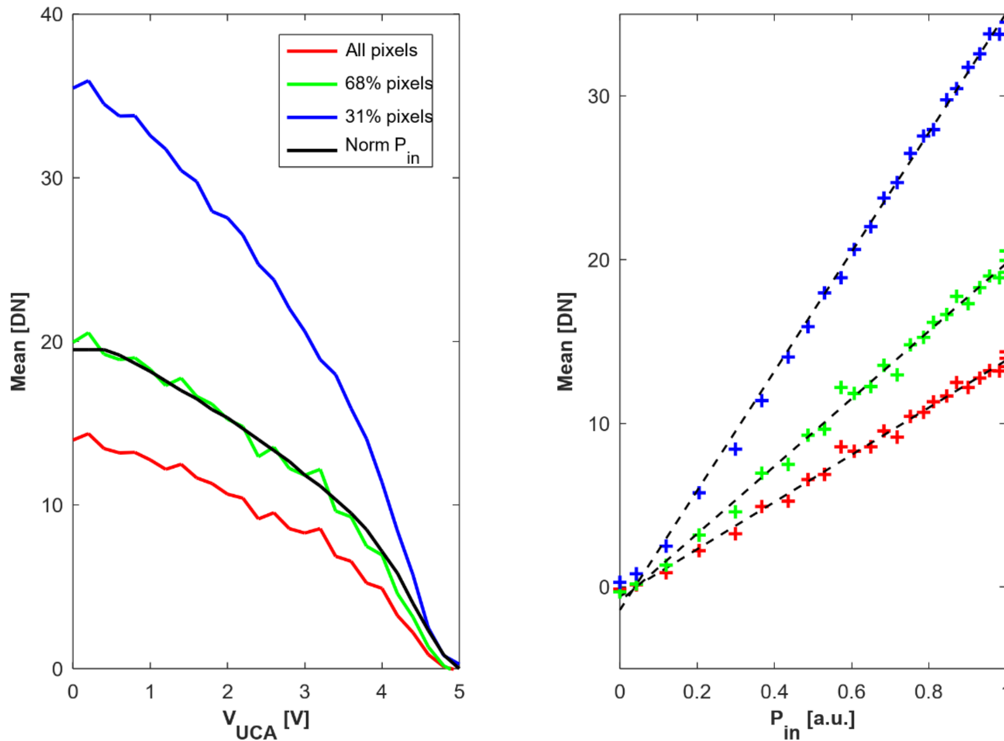


Figure 5.13. Imager output with the user-controlled attenuation (UCA) of the source (left, sensor response in red, green, blue, and normalized nominal attenuation in black) and sensor linearity evaluation (right)

For a precise numerical evaluation of the responsivity and NEP it is necessary to calibrate correctly the impinging power on the detector [Ali2016]. Figure 5.14 shows the characterization of the total power reaching the focal plane. The impinging power has been obtained with a pyroelectric reference detector in the same setup, as shown in Figure 5.1. The pyroelectric detector requires slower modulation frequencies: for this specific measurement, the beam has therefore been modulated at 50Hz. From the device specifications, at this modulation and at a source frequency of 250-350GHz, the responsivity is 300V/W. The pyroelectric detector therefore measured a maximum power of 343μW at the focal plane.

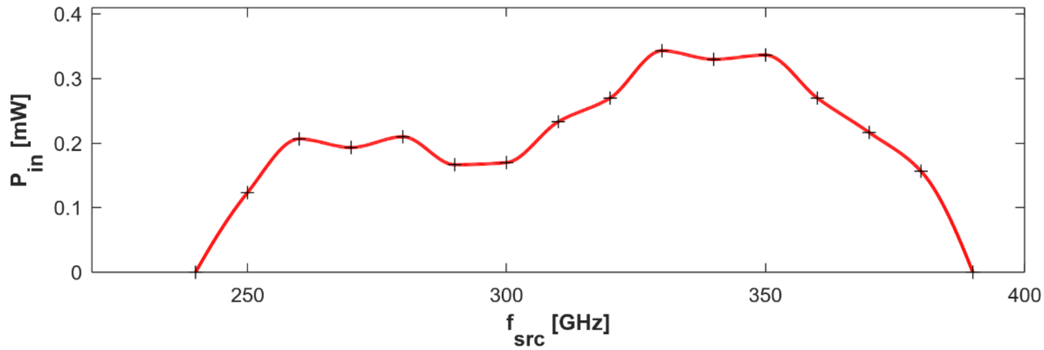


Figure 5.14. Measured power impinging onto the focal plane by using a pyroelectric detector

The imager, being hosted in a PCB with several metallic parts perpendicular to the beam, exhibits strong oscillations in the response due to reflections. In order to properly evaluate the responsivity, it is necessary to filter out these oscillations to avoid over/underestimation. In this measurement, it has been found that the periodicity of these ocillations is ~7 samples at 0.1GHz, so a moving average of length equal to 7 will be applied. This periodicity corresponds to a ~21cm cavity: indeed, it is compatible with the length of the setup. The measured average frame is then summed up across pixels to integrate the beam, and divided by the calibrated incident power, yielding the responsivity R_V, and then the output noise is referred to the input yelding the *NEP*.

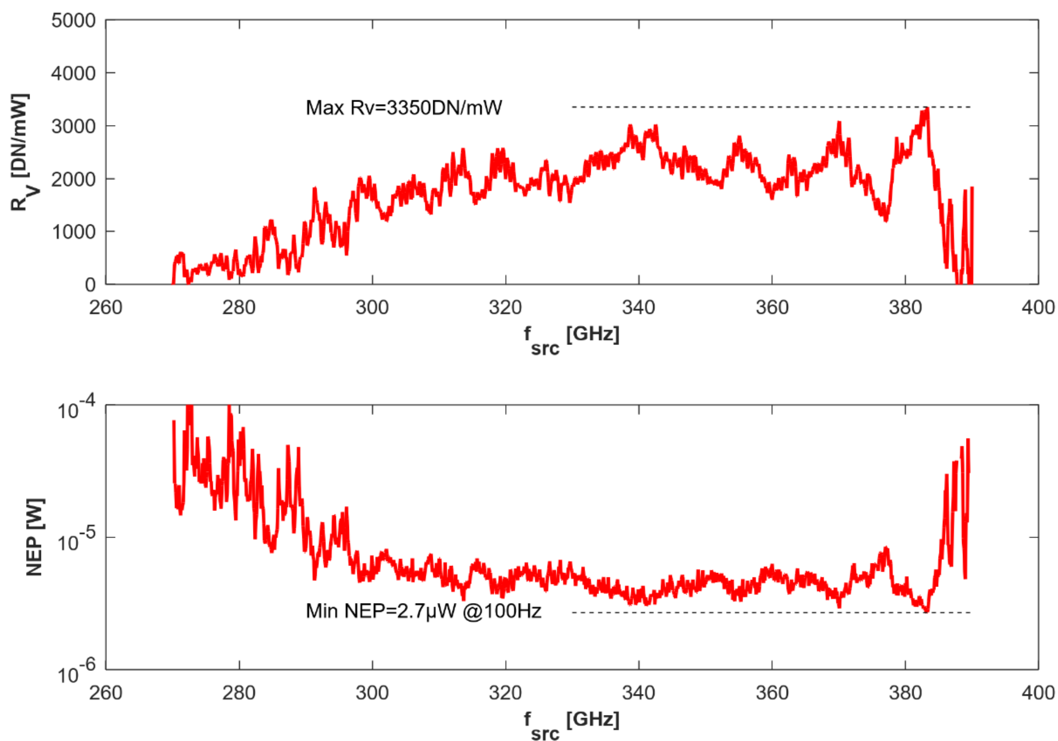


Figure 5.15. Voltage responsivity R_V and integrated NEP of the image sensor vs. source frequency, at 100Hz frame rate and best biasing conditions (V_G=0.36V).

Figure 5.15 shows responsivity and noise equivalent power in function of the frequency: a maximum responsivity is obtained at ~380GHz, as similarly achieved in [Perenzoni2016] where the same antenna has been used.

The best performance is R_V=3350DN/mW and integrated NEP=2.7μW at 384GHz, that at ~100Hz frame rate corresponds to a spectral NEP=270nW/$\sqrt{Hz}$.

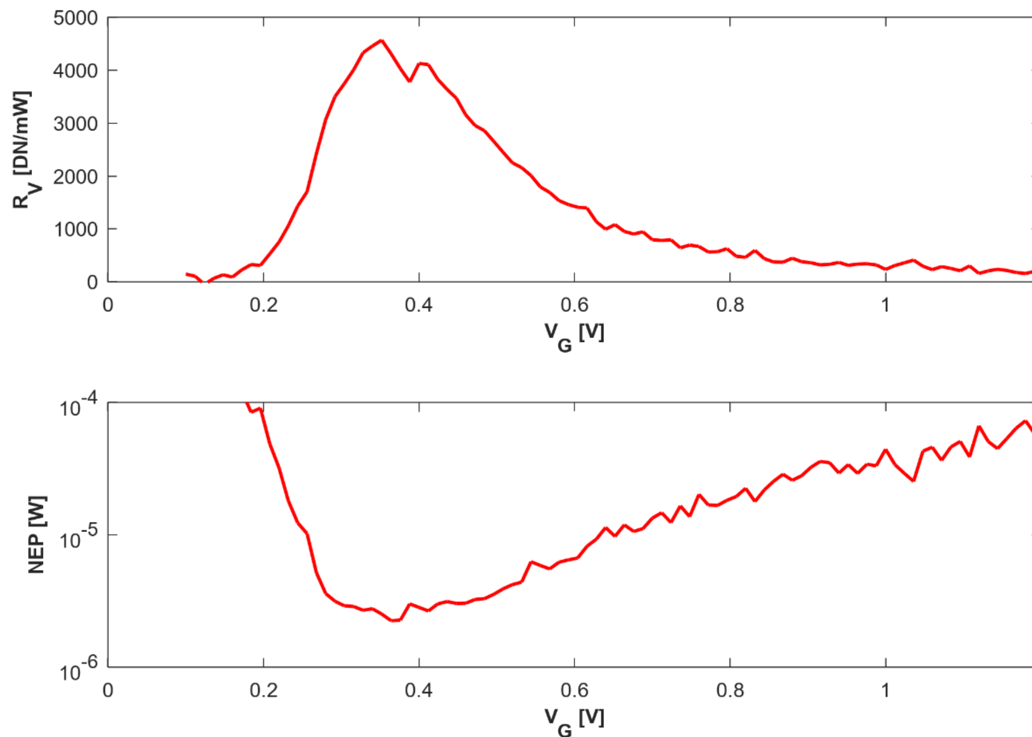


Figure 5.16. Voltage responsivity R_V and integrated NEP of the image sensor vs. detector bias V_G, at 100Hz frame rate and f_{src}=335GHz.

The detector bias sweep of Figure 5.16 has been performed at the point with the maximum signal, at f_{SRC}=335GHz, where a constructive reflection brings the response beyond the spectrally averaged value. With this measurement it is possible to confirm that the best operating region for the gate bias is in the interval V_G=0.35÷0.45V.

5.2.2 VIS imaging characterization

It is expected that the visible imager is affected by a large non-uniformity due the different boundary conditions that the pixels experience, and moreover some pixels will also show reduced or very low response due to the shading of the antenna arms.

A characterization of the non-uniformity has been performed by measuring a uniform image (it is sufficient not to use any optics and to avoid shading on the image sensor) in the dark and in the light, as shown in Figure 5.17.

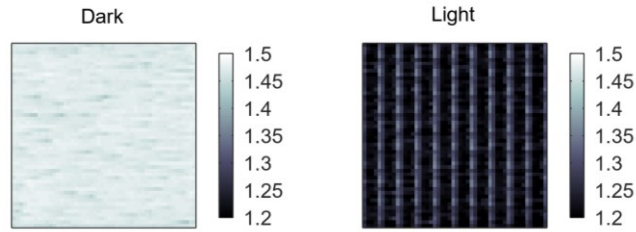


Figure 5.17. Characterization of fixed pattern noise (left) and photoresponse non-uniformity (right).

While on the dark a random pattern is present due to the residual differences not canceled by the channel amplifier, in the bright image it is possible to see how several shaded pixels do not decrease in voltage. The dark value is 1.487V, while the saturation level is 1.062V.

In order to recover the image quality, some processing is needed. While the residual FPN can be easily reduced by subtracting a previously acquired dark image, the photoresponse non-uniformity (PRNU) typically requires a characterization calculating a coefficient for each pixel.

In this case, however, it is possible to notice in Figure 5.17 that the PRNU repeats with a 5x5 kernel, that is indeed the unitary repetition pattern of the VIS pixels inside a THz pixel.

Table 5-3. Octave code for on-the-fly calculation of gain correction factors.

```
function dataGain = extractGain(dataImg)
                                                    // Define 5x5-pixel gain kernel
   gKernel=zeros(5,5);
   for x=1:10
     for y=1:10
       cx=(x-1)*5+1;cy=(y-1)*5+1;
       gKernel +=dataImg(cy:cy+4,cx:cx+4);          // Accumulate all 100 sub-blocks
     endfor
   endfor
   gKernel = gKernel./100;                          // Obtain average sub-block

   dataGain=zeros(50,50);                           // Define 50x50-pixel gain factors
   for x=1:10
     for y=1:10
         cx=(x-1)*5+1;cy=(y-1)*5+1;
        dataGain(cy:cy+4,cx:cx+4)= gKernel;         // Tile kernels together
      endfor
    endfor
  dataGain=dataGain./mean(mean(dataGain));          // Normalize gain factors

endfunction

…
…

gain=extractGain(dark-data);                        // Extract gain from dark image and data
img=(dark-data)./gain;                              // Apply FPN and PRNU correction

…
…
```

As a complete image has 100 sub-blocks that typically experience different illumination conditions, it is enough to build a statistics on the fly in order to reconstruct the kernel and correct the image. This calculation can be based on the very same data, without characterization, as implemented in the Octave script shown in Table 5-3. Additionally, some residual noise can be smoothed by a blur filter. The results of an image taken by using a single lens of a discrete transistor is shown in Figure 5.18.

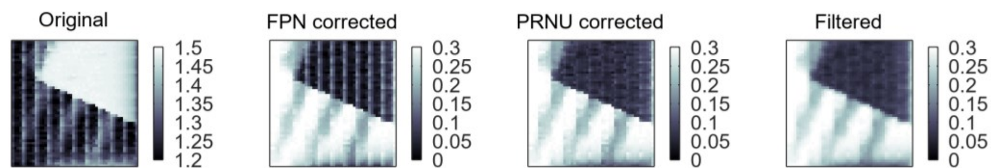


Figure 5.18. Image quality recovery by FPN correction, PRNU correction, and smoothing filter.

5.2.3 Summary of the characterization results

Overall, the performance of the VIS imager is satisfactory: strong non-uniformity was expected but, thanks to a tailored post-processing, the image quality can be recovered up to an acceptable level. On the other hand, the outcome of the THz imager characterization is below the expectations. Therefore, a specific discussion and some considerations are needed.

The measurements result in terms of spectral NEP is representative of both the detector and channel noise, but also of the overall response. By comparing the obtained *NEP=270nW/√Hz* with the results obtained for the same detector in [Perenzoni2016] that achieves *NEP=278pW/√Hz*, there is a huge difference: a 10^3 factor.

Where does this difference come from? This could be due to lower response, higher noise, or both; moreover, the worse performance can be caused by either the antenna coupled detectors, or the readout channel.

In order to understand where is the discrepancy, it is possible to calculate the expected signal. Substituting the current conditions in eq.(4.4) the ADC gain results $G_{ADC}=1.42DN/\mu V$ while for the detector a responsivity $R_{VFET}=200V/W$ is expected. The overall responsivity should then amount to $1.42DN/\mu V \cdot 200V/W=284000DN/mW$ instead of $3350DN/mW$: therefore, the response is 85× lower than expected. In this chip, unfortunately it is not possible to evaluate separately the contributions (i.e. the effective ADC gain and the effective detector responsivity), but some hypothesis can be made:

- The array arrangement of the pixels is surely different from the single pixels tested in [Perenzoni2016], for example for what concerns the interaction between pixels (e.g. crosstalk). Moreover, while in the referenced paper the antenna effective area has been used of 0.198mm^2, in the array the whole beam power is considered, therefore

implicitly the pixel area is $(456\mu m)^2$=0.207mm^2. Together with pixel crosstalk, this can cause a decrease of R_V in the order of some percent;

- The antenna-coupled detector may have decreased its responsivity due to both the presence of the apertures in the ground plane for the visible pixels, and to the proximity of the incremental ADC electronics (indeed the area dedicated to the antenna is rectangular, see Figure 4.10). These factors may have further lowered the aperture and radiation efficiency of the antenna of ~10-20%;
- The electrical connection of the detector with the channel may be affected by the dynamic impedance of the chopper, as it is visible in the measurement of Figure 5.11. This effect is expected to contribute to a very small decrease in response, if present;
- The incremental ADC gain, although it cannot be verified, it is expected to be reliably represented by eq.(4.4). However, it is not possible to completely predict how the mismatches are impacting on the ADC gain.

None of the identified causes seems to contribute predominantly to the 85× lower responsivity, although many of these are effectively present. In order to get further insight on this unexpected lower responsivity, it would have been necessary to include more testing points in the signal chain. Further investigations are necessary in the future.

However, a remaining portion of $10^3/85\approx 11\times$ should come from the other contributor of the NEP, i.e. the noise: in particular, with the hypothesis that the FET noise is known, there should be a relevant contribution from the readout chain. All measurements involving a gate bias sweep have been plotted together in the scatterplot of Figure 5.19, where it can be immediately noticed that there are two regions: one is determined by the FET noise at low gate bias (high channel resistance) and the remaining part is the $\Sigma\Delta$ incremental converter noise. By using the eqs.(3.7) and (3.15) the FET contribution (active + dummy) can be calculated, and converted in digital numbers by $G_{ADC}=1.42DN/\mu V$ from eq.(4.4). It has been plotted and also added in quadrature to the measured ADC noise, matching extremely well the measurement.

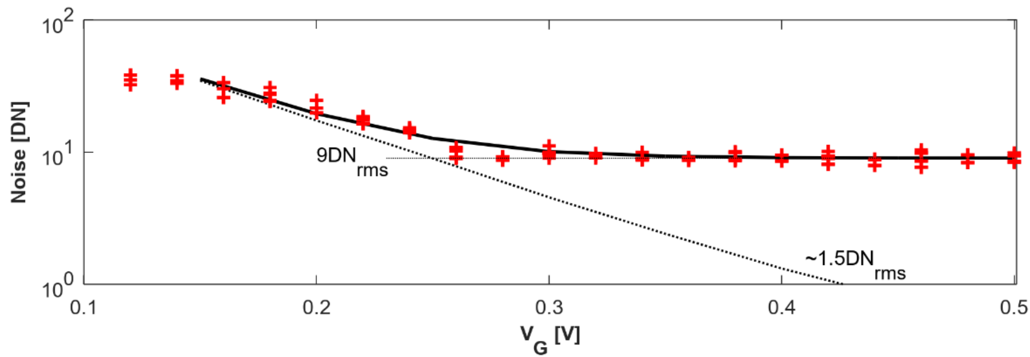


Figure 5.19. Output noise behavior in function of the gate bias, with superimposed the ADC constant measured noise of 9DN_{rms} and the expected FET (dummy+active) noise: their sum is the solid black line.

This analysis shows that the noise of the ADC is too high to properly preserve the detector intrinsic performance, and at the same time it confirms the reliability of the calculated ADC gain. The input-referred noise of the pixel results $9DN/1.42DN/\mu V=6.34\mu V_{rms}$ at 100Hz frame rate and should be $\sim 1\mu V_{rms}$ ($1.5DN_{rms}$) to match the detector at 0.4V bias. The previous version of the channel [Khatib2017] exhibited $1.3\mu V_{rms}$ of noise: most probably the noise increase is due to the disturbances on the supply lines, voltage references and substrate. It is indeed necessary to consider that in the imager there are 100 $\Sigma\Delta$ converters working together and injecting noise on common signals. Also, the impossibility to operate the pixels without periodic reset plays a role in the noise increase.

Overall, there are two contributions to the lower performance with respect to the standalone detector: *a loss of responsivity of the detector, most probably not accountable to the readout chain, and a higher noise of the incremental converter*.

Nevertheless, the multispectral imager is operating correctly and it is able to capture simultaneous VIS and THz images at 100 frames per second. The terahertz imager provides the capability of detecting 270nW, per pixel, at 1Hz averaged frame rate, that is enough to realize real-time videos with commercially available THz sources, typically producing microWatts or milliWatts of power. The summary of the VIS and THz imager performance is listed in Table 5-4.

Table 5-4. Performance summary of the multispectral THz-VIS imager.

	Parameter	Symbol	Value	Unit
Chip	Technology		150	nm
	Supply voltage	V_{DD}	1.8	V
	Chip area		5×5	mm^2
	Power consumption	P_{DISS}	2.84	mW
	Terahertz pixels		10×10	
	Visible pixels		50×50	
	Frame rate		97.5	Hz
Visible imager	Output voltage range	V_{OUT}	1.062-1.487	V
	Full-scale signal	FS	425	mV
	Fixed pattern noise	FPN	7.3 1.7%	mV %
	Photoresponse nonuniformity	PRNU	20.3	%
	Corrected nonuniformity	$PRNU_{corr}$	5.25	%
Terahertz imager	Readout channel gain	G_{ADC}	1.42*	DN/μV
	Readout channel noise	σ_{ADC}	9	DN_{rms}
	Input referred noise	IRN	0.634	μV/√Hz
	Max responsivity	R_{Vmax}	3350	DN/mW
	Minimum NEP	NEP_{min}	270	nW/√Hz
	Peak response	f_{peak}	384	GHz
	-3dB bandwidth	f_{min}-f_{max}	295-385	GHz
	Optimum bias	V_{Gopt}	0.36	V

*calculated, but confirmed by indirect measurements

5.3 Imaging THz+VIS with the Multispectral Image Sensor

After the detailed characterization of the sensor, it is possible to setup an imaging experiment with the objective to validate the capability of simultaneously acquiring the two wavelengths, THz and VIS, in real-time.

5.3.1 THz+VIS measurement setup

The measurement setup for the multispectral imaging experiment realizes a standard VIS imaging and a transmission THz imaging; it is sketched in Figure 5.20. Two TPX lenses having *f=25mm* and *d=25mm* are placed in the THz beam in order to first collimate it and then focus it on the focal plane. The parallel rays at the target illuminate an area approximately equivalent

to the lens aperture: the power is however not uniform. For the VIS component, only the second lens (towards the sensor) contributes to the imaging.

As in the previous measurement, the source is modulated by DAQ boards and synchronized with the sensor via the *CKMOD* signal, and a second UCA modulation is performed to subtract long-term drifts and fixed pattern noise.

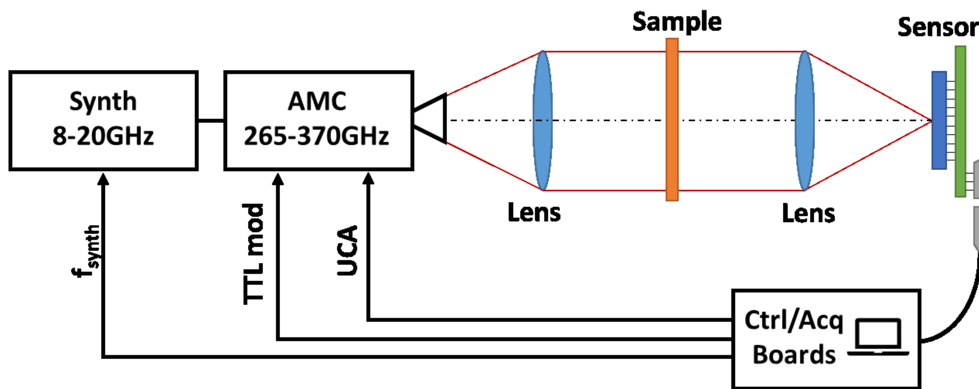


Figure 5.20. Measurement setup for the multispectral THz+VIS imaging experiment.

As target sample, it was decided to exploit the properties of THz to penetrate many dielectrics: the FBK logo was printed on a sheet of paper, and a strip of antistatic film (i.e. conductive) was hidden behind it. In this way, the VIS target is invisible to the THz, and the THz target is invisible to the VIS. The setup and the target are shown in the pictures of Figure 5.21.

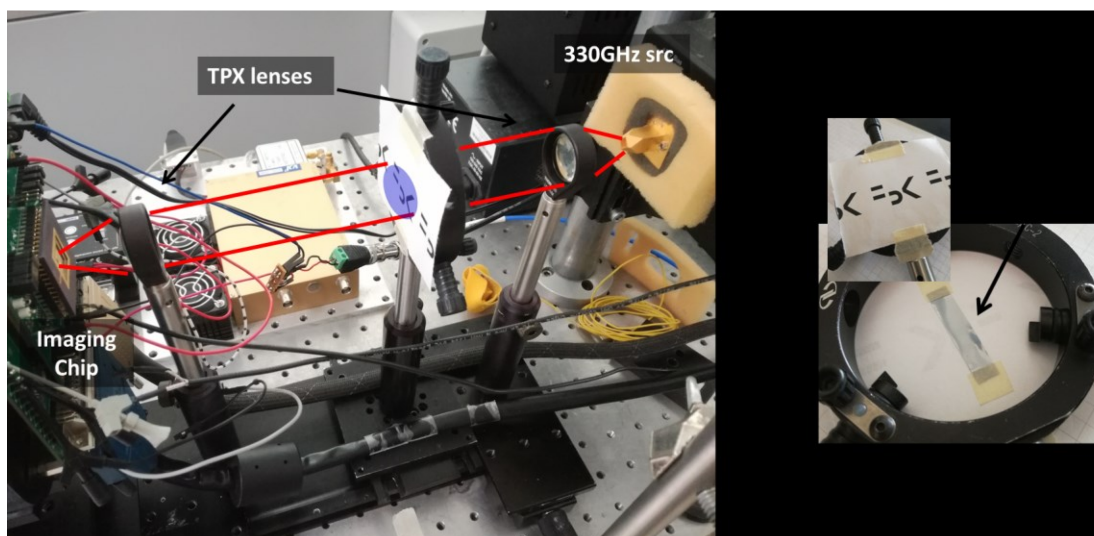


Figure 5.21. Photograph of the setup (left) and of the target (right) for the imaging experiment/

5.3.2 Multispectral imaging

While some postprocessing for the VIS image has been already described in paragraph 5.2.2, there are two corrections that need to be done for what concerns the THz image:

- In this setup multiple reflections are present, and moreover diffraction at the object with a single wavelength causes interference fringes that worsen the quality of the image. For this reason, the source is swept across the range 330-340 GHz and images are averaged;
- Due to the non-uniform beam, it is necessary to characterize the beam itself and use it as an intensity mask to correct the received power. In this way, the final per-pixel information is the attenuation experienced by the THz beam, regardless of the absolute intensity. Moreover, pixels receiving a very small intensity need to be excluded by the computation.

The THz integration time has been increased to $T_{int}=32ms$, due to the smaller intensity expected (sample object attenuation), with $N_{UCA}=10$ and $N_{Cycles}=10$, referring to the acquisition scheme of Figure 5.7. Overall, $N_{Cycles}x(N_{UCA}+N_{UCA})$=200 frames are acquired and averaged for each frequency from 330GHz to 340GHz at 0.5GHz step.

Figure 5.22 shows the measured beam at the various frequencies, exhibiting also a slightly changing shape: this is due to the spurious reflections in the setup that create local maxima or minima. By averaging them, these effects are reduced, and a more uniform measurement can be obtained.

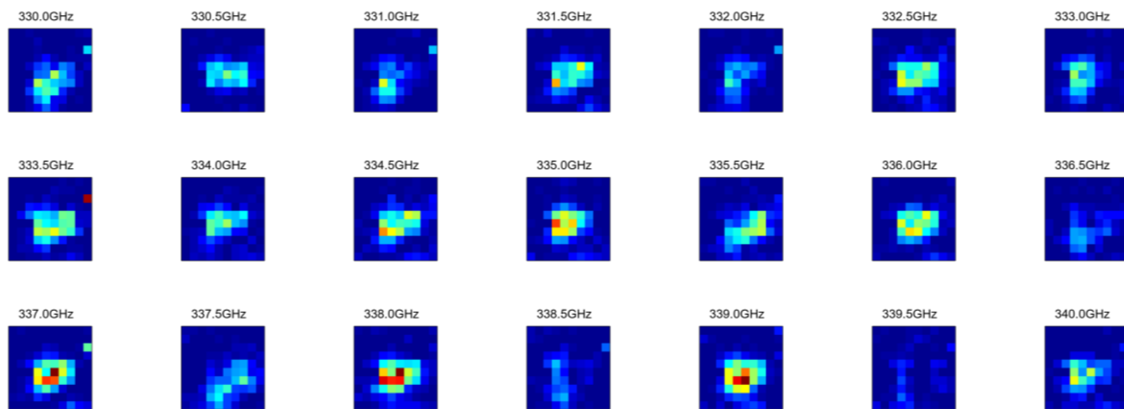


Figure 5.22. Measured THz beam at different frequencies from 330GHz to 340GHz.

The processed measurement results, for different positions of the target, are shown in Figure 5.23. Under the letter "B" of the FBK logo lies the strip of metallic film: it can be noticed that the THz normalized transmission image reveals its position, as also indicated by the profile obtained averaging 5 rows in the middle of the image.

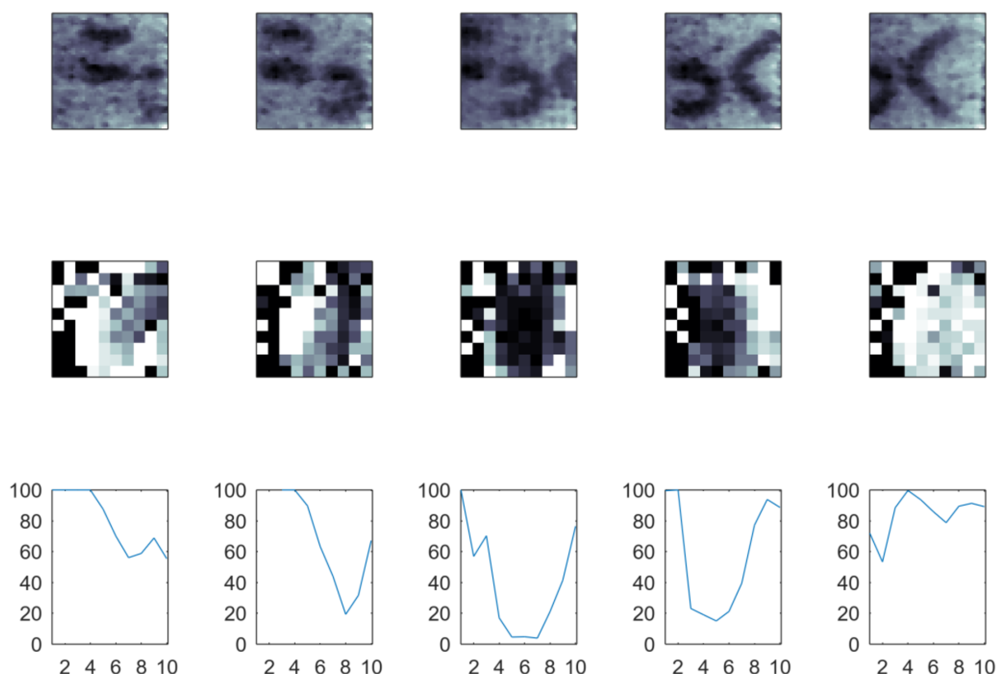


Figure 5.23. Simultaneous visible and terahertz imaging with target sliding from right to left: visible image (top), terahertz transmission (middle), profile of terahertz transmission (bottom).

It can be noticed that the profile if the strip is not very sharp: this is due to the resolving power of the lens. Indeed, it can be calculated that for the used lens, the pixel size is below the diffraction limited spot. At 330-340GHz frequency the wavelength is approximately 1mm, that together with F#=1 of the lens and eq.(4.2) gives $\Delta L = 1.22\lambda F\# \approx 1.22mm \approx 3$ pixels. Indeed, by observing the profile of Figure 5.23 the transition between maximum and minimum transmission takes approximately 3 pixels. In order to obtain a better resolution, a smaller F# would be needed, i.e. larger lens diameter with same focal length.

5.4 Chapter Summary

This chapter distills the main objective and result of the thesis: the realization of *simultaneous and real-time visible and terahertz multispectral imaging with a single CMOS integrated chip*.

During the characterization, several issues emerged: the high non-uniformity of both VIS and THz channels, the need to correct the common mode saturation of the ΣΔ converter, the NEP higher than expected. Nevertheless, none of these aspects were jeopardizing the achievement of the main goal; actually, for some of them it has been possible to find workarounds driving towards more than acceptable solutions.

There are surely aspects that are worth addressing in future improvements of the sensor so as to achieve better performance: noise reduction and signal enhancement, larger pixel count for higher quality images, integrated non-uniformity correction.

Eventually, the results of Figure 5.23 could represent for integrated multispectral imaging what, almost two centuries ago, Figure 1.1 represented for photography: just a starting point for an exciting journey into pictures.

6 INNOVATIVE THZ DETECTORS: THE THZSET AND GRAPHENE

The signal generated by an antenna-coupled FET detector is often very weak and it requires proper amplification to successfully retrieve the carried information. Electronic amplification, as clearly shown in previous chapters, is however complex and noisy: the design has to be done extremely carefully in order to avoid degradation of the overall signal-to-noise, and tradeoffs with power consumption and area have to be done.

If one finds a way to amplify the signal already at the device level, it could be done with minimal or negligible noise. This similarly happens in the photodetectors domain by means of avalanche multiplication devices (avalanche photodiodes, APDs [McIntyre1972], or single-photon avalanche diodes, SPADs [Rochas2003]) which are characterized by an internal gain, greatly increasing the sensitivity. In this chapter the idea of exploiting the avalanche multiplication in a CMOS device by integrating it with the FET detector will be developed.

Furthermore, some details will be given for what concerns the trials to integrate CMOS and graphene FET (GFET) detectors for THz radiation, with the long-term objective to exploit the high graphene mobility to realize resonant high-responsivity sensors.

6.1 THZSET PRINCIPLE OF OPERATION

The basic idea for the novel THz detector is to combine a device with internal gain (avalanche multiplication) with a FET detector. By properly designing the complete device, the current generated by the detection mechanism should be able to inject charges in a region where the internal gain is realized. If this is realized, it is expected to obtain macroscopic signals for infinitesimally small detected signal. The device at the root of this idea is the Single-Electron Bipolar Avalanche Transistor, or SEBAT [Lany2008]. The SEBAT is a peculiar type of bipolar transistor, where the collector-base diode is formed with an avalanche multiplication junction.

6.1.1 The integrated SEBAT

Before talking about the SEBAT device, it is necessary to mention the single-photon avalanche diode, or SPAD, that is a P-N junction specifically engineered to work beyond the breakdown voltage. Typically SPADs are employed to sense single photons, thanks to the fact that – when detected – they generate an avalanche and therefore a macroscopic signal. The SPADs are implemented in commercial CMOS technologies since [Rochas2003] and currently they are also part of mainstream products, for example smartphones. They are carefully designed diodes, with a guard-ring structure that controls the electric field distribution, paired with a so-called “quenching” circuitry that manages the avalanche by reducing the current, thus avoiding the destruction of the device while providing an output voltage pulse.

In a SEBAT, the collector-base junction of a bipolar transistor is replaced by a SPAD, where the purpose is not anymore to achieve single-photon sensitivity but single-electron sensitivity, in particular the charges injected by the base-emitter current. In its first appearance in [Lany2008], it has been shown that this device can be used to measure extremely low currents by “counting electrons” via counting the number of avalanche pulses. In [Webster2012] a SEBAT has been realized in a 90nm CMOS technology, showing its viability also in modern deep-submicron technologies.

Following this idea, the structure shown in Figure 6.1 (cross-section) has been designed in a 150nm CMOS technology, by exploiting a known and working SPAD structure. The avalanche multiplication area is situated between the PW and DNWELL regions; the DNWELL is contacted through an outer ring of N+/NW, and the PW is contacted through P+ diffusion areas. A low-doping zone (lighter and dashed in figure) is used to reduce the electrical field on the borders. As described, the structure would be a SPAD, but with the addition of the N+ emitter region a n-p-n configuration is created where the base-collector diode can be effectively operated in avalanche mode. An additional polysilicon layer is added on top, to avoid the generation of shallow-trench isolation oxide on the surface of the wafer, which presence could induce stress on the silicon lattice thus increasing the intrinsic noise of the device.

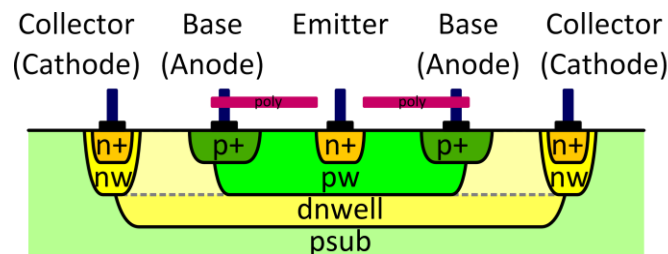


Figure 6.1. Cross-section of the implemented SEBAT in 150nm CMOS technology

The device noise is given by the dark count rate (DCR), that is the average number of avalanches generated by unwanted phenomena such as thermal generation of carriers in the avalanche region or charge tunneling. The DCR is typically proportional to the device area: in avalanche photodetectors, the sensitive area is a fundamental parameter, but in a SEBAT it is possible to design the avalanche region to be as small as possible so to minimize the intrinsic noise.

6.1.2 The THzSET device

The next step is to find a way to inject charges that depend on the THz FET detection mechanism. As demonstrated in the modeling chapter, the FET detector generates a weak negative voltage at its drain, representative of a sinking current: therefore, as depicted in

Figure 6.2, the FET can be connected to the SEBAT emitter to realize what here has been defined as THzSET (terahertz single-electron transistor).

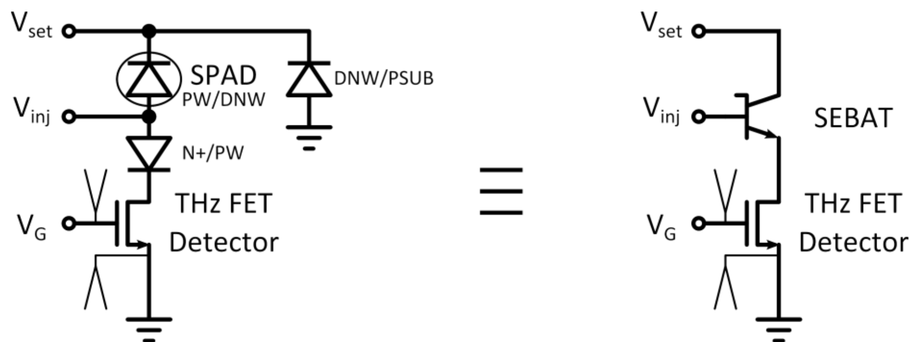


Figure 6.2. THzSET configuration with FET connection and individual junctions highlighted (left) and with the SEBAT symbol indicating the avalanche junction with a short line on the base (right).

With such a device, it is expected to measure the impinging power by simply counting the number of generated avalanches. Referring to Figure 6.2, it will be operated with a fixed injector voltage V_{inj}, setting the SPAD bias together with V_{set} beyond the breakdown. The detection of THz radiation will cause a decrease of the drain voltage, and therefore of the voltage at the cathode of the injector diode N+/PW. This in turn increases the voltage drop across it: the additional charges flowing in the base-emitter portion of the semiconductor will be partly captured by the PW/DNW junction, that will cause the device to enter in avalanche breakdown due to the high bias applied. As for the SPAD devices, it will be necessary to apply some quenching device able to extinguish the avalanche.

As an experimental test structure, it has been realized without additional electronics, therefore giving the possibility to access the terminals corresponding to the collector (V_{set}), the base (V_{inj}) and the FET gate (V_G). The microphotograph of the fabricated structure is shown in Figure 6.3.

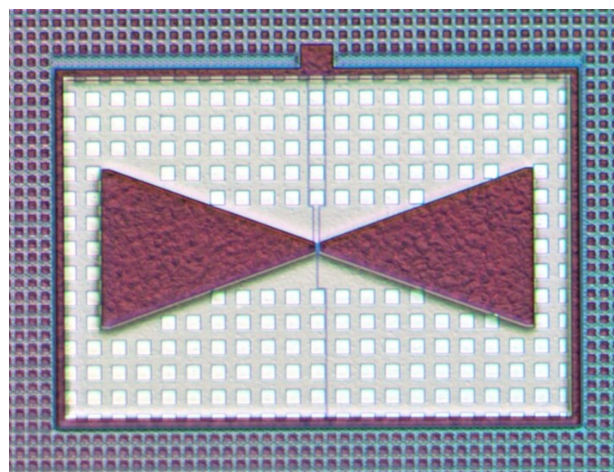


Figure 6.3. Microphotograph of the fabricated test structure including the ~300GHz antenna, the FET detector (in the middle of antenna) and the SEBAT (hidden by the small metal square on the upper side)

6.2 ELECTRICAL AND TERAHERTZ THZSET MEASUREMENTS

The measurement configuration of Figure 6.4 has been conceived in order to perform most of the characterization and acquisitions needed, potentially in an automated way. The device has been connected to a National Instruments analog generation/acquisition board and to a general-purpose motherboard, where several ADCs and DACs can be controlled via LabView™ software.

In particular there are two DACs controlling V_{inj} and V_G, enabling automated voltage sweeps. V_{set} is fixed by an external supply (due to the >20V required for the avalanche junction): its negative terminal on V_{inj} guarantees that the voltage applied to the collector-base diode is not influenced by the injector setting. The four ADCs are used to measure the injected current, the effectively applied voltage V_{set}, and the avalanches:

$$I_{inj} = \frac{ADC2 - ADC1}{1200}$$

$$V_{set} = 22.3 \cdot ADC3 - ADC2$$

For the avalanches' measurement, a 22kΩ resistor is used as a quenching load limiting the avalanche current; at the same time, the avalanche current causes a voltage drop that is capacitively coupled to a resistive divider so to shift the value to a range compatible with the board ADCs. The waveform acquired on ADC0 then requires some processing in order to extract the count rate, that will be described later.

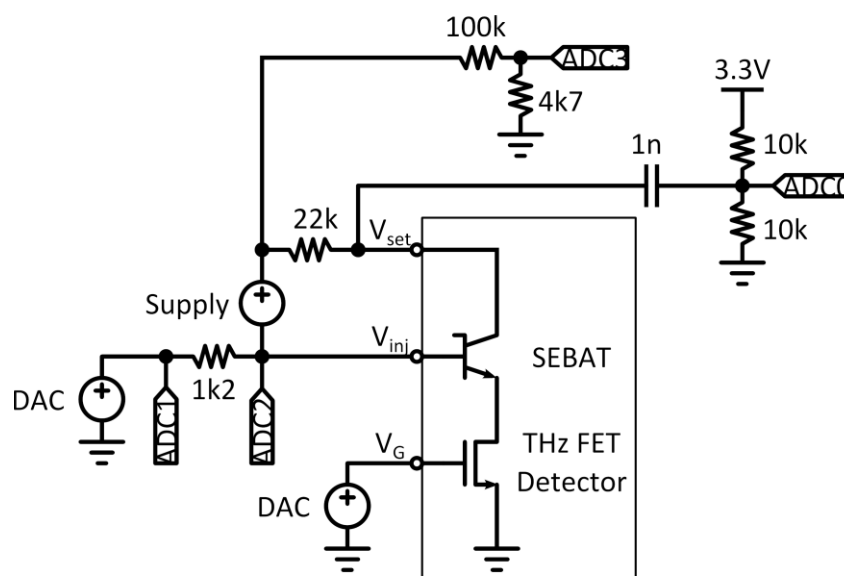


Figure 6.4. General-purpose THzSET measurement configuration.

This configuration has some limitation in terms of maximum count rate: in order to fully exploit it, an integrated quenching circuit would be needed. However, for the purpose of this investigation, the external acquisition and processing is giving satisfying results.

6.2.1 Static electrical characterization of the THzSET device

Since the avalanche operation injects additional pulsed currents that make it impossible to accurately measure and characterize the THzSET device in DC conditions, a first electrical characterization has been performed with V_{set} shorted to V_{inj}, thus nulling the contribution of the avalanche junction.

The values of V_{set} and V_G have been swept in order to extract the IV characteristics of the FET detector in series with the N+/PW diode, so as to check that the device is properly working and to evaluate the current flowing into the injector. Measurements are shown in Figure 6.5.

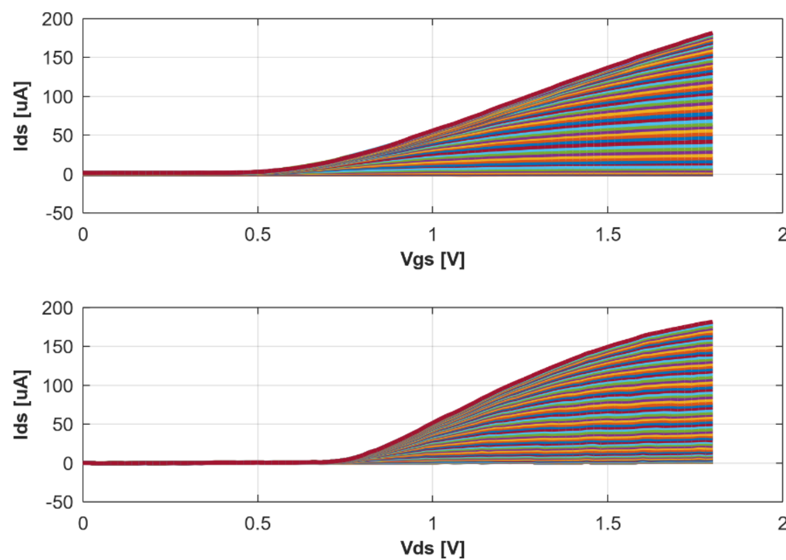


Figure 6.5. Measured IV characteristics of the THzSET structure in static conditions, with $V_{set} = V_{inj}$.

While the known behavior of an FET is visible in the output current vs. V_G, showing a threshold voltage of about 0.4-0.5V as expected by the technology specifications, it can be seen that the series diode shifts the current behavior to the right in the V_{inj} sweep (that is the drain-source voltage plus the diode drop).

6.2.2 Dynamic Electrical Characterization of the THzSET Device

As soon as V_{set} is increased, some of the injected charges into V_{pw} get amplified by the SEBAT, causing a net additional current that brings to a negative measured I_{inj}. In this situation, and in particular at voltages higher than the breakdown voltage of the avalanche junction, the average current value loses meaning, while it makes more sense to count pulses, i.e. to measure the average counts per second of the generated avalanches.

Since there is no front-end circuitry directly connected to the THzSET device and the quenching is relatively slow due to the high capacitance, the chosen approach has been to capture directly the analog voltage and subsequently process the waveform. The analog

waveform, sampled at 200ns rate for 10ms (50ksamples), is differentiated and an adaptive threshold at 20% of the min-max amplitude with a limit of 10mV minimum to avoid noise triggering is used in order to count the crossing points. Figure 6.6(left) shows the algorithm applied to a low frequency, which is a “clean” situation (i.e. the interarrival time of avalanche pulses is large enough that the voltage relaxes up the SEBAT bias). In presence of high frequency, the waveform becomes more “dirty” but the algorithm still works quite well, as shown in Figure 6.6(right): relevant pulses pile-up occurs as visible in the insets. Several trials showed that the processing could retrieve up to a maximum of several hundreds of kHz, depending on the pulses bunching. The acquisition is repeated several times (tens to hundreds) in order to average the obtained values and enlarge the observation time up to some seconds, corresponding to a minimum count rate below the single count per second.

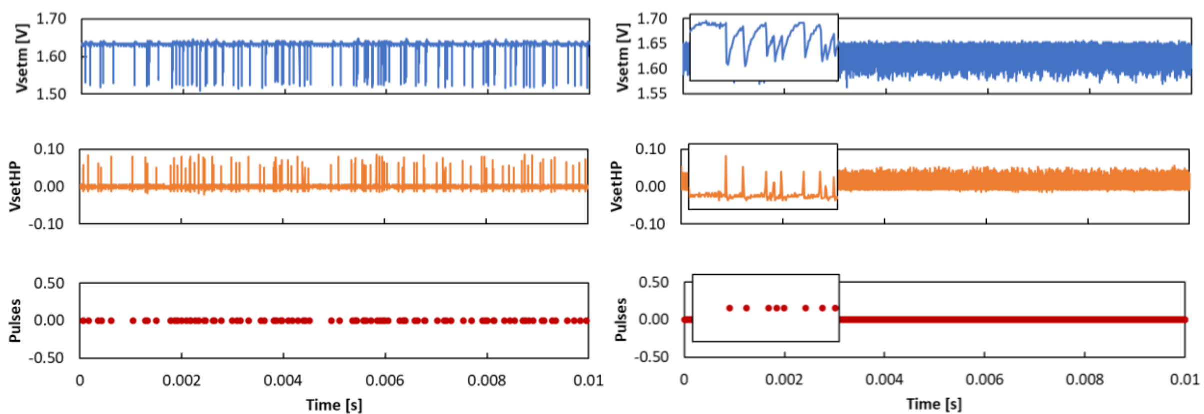


Figure 6.6. Acquisition of counts with a low frequency (left) and high frequency (right), with an inset of 40μs to show the detail of the extracted pulses

A first rough sweep of the bias voltages highlighted some peculiar behavior, characterized by three operating modes clearly distinguishable between them, if observed at the oscilloscope. In order to ensure proper characterization and measurements, some more investigation has been done. Figure 6.7 depicts these modes:

- Mode 1: normal avalanching mode, most probably it can be described with a Poissonian process as in conventional SPADs.
- Mode 2: very jittered oscillation characterized by large pulses, apparently going beyond the SEBAT bias and then relaxing.
- Mode 3: stable oscillation with very small pulses, almost glitches, at relatively high frequency.

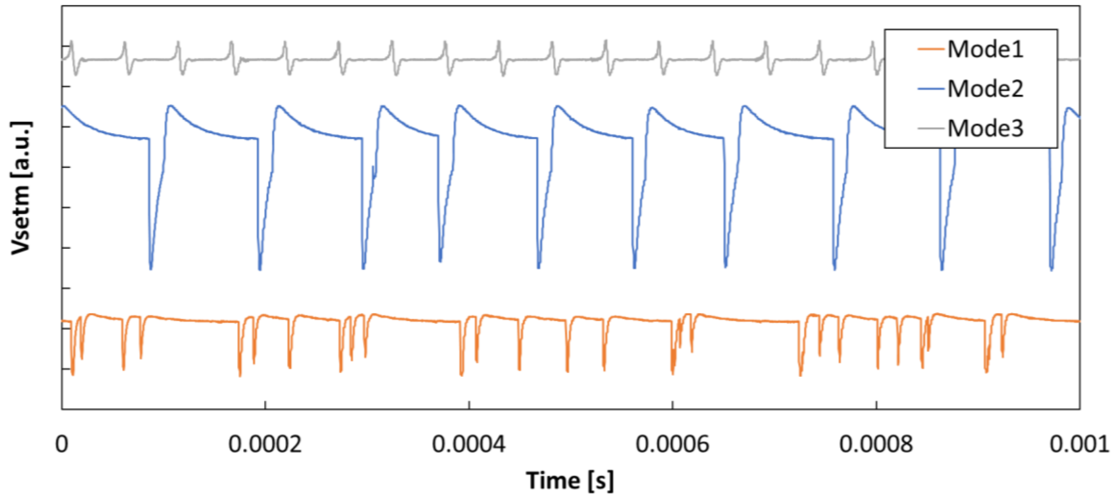


Figure 6.7. Oscilloscope traces (vertical offset added for clarity) of the three operating modes: only mode 1 corresponds to the desired operation.

Modes 2 and 3 are most probably the consequence of the additional parasitics added by the external circuitry and must be excluded from the measurements in order to avoid artifacts. A full sweep has been performed, recording the count frequency and the relative jitter (see Figure 6.8).

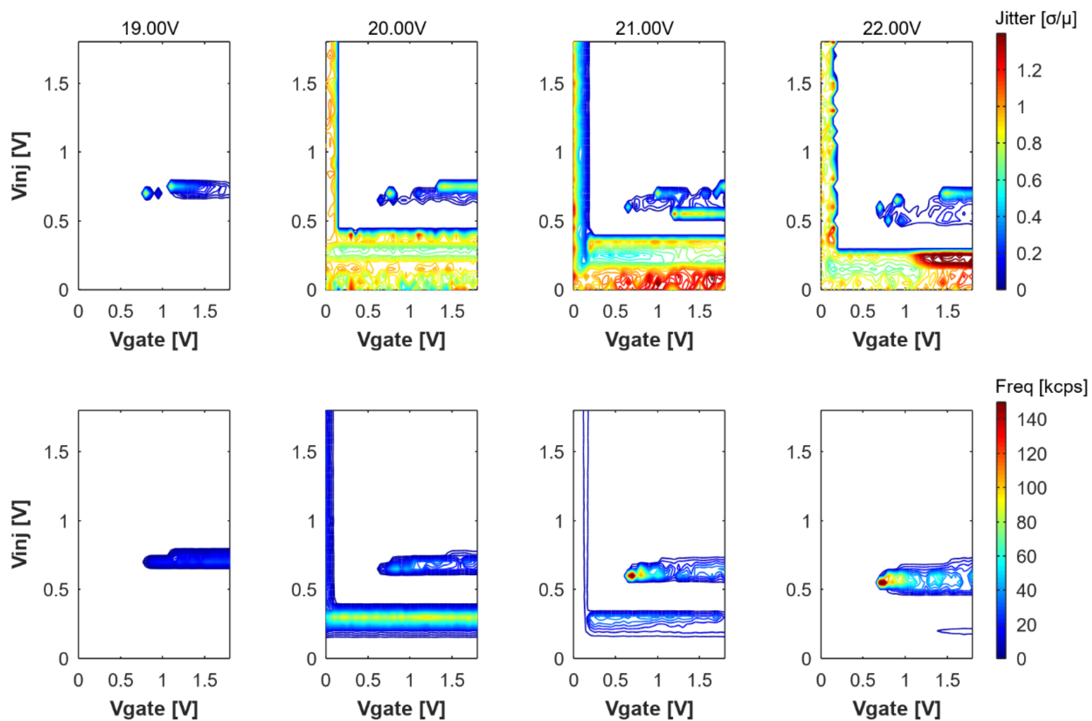


Figure 6.8. Relative jitter and counts per second by varying the various bias: V_{set}, V_{inj}, V_{gate}. It can be seen that the desired behavior is confined around V_{set} = 20V and $V_{inj} \approx 0.3V$

Further investigations are beyond the scope of this work, where the study was limited to understand the different regions in the bias space for the measurement purpose:

- **Mode 1: V_{inj} = 0.0 … 0.5V, V_G = 0.2 … 1.8V**
- Mode 2: V_{inj} = 0.0 … 1.8V, V_G = 0.0 … 0.2V
- Mode 3: V_{inj} = 0.5 … 0.9V, V_G = 0.2 … 1.8V

One interesting behavior that can be observed is related to the negligible influence of the V_G voltage on the count rate, as visible in Figure 6.8, second column corresponding to $V_{set}=20V$, when approximately $V_G>0.2V$.

By setting $V_{inj}=0V$, the base-collector junction can be operated as a conventional SPAD and therefore some parameters can be extracted. The results give an approximate breakdown voltage of $V_{BD}=19.5V$, with a *DCR=600cps* at an excess bias $V_{EX}=2.5V$. Figure 6.9 shows that this behavior holds up to $V_{inj}=50mV$.

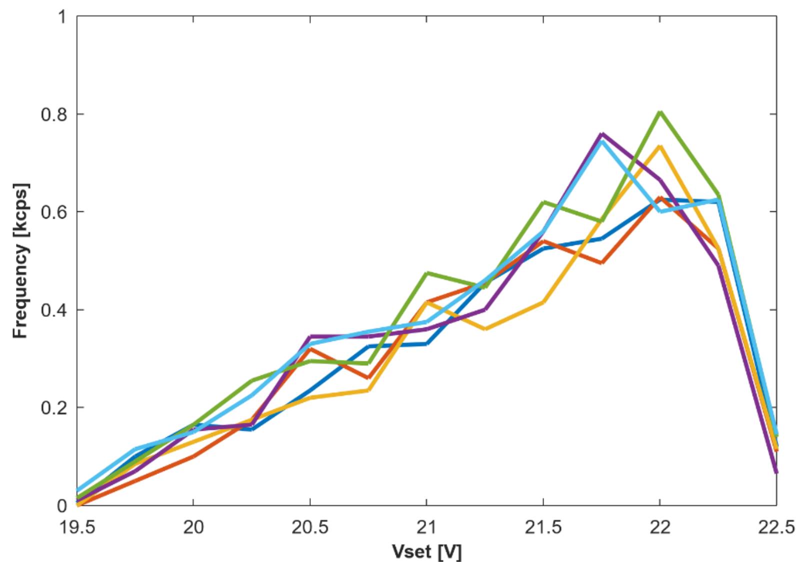


Figure 6.9. Count rate for V_{inj} = 0.00 ... 0.05V, where the base-collector junction operates as a conventional SPAD.

Increasing the injector voltage, it is possible to map the behavior in the interesting operating region where the electrons reaching the multiplication region effectively generate avalanches. This characterization is shown in Figure 6.10, where a significant drop can be seen for large values of both the voltages: a closer look at the acquired waveforms reveal that the pulses become nearer and smaller, until the pulse detection algorithm fails. Indeed, earlier works such as [Webster2012] with integrated front-end do not see this effect.

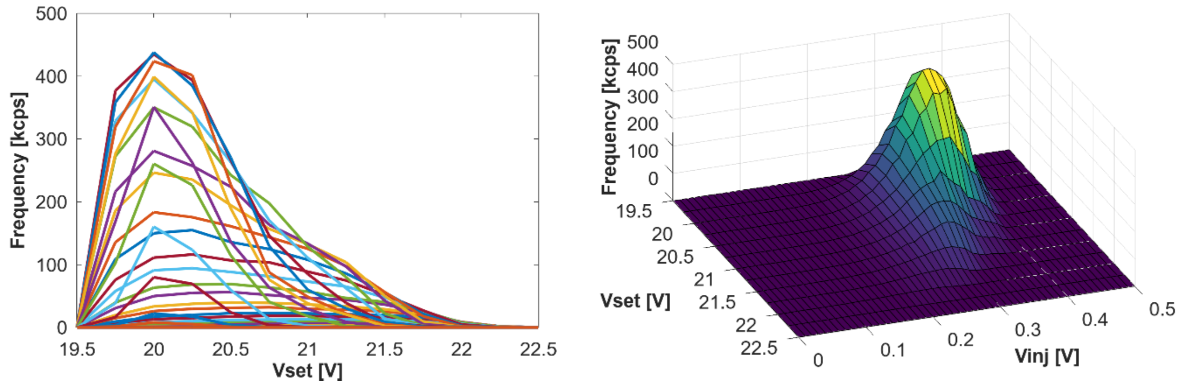


Figure 6.10. Count rate as a function of V_{inj} and V_{set}: the rightmost surface plot allows to qualitatively catch the device behavior.

In order to understand the usability as a signal multiplier for the THz detector, it is important to evaluate the sensitivity of the device count rate to the change in V_{inj}, that is expected to be caused also by the THz detector. The plot of Figure 6.11 represents the previous data in function of the injector voltage, with the highest curve being the $V_{set}=20V$: unfortunately, beyond this value the avalanches start to be not anymore recognizable from the acquired waveforms.

It can be seen that below $V_{inj}<0.1V$ the device noise dominates (corresponding to the counts visible in Figure 6.9), that sets the minimum current that can be sensed by the SEBAT. Extrapolating the characteristics at $V_{inj}=0.1V$, the injected current and therefore the smallest measurable current should amount to approximately 1pA (this value is just a ball-park figure, but enough to understand the order of magnitude). The electron rate at 1pA is 600kcps, that gives a relatively low efficiency of 10^{-4} ([Lany2008] evaluated a 0.7 efficiency). One of the causes could be the presence of a potential barrier that prevents electrons from the injector to easily reach the avalanche region.

From this first analysis it is possible to find several aspects to be improved in future trials, such as integrating a quenching front-end in order to expand the count rate capability, and the improvement of the device efficiency.

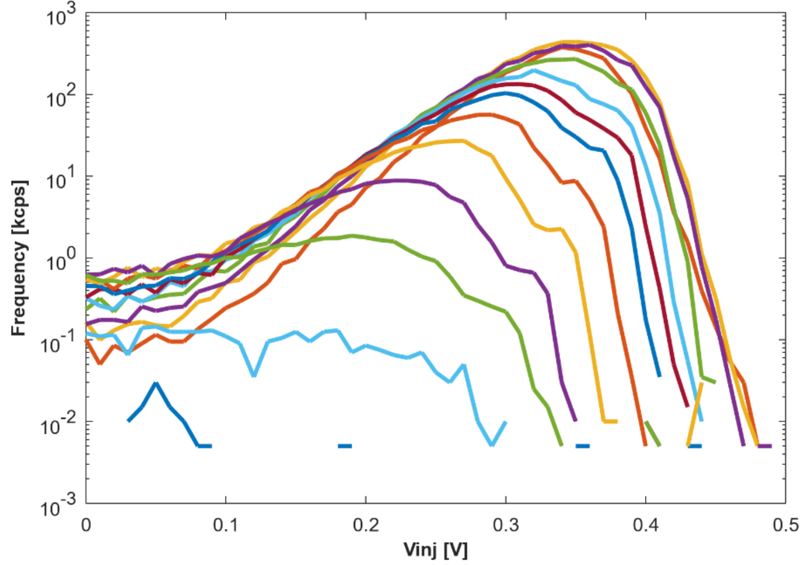


Figure 6.11. Count rate variation vs. injector voltage: maximum values are obtained before saturation of the measurement system at about 0.35V and show an exponentially increasing envelope.

More interesting for the THz detection are the plots obtained in Figure 6.12, where the SEBAT bias has been limited to V_{set}=*19.75, 20.00, 20.25, 20.50V* that exhibit the largest frequency. In this case, two quantities have been defined. The sensitivity S_{THzSET} can be defined as the derivative of the previous plot and gives the sensitivity of the count rate for a signal applied at the injector, while the signal-to-noise ratio SNR_{THzSET} is the sensitivity normalized by the standard deviation of counts (square root of counts for a Poisson process) in a bandwidth of 1Hz:

$$S_{THzSET} = \frac{df_{THzSET}}{dV_{inj}} \tag{6.1}$$

$$SNR_{THzSET} = \frac{S_{THzSET}}{\sqrt{f_{THzSET}}} \tag{6.2}$$

Figure 6.12(left) shows the sensitivity, reaching a maximum value of *5.7kcps/mV* at V_{inj}=*0.32V* and V_{set} = *20V*. Figure 6.12(right) instead plots the expected signal-to-noise ratio, with a peak value of *10mV^{-1}Hz$^{-0.5}$* at the same conditions. As an example, in these conditions 1mV of signal creates a Δf_{THzSET} = *5.7kcps*, and if evaluated during 1 second it achieves a signal-to-noise ratio of ~10.

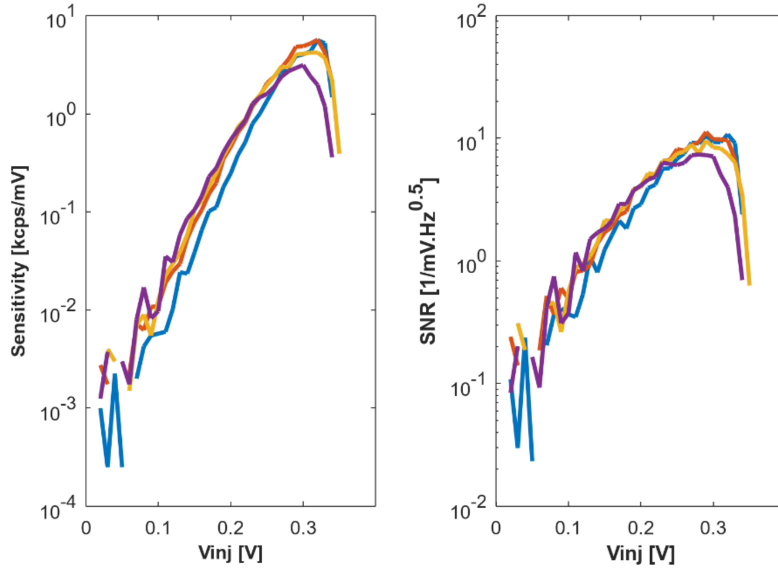


Figure 6.12. THzSET sensitivity in count rate variation over injector voltage (left) and signal-to-noise ratio as the counts standard deviation in 1 second for a milliVolt variation (right). V_{set} = 19.75, 20.00, 20.25, 20.50V.

6.2.3 Terahertz Characterization of the THzSET Device

Due to the low efficiency of the SEBAT, the expected signal in frequency will be extremely low, as calculated in the previous paragraph, and therefore it is very difficult to perform a "blind" alignment of the THz source in the setup. In order to have better chances of identifying the signal, a setup like the one of Figure 6.13 is prepared, using the schematic of Figure 6.14. Here the FET is biased with a given V_{inj} and V_G, and the AC signal V_{det} is measured by the lock-in amplifier. It is necessary to bias the base of the SEBAT in order to bring the diode in conduction: this lowers its equivalent dynamic resistance and permits the detected signal to reach the output terminal at V_{inj}.

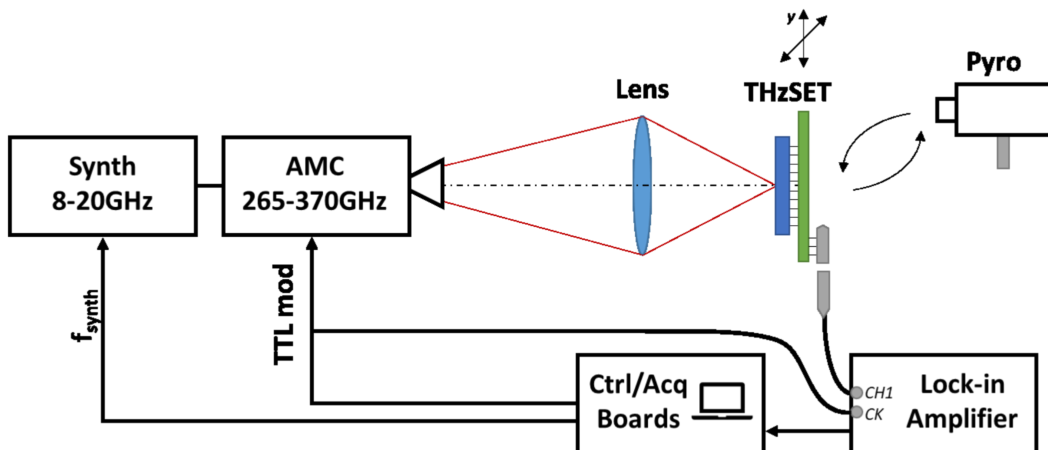


Figure 6.13. THz setup for the THzSET voltage mesurement.

Here the FET detector is "loaded" with an equivalent resistance of 1MΩ (needed to measure the injected current) in parallel with the ADC2 input resistance, again of 1MΩ. The resulting

500kΩ resistance is expected to lower the response by a significant factor (see paragraph 3.2.3). The FET output resistance changes steadily from 865kΩ at V_G*=0.35V*, to 91kΩ at V_G*=0.45V*, with an attenuation factor $R_L/(R_{DS}+R_L)\approx 0.366\div 0.846$. Moreover, there is the series of the base-emitter diode of the SEBAT that is surely compressing, with its exponential relation between current and voltage (dynamic resistance), the detected voltage: for these reasons, the signal will result strongly attenuated. However, a gain factor can be expected due to the bias current, realizing substantially a common source amplifier with the detector acting as the active device.

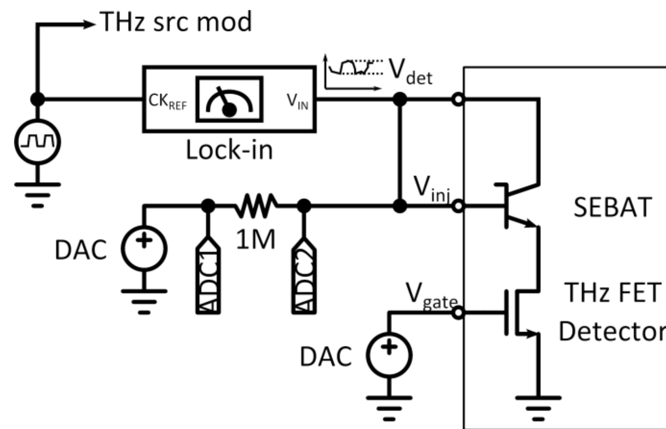


Figure 6.14. Schematic for the voltage THZ measurements of the FET detector

With the optimization of the source-lens-detector distance and the xy position of the detector, the results of Figure 6.15 have been obtained. The best operating conditions result to be f_{src}*=337.5GHz* (exploiting a constructive interference) and V_G*=0.46V*, with a detected voltage of V_{det}*=68μV*. With a fixed DAC voltage of 2.5V and low V_G, the resistive partition 1MΩ(RES)+1MΩ(ADC2) brings the DC value of V_{inj}*=1.25V* but with zero drain current: the net drain current of the detector then increases as soon as the gate bias goes beyond the threshold, bringing to some signal amplification.

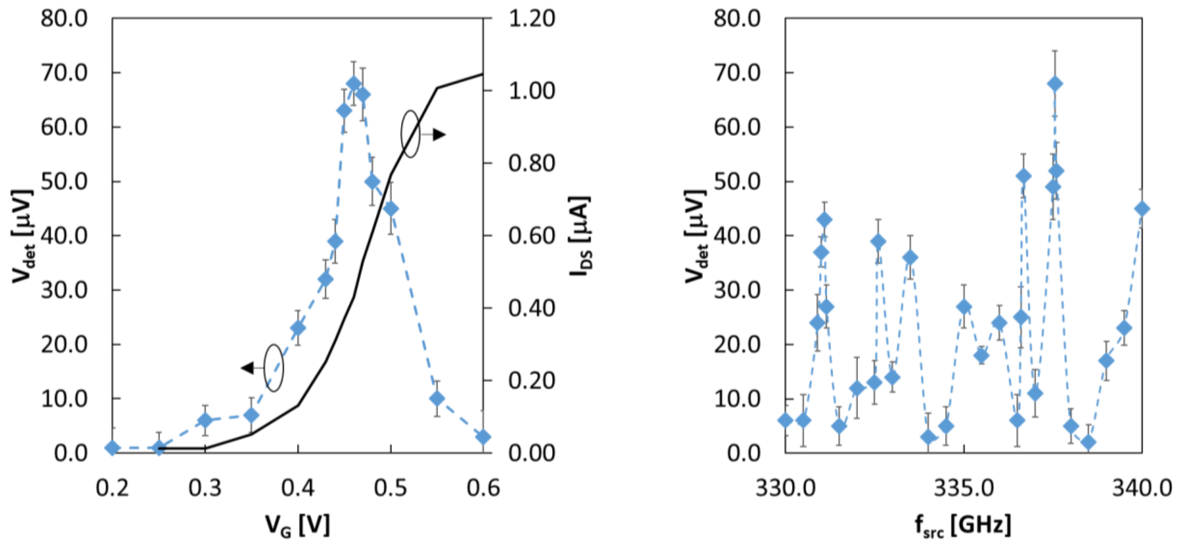


Figure 6.15. Voltage response of the THzSET detector without avalanches, in function of the FET bias with the drain current at f_{src}=337.5GHz (left) and in function of frequency at V_G=0.46V (right).

After the measurements of Figure 6.15, a further slight improvement of the signal has been achieved, getting eventually 86µV of net signal at $f_{src}=331.8GHz$ and $V_G=0.48V$.

However, as described in the previous paragraph and clearly visible in Figure 6.12, the best conditions for the THzSET device are between $V_{inj}=0.3\text{-}0.35V$. Extrapolating the value by performing measurements at different voltages, and considering the load effect factor $R_L/(R_{DS}+R_L)\approx 0.366$, it can be expected to have $V_{det}=8.6\mu V$ at $V_{inj}=0.32V$ and $V_G=0.48V$.

With the very same setup position and conditions (maximized response), the schematic of Figure 6.4 is put in place, now evaluating the THzSET pulses frequency. The measurement setup now uses the PC-controlled acquisition boards as shown in Figure 6.16: together with the modulation frequency, also the slow UCA control is employed to get a cleaner signal.

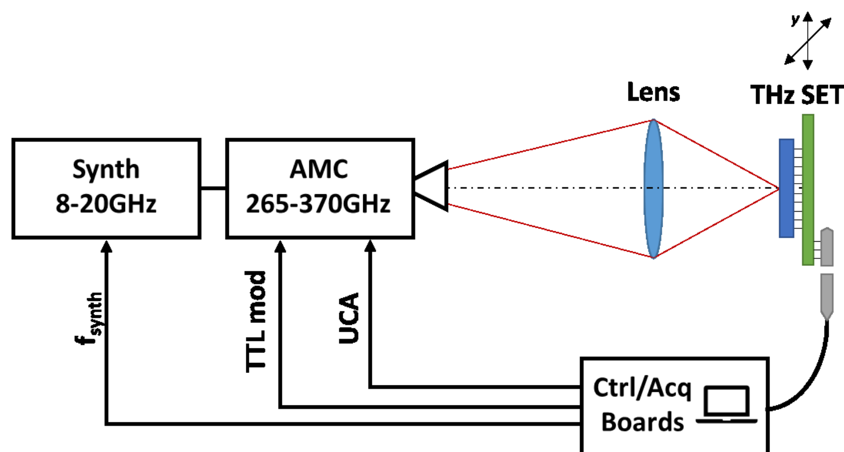


Figure 6.16. THz setup for the THzSET frequency measurement

The acquisition strategy (Figure 6.17) foresees the evaluation of the measured frequency by acquiring $N_{sample}=6M$ analog voltage points at $5MS/s$ (for memory and processing reasons, 30

chunks of 200kpts), i.e. 1200ms of "integration time". This phase is repeated both with the signal on and off, by using the source TTL modulation, obtaining $f_{bg}(t)$ – the background counts – and $f_{src}(t)$ – the source and background counts. The resulting frequency difference, ideally containing the detection contribution, is further modulated with the user-controlled attenuation. Therefore, both $\Delta f(t)^{on}$ and $\Delta f(t)^{off}$ are acquired $N_{UCA}=100$ times, averaged and subtracted, eventually yielding the final Δf with double modulation.

The overall observation time is $2N_{UCA}\times 2N_{sample}\times 200ns=240s$; a relatively long time that in practice is also slightly increased due to the data transfer from the acquisition boards to the PC, and the processing time. This long acquisition is justified by the calculations previously shown: an expected THzSET signal of $8.6\mu V$ with a sensitivity of $5.7kcps/mV$ should bring to a frequency variation of $\Delta f_{THzSET}=8.6\mu V\cdot 5.7kcps/mV=49.02cps$, moving around an average $f_{THzSET}=300kcps$. From eq.(6.2) the expected is $SNR(1)=8.9\cdot 10^{-2}$ for 1s observation, while a 240s observation time would lead to $SNR(240)=SNR(1)\cdot\sqrt{240}=1.37$, slightly above unity: enough to recognize the signal across multiple Δf acquisitions.

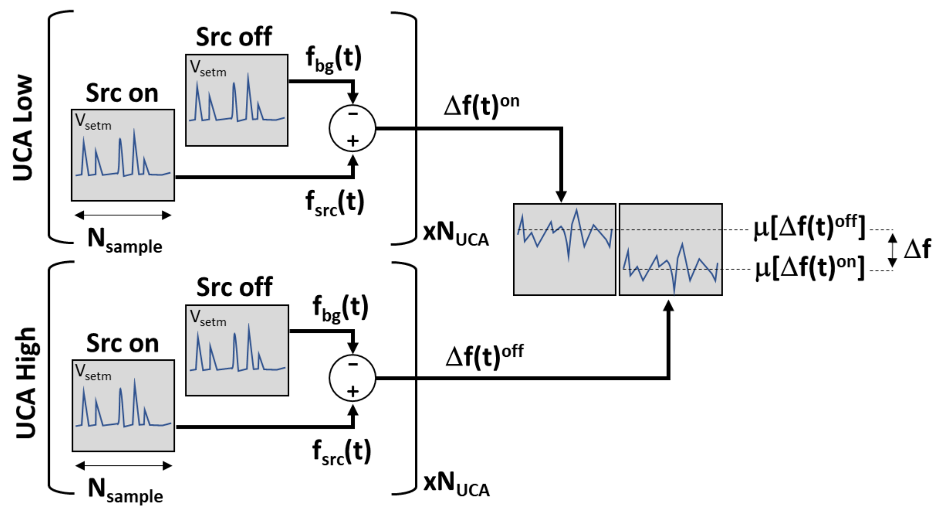


Figure 6.17. Scheme of the THzSET frequency acquisition with the additional UCA modulation.

An acquisition has been performed with the following THzSET bias conditions: $V_G=0.48V$, $V_{inj}=0.31V$, and $V_{SET}=21.21V$. This slightly changed optimal point has been necessary in an effort to further reduce the failing rate of the frequency extraction algorithm, that would have been dramatic for very long acquisitions. One example of the obtained waveforms are plotted in Figure 6.18, where 6 UCA periods have been acquired and the difference is evaluated at every transition of V_{UCA}: thus obtaining 12 values of Δf: ideally, $\mu[\Delta f(t)^{on/off}]$ should be a square wave in phase with the user-controlled attenuation, and Δf constantly positive.

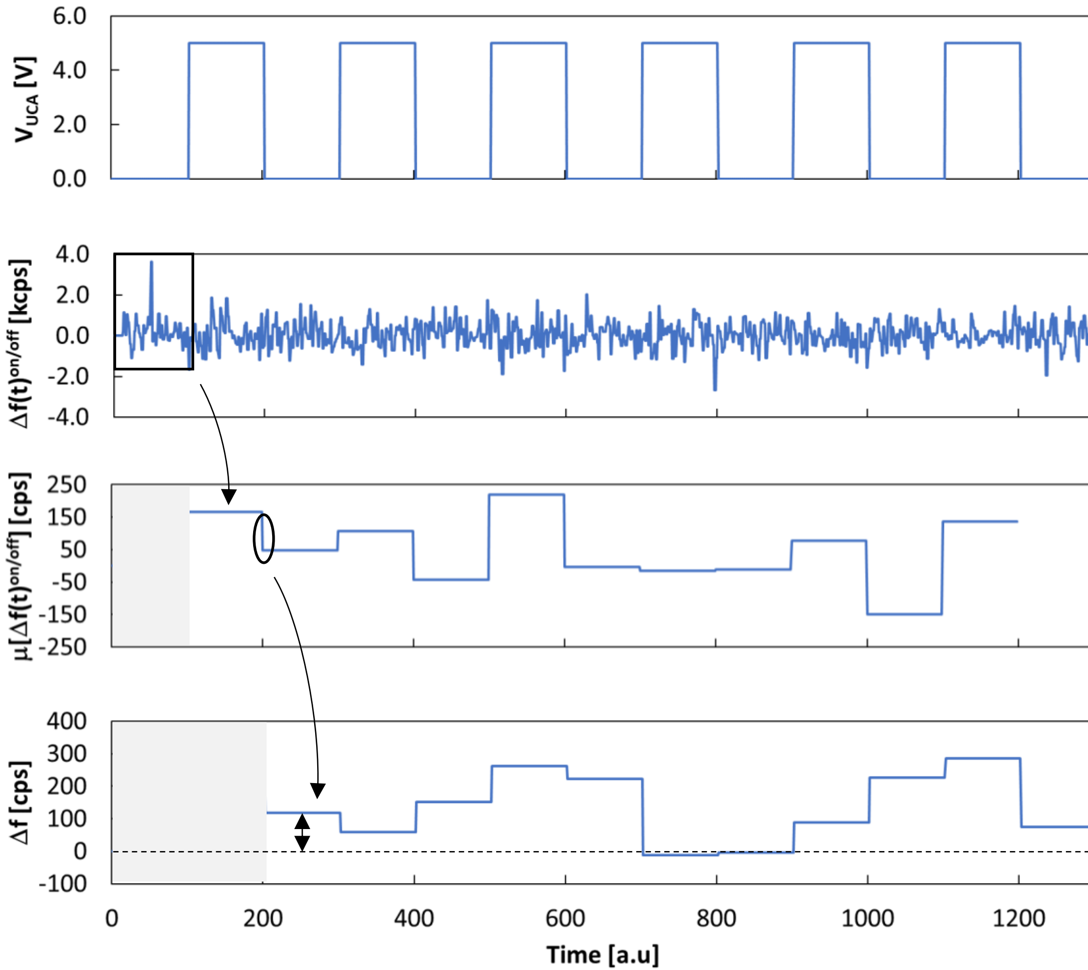


Figure 6.18. THzSET frequency measurement results, from top to bottom: UCA modulation, frequency difference from source modulation, average of frequency difference in UCA phases, final frequency difference of averages.

This single measurement, clearly noisy, shows an average $\Delta f=134cps$ with a standard deviation of 99.3cps (obtained at each UCA transition, so for samples every 120s), therefore with a SNR slightly higher than unity and values in the same order of magnitude with respect to the expected ones, and *proves the validity of the THzSET principle of operation*.

The difficulty of finding an optimum setup and the very weak signals prevented a thorough characterization, for example calibrating the input power. However, it has been roughly estimated that the incident power on the detector could be of about ~40μW, thus bringing to an estimated THzSET detector *frequency responsivity* (the output is indeed in counts per seconds) of $R_f=134cps/40\mu W=3.35\cdot 10^6 cps/W$. The normalization of the noise with respect to responsivity and bandwidth brings to an approximate value of noise-equivalent power of $NEP=N_f/R_f=99.3cps\cdot\sqrt{120s}/3.35\cdot 10^6 cps/W=324.7\mu W/\sqrt{Hz}$.

Even though with a very low statistics and therefore low SNR, it has been possible to perform an acquisition with different gate bias of the FET, V_G, and with different injector voltage, V_{inj}. The results are plotted in Figure 6.19 and Figure 6.20, respectively.

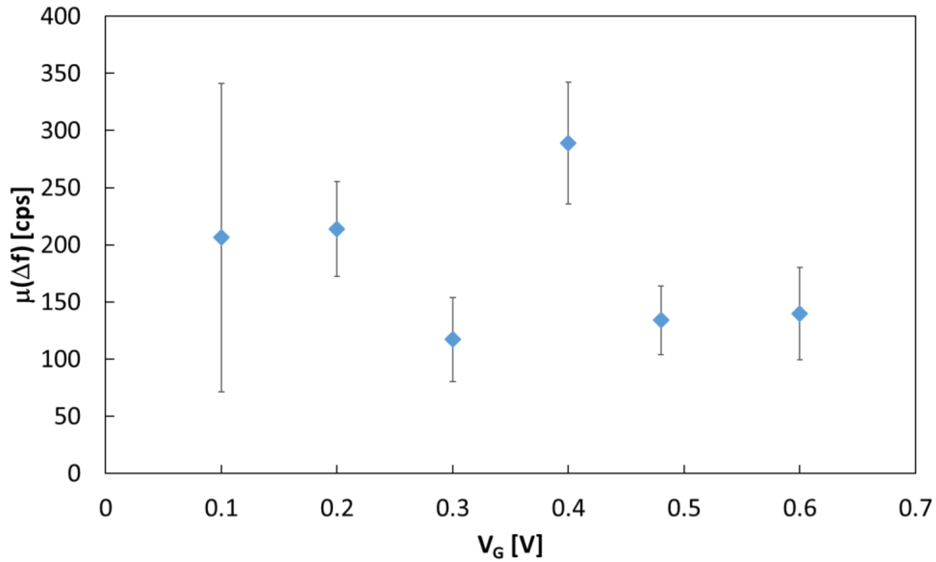


Figure 6.19. THzSET frequency difference response in function of the FET gate bias. Error bars indicate the 1σ confidence of the measurement.

The expected behavior in function of the gate bias should see a maximum at V_G=*0.4V*, with the signal decreasing at low and high bias. It can be seen, from the large error bars, that this measurement is insufficient to evaluate a trend. At the same time, it confirms the operation of the THzSET detector, clearly providing a constantly positive signal for all measured values.

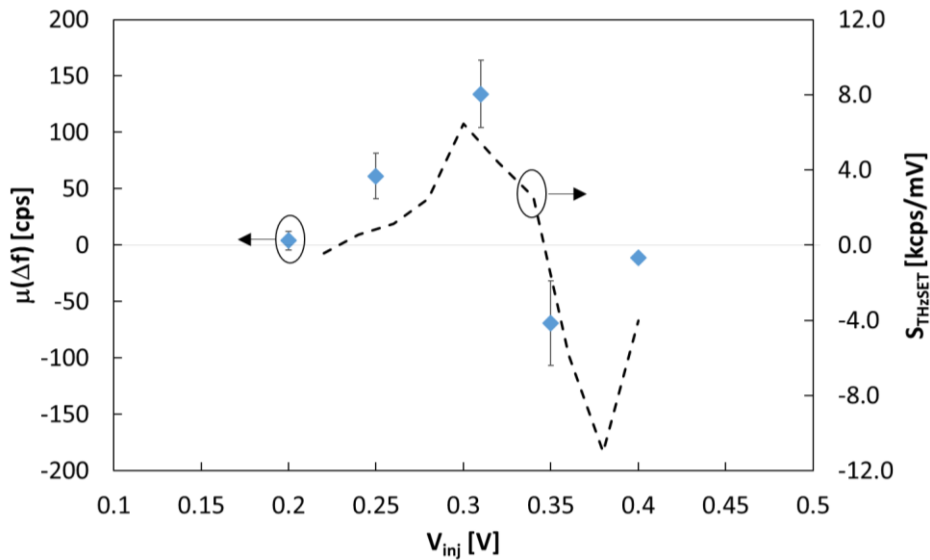


Figure 6.20. THzSET frequency difference response in function of the injector bias, superimposed with the SEBAT sensitivity. Error bars indicate the 1σ confidence of the measurement

Similarly, the measurements in function of the injector voltage of Figure 6.20 are affected by a relevant error but it is possible to notice that is follows quite well the expected behavior. Indeed, plotted as a dashed line is the SEBAT sensitivity (first derivative of the absolute frequency with respect to the injector voltage), that reaches a peak at about V_{inj}=*0.3V* and then brings the response to negative levels beyond the frequency peak, again confirming the

validity of the measurements acquired so far. It is worth noting that the frequency drop that causes the negative peak, apparently of relatively high absolute sensitivity value, is due to the counting failure at too high frequency and it has been considered not reliable enough to provide another optimum for the device operation.

6.2.4 THzSET performance summary and discussion

The overall THzSET measured performance are shown in Table 6-1, where the terahertz responsivity and NEP are a rough estimate (not accurately calibrated). It has been demonstrated that it is possible to sense THz radiation with this device, although with limitations due to the reduced sensitivity. Nevertheless, the potential is very high, as the THzSET device represents an extremely compact terahertz-to-frequency converter, that can be easily converted into a digital number with the use of a simple counter.

Table 6-1. Performance summary of the SEBAT/THzSET device.

Parameter	Symbol	Value	Unit
SEBAT device (THz detector inactive)			
Breakdown voltage	V_{BD}	19.5	V
Dark counts at 2.5V excess bias (no injection current)	DCR_{SEBAT}	600	cps
Max count rate	f_{max}	430	kcps
Dynamic range	DR_{SEBAT}	57.1	dB
Electron-avalanche efficiency	η_{SEBAT}	10^{-4}	
Estimated minimum measurable current	I_{min}	1	pA
THzSET device			
Maximum sensitivity	S_{max}	5.7	kcps/mV
Maximum SNR	SNR_{THzSET}	10	$mV^{-1}Hz^{-0.5}$
Estimated responsivity	R_f	3.35	Mcps/W
Estimated noise-equivalent power	NEP	324.7	$\mu W/\sqrt{Hz}$

There are several improvements that can be done and that make this device potentially promising as THz detector:

- Currently the pulses are detected externally, with large parasitic capacitances that make the process slow and noisy, while the analog acquisition with filtering and threshold is sensitive to the biasing conditions. By switching to integrated quenching and pulse detection (for example with commonly used SPAD active quenching circuits), it is expected to reach >10Mcps, with a potential 100× boost in sensitivity and 10× increase in SNR.

- The SEBAT efficiency of the present implementation is low ($<10^{-3}$): there are demonstrations in literature of higher efficiency devices, therefore it is expected that with additional device simulation and optimization it will be possible to increase it by 2-3 orders of magnitude, thus bringing the sensitivity to a much higher level.
- Integration of fast counters, for example programmable up-down counters directly on the chip, near to the device, is an easy task that together with the integrated quenching simplifies enormously the measurement setup and the acquisition. This is expected to improve the measurement efficiency, with easier and faster characterization.

Overall, bringing the THzSET to the FET detection limit means lowering the NEP from 324.7μW/√Hz down to <100pW/√Hz, i.e. improving the SNR by a factor of *10⁶*, which is a huge step. Nevertheless, as discussed before there is margin for improvement, potentially several orders of magnitude, that can make this solution interesting. In particular, for higher frequencies where the pixel/antenna size is such that it is not possible to integrate complex electronics such as in Chapter 4, the very compact solution of a simple THzSET with quenching circuit and an up-down counter can be extremely attractive with large pixel counts. There is surely need for more investigations, modeling, and additional understanding of how this device could be improved.

6.3 Graphene THz Detectors in CMOS

In the theory of plasma waves of THz detectors [Dyakonov1996] there is another operating mode with respect to the one analyzed up to now: it is the so-called *resonant plasma wave detection*, where the mobility of the carriers in the channel is high enough that, at THz frequencies, the plasma wave propagates in the channel creating a stable, resonant, standing wave. The advantage of such a condition is that the response at resonance is much higher, depending on the resulting quality factor, and that the center frequency is potentially tunable with the bias conditions of the detector. Resonant detection has been proved with HEMT (high-electron mobility transistors) such as in [Knap2002b]; due to its potentially very high mobility, also *graphene* is a material that can exhibit such a condition [Bandurin2018]. In this paragraph the focus will be on the challenges of integration of these graphene FET (GFET) detectors in the back-end process of CMOS technology, while for the important properties and applications of graphene, a large number of papers in literature covers all the aspects, in particular in the field of detection [Rogalski2019].

6.3.1 Detection of THz with graphene FET

The principle of operation of the GFET detector is the same of the silicon MOS detector, with the intrinsic differences given by the transistor characteristics. A GFET transistor (Figure 6.21)

is made by a graphene sheet connecting two electrodes, namely the source and drain, and a gate electrode separated by a thin dielectric with respect to the graphene region that represents the transistor channel.

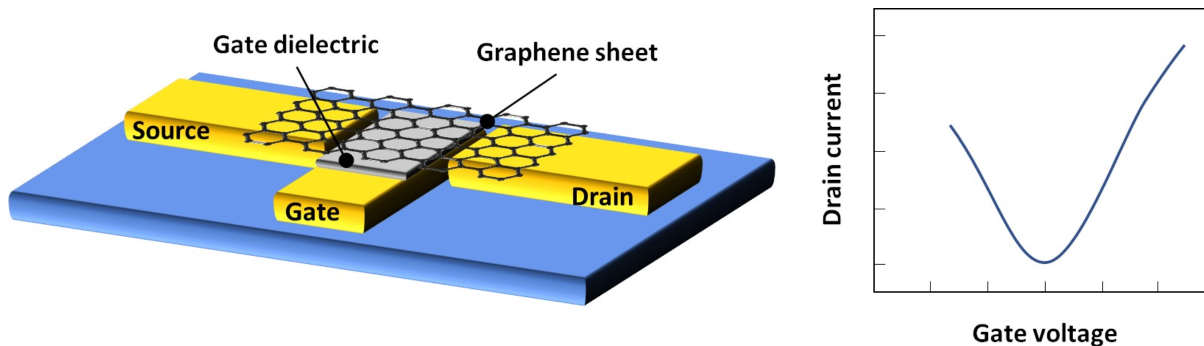


Figure 6.21. Pictorial representation of a GFET device

Typically, custom designed GFETs are built by transferring on a specific substrate (e.g. silicon carbide) a graphene “flake”, and then metals/dielectrics are patterned on top, in the right position [Bianco2015], that is hardly compatible with standard CMOS processing. Therefore, techniques targeting growth or transfer with precise patterns has been researched and developed [Bianco2020].

The GFET, ideally, is a symmetric device: the electric field induced by the gate voltage causes the graphene to move from a charge neutrality situation (the Dirac point) to a p-type transistor behavior ($V_G<0$) or to a n-type transistor behavior ($V_G>0$) as shown on the right side of Figure 6.21. The nonlinearity in proximity of the Dirac point operates in the same way as observed for silicon FETs for what concerns THz detection: it can be shown that the responsivity is approximated by $1/\sigma\ d\sigma/dV_G$, where σ is the source-drain conductivity of the GFET.

6.3.2 Integration of GFET detectors in CMOS

In this activity, the goal is to *realize the GFET at the end of the CMOS fabrication process*, thus exploiting the integrated circuit for amplification, multiplexing, and readout, together with the antenna implementation. Therefore, it is necessary to pay attention to the final steps of the CMOS back-end of line (BEOL) process (i.e. the metallization and dielectrics) in order to enable graphene transfer and contacting.

The first attempt contains several different structures: 3x4 pixels (300GHz) and 4x3 pixels (850GHz), and a small (2THz) test antenna, implemented in a standard 150nm CMOS technology. The primary goal is to check the GFET realization, and if successful, to evaluate the THz responsivity and noise. In order to realize the thin gate oxide, the chosen strategy was to complete the standard CMOS process, and perform a post-processing DRIE (deep

reactive ion etching) step, tuned to remove the top passivation down to 100nm±10nm. Figure 6.22 shows the detail of the fabricated chip, and the desired processing and final result.

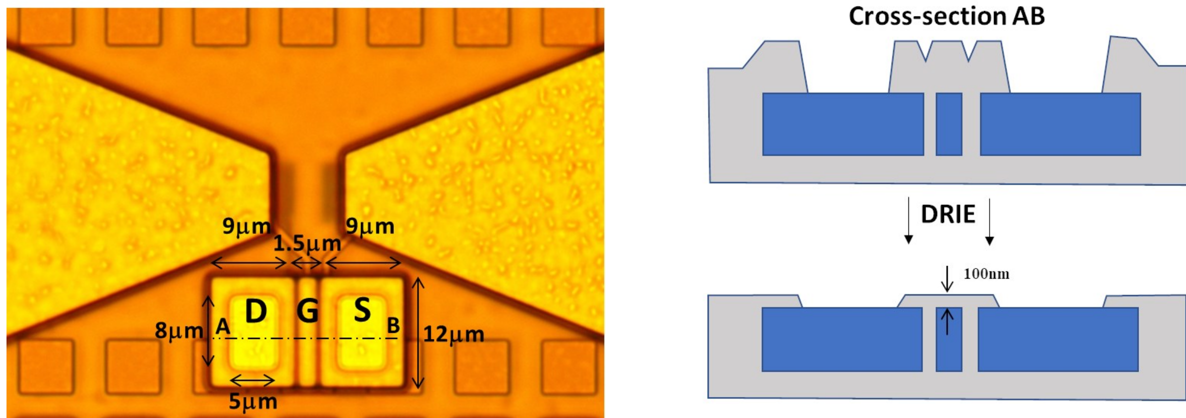


Figure 6.22. Detail of one of the fabricated structures (left) and post-processing to achieve the 100nm gate oxide using deep reactive ion etching (right).

However, during the graphene transfer (realized by the University of Pisa and Graphenea, Spain) it was clear that the single-atom layer was not adhering to the surface and cracked in many areas. Therefore, a deeper analysis of the surface was performed, acquiring the surface topology with atomic force microscope (AFM).

As visible in Figure 6.23, an oxide spike is present around the pad opening: after discussion with the process engineers, this may be due to a residue of polymer from the CMOS fabrication process. The height and sharpness of the oxide spike is such that it prevents a proper graphene transfer: several additional trials have been made to remove this spike, but without success.

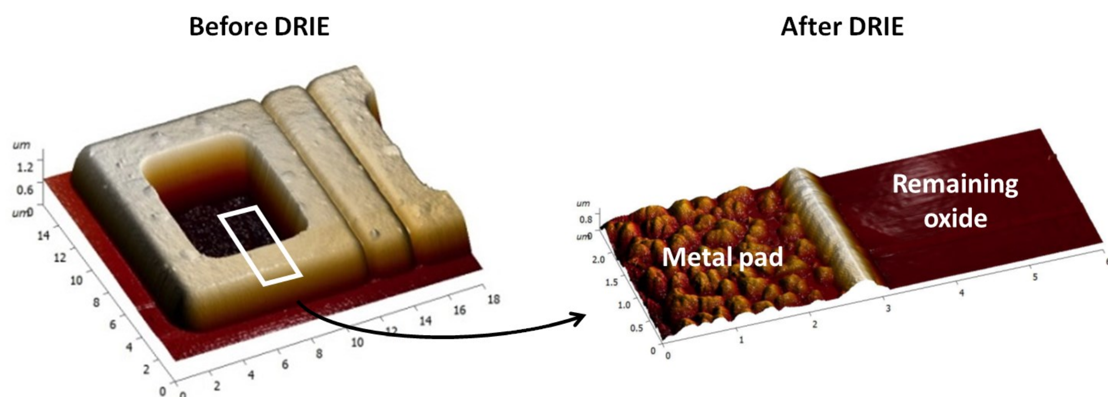


Figure 6.23. AFM profile of the GFET area before thinning (left) and after DRIE etching (right) showing the residual oxide spike

Because of this, the second attempt has been made by agreeing with the foundry about a specific BEOL process, ensuring better planarity. The chip has been redesigned so that it contains an array of 11x10 550GHz antennas, making also possible to evaluate the yield of

the GFET realization. Each pixel has two readouts, one passive (via switches) and a second one with a source follower buffer. The pixel's output is multiplexed to an unbuffered output or, in parallel, to a low noise amplifier. One out of the 11 columns is reserved for electrical tests.

Figure 6.24 shows the realized chip micrograph and the results of the custom CMOS BEOL processing. The scanning electron microscope (SEM) shows a successfully planar structure, with a topology roughness well below 20nm and a gate oxide of 110nm.

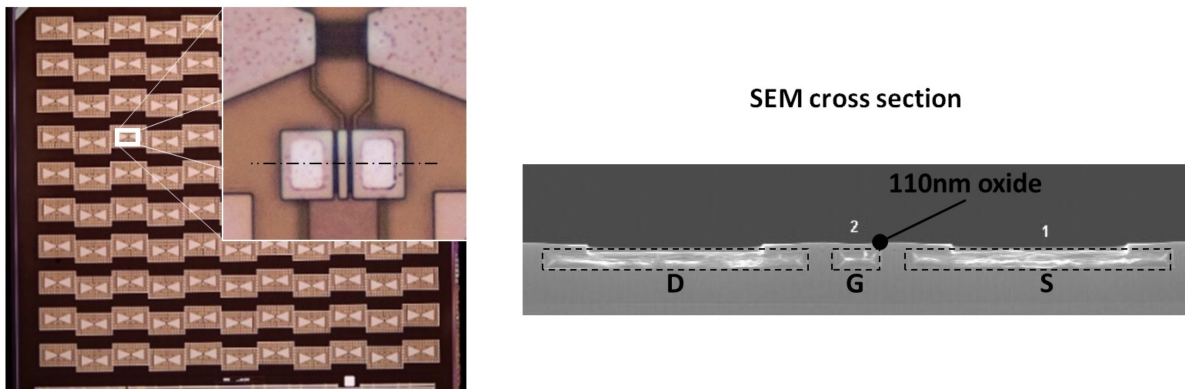


Figure 6.24. Micrograph of one of the structures of the second attempt and SEM cross-section showing the result of the custom BEOL processing with 110nm gate oxide.

The GFETs were then realized using graphene produced by chemical-vapour-deposition (CVD). The graphene was synthetized by Dr. C. Coletti’s group from Istituto di Tecnologia Italiano (IIT, Italy) using spatially-ordered growth and patterning [Bianco2020]. A semi-dry transfer technique was used to detach graphene crystals from copper foil and transfer them onto the chip by precisely placing the crystals on top of FETs electrodes area with micrometer resolution. The successful graphene transfer on top of the CMOS chip and electrodes area was confirmed by micro-Raman spectroscopy. The patterning of the transistor channels was realized by a polymer mask defined via electron beam lithography (EBL) and subsequent dry etching (oxygen-based reactive ion etching). An overall yield of about 75% was achieved, as depicted in Figure 6.25(left).

The IV characterization of the drain-source connection was performed at the probe station on a single device having access to a test pad. The measurement, plotted in Figure 6.25(right), showed a high contact resistance, exhibiting the typical behavior of soft-oxide breaking: the aluminum of the pads creates a thin native oxide that increases the contact resistance. Measurements with gate voltage modulations showed little or no change of the channel conductivity: it has been evaluated by Pisa colleagues that the 110nm oxide thickness is probably still too thick to allow the gate electric field to influence the graphene.

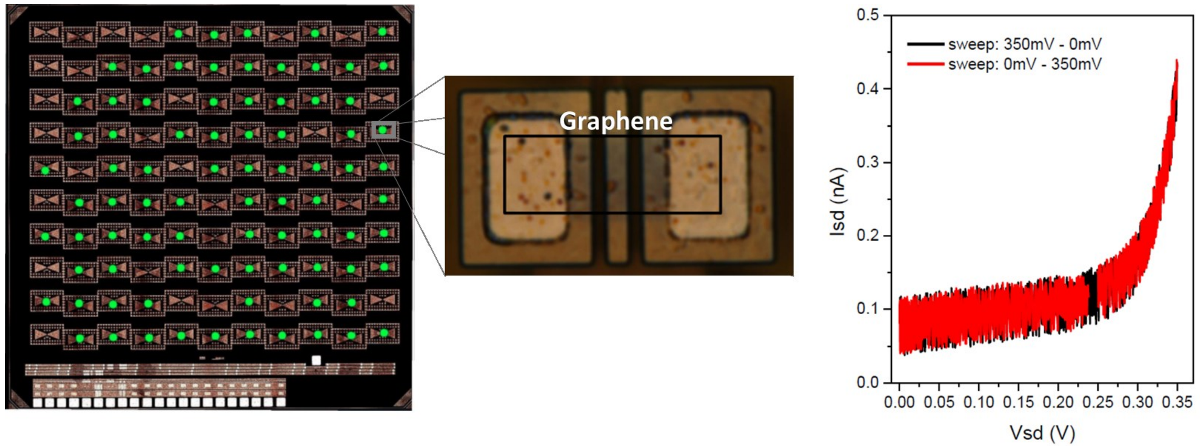


Figure 6.25. Transfer, patterning and measurement of graphene: micrograph of the chip, with green dots indicating graphene correctly covering D-S terminals (left) and IV characteristics of the drain-source connection, showing high contact resistance (right).

While it was possible to break the aluminum oxide at the probe station on a single structure, during the whole chip measurements instead it was not possible to obtain the same behavior. This is due to the fact that the multiplexing electronics was designed to measure the voltage at the drain, and not to apply an external voltage: the series resistance of the switches and the limited voltages that can be applied unfortunately prevent this possibility.

Further trials are ongoing, with refinements of the BEOL processing steps and reduction of the contact resistance.

6.4 Chapter Summary

A *novel device for terahertz detection, the THzSET*, has been introduced in this chapter. It combines a single-electron bipolar avalanche transistor (SEBAT) with a THz FET detector. The potential advantage of this device is its intrinsic voltage-to-frequency conversion that can be transferred in the digital world by a simple counter: that would result in an extremely compact *THz digital sensor*.

The THzSET device has been designed and fabricated, and eventually characterized. Several aspects are far from the optimal condition (i.e. very low electron-to-avalanche efficiency, or need for external quenching and counting, etc.), but nevertheless it has been possible to characterize the device from the electrical point of view.

The tougher challenge was the terahertz characterization: eventually, the weak signal together with the sub-optimal conditions of the prototype did not prevent the verification and validation of the expected operation. As the principle of operation is currently confirmed, there will be the need to optimize the device in order to achieve a higher performance towards its intrinsic limits. To this end, additional modeling, design, and measurements are needed.

In parallel, an activity aiming at integrating THz graphene detectors in CMOS was conducted: in this specific case, challenges were on the technological and processing side, with the need of finding a way to work with a CMOS-compatible BEOL processing and achieving a good contact and adhesion. The main hurdles have been identified as the planarity (solved with a customized BEOL), the oxide contact and the thickness of the gate oxide. Further investigations are ongoing, addressing these issues.

7 CONCLUSIONS AND OUTLOOK

Shooting images has become a more-than-daily activity, and we forget how long it took to get to this point. Despite this, there are wavelengths in the electromagnetic spectrum where still it is difficult to shoot images: one of these is the terahertz range. Terahertz sensing and imaging experienced a flourishing research activity in the last decade, with the CMOS FET approach emerging as a de facto choice for low-cost, room-temperature, and practical THz image sensors. Even in this specific case, an heterogenous landscape of solutions exist, with many variations in the antenna type, detector topology, readout techniques and architectures.

This thesis tried to grab what has been developed to date and make one step further, by exploring the possibility to enhance the sensing capabilities to more than one spectral band. The vision was to realize a device, as small as a conventional camera, able to capture simultaneously terahertz and visible images. The challenge was manifold; not only the integration of the two sensing principles required relevant effort, starting from the sensor level up to the system level, but also the terahertz imaging alone was a non-trivial task to get done.

7.1 ACHIEVEMENTS AND RESULTS

Understanding the THz detector operation and tradeoffs was of paramount importance: while literature search highlighted many modeling attempts, of broad levels of complexity and increasing accuracy, it was clear that there was a lack of a compact and complete analytical model. In practical terms, a pen-and-paper tool that could help in understanding, learning, and designing the main aspects of an antenna-coupled FET detector. This goal was achieved by *the development of a complete model, spanning from the electromagnetic capture to the detection mechanism and the electrical signal readout*. The main characteristic of the model is that it can be used directly with the PDK data, and it does not need any calibration nor fitting from measurement. Validation of the extracted equations has been performed: comparison with measurements realized on fabricated samples in a 180nm CMOS technology showed very good agreement with the model predictions.

The second objective was to define the sensor concept, and with it, the surrounding system enabling multispectral detection. It has been chosen to realize pixels sharing the same focal plane, even if the wavelengths differ more than 3 orders of magnitude. Materials and setups for coaxial imaging experiments have been envisaged, and tradeoffs concerning resolution, optics, and dimensions have been set out. The final outcome of this study was *the concept of the multispectral camera with at its heart a terahertz and visible focal-plane array*.

Terahertz imaging, as mentioned, remains still a challenge. Starting from an existing antenna design, result of a previous activity, the implemented idea was to realize the equivalent of a digital lock-in amplifier in each pixel, with scalability in mind. For this purpose, a continuous-time $\Sigma\Delta$ incremental converter small enough to fit within one pixel has been designed, realizing at the same time signal integration, analog-to-digital conversion, and lock-in operation. *A scalable array of 10×10 terahertz digital pixels* has been realized, limited in number by the silicon size. Together with the terahertz pixels, conventional *3T APS have been integrated to obtain a 50×50-pixel visible image sensor on the same chip*, with a careful layout scheme and addressing architecture.

The realization of terahertz and visible measurements and experiments was the main milestone of the activity, eventually demonstrating *real-time multispectral terahertz and visible imaging in CMOS technology*. Starting with a careful characterization and optimization of each part separately, with dedicated setups, a multispectral imaging experiment confirmed the validity of the approach and demonstrated for the first time a monolithically integrated terahertz and visible imager in standard CMOS.

Along the road, several parallel ideas and activities were explored, in order to anticipate future developments and envisage the evolution of the technology. In particular, the THzSET, a novel type of sensor resulting from *the combination of an antenna-coupled FET detector and a SEBAT* (single-electron bipolar avalanche transistor) device has been conceived, realized, and characterized. Despite the difficulties and non-optimal behavior, it was possible to validate its operation in a terahertz setup, identify weaknesses and propose improvements: possibly, in the future this device could replace the incremental converter and realize ultra-compact digital conversion. At the same time, emerging devices such as *GFET-based terahertz detectors* have been studied from the point of view of integration possibilities with CMOS. Several trials have been performed in order to enable GFET arrays on top of CMOS readout circuits, with the objective to realize high-performance terahertz cameras with resonant detectors. Although a GFET terahertz imager is still not available, many steps forward have been done and new solutions are currently under investigation.

7.2 Future Developments

Overall, the various achievements of this thesis represent only a first small step towards the vision: terahertz and multispectral imaging in everyday life for enhanced sensing. There are several “next steps” that can be done, and some of them are already getting started.

In order to investigate the use of the *multispectral camera* in various applications, it is necessary to have it available as a practical *tool*. Currently, the prototype is a small scale one,

with a total of only 100 THz pixels, and it is suitable just for a laboratory: bulky and not autonomous, it needs various instrumentation, and it is not portable. The realization of a practical prototype is fundamental. Indeed, the present sensor has been designed with in mind the possibility to be tiled in 2x2 configuration, thanks to the single line of pads. As an example, the COB (chip-on-board) assembly of Figure 7.1 is currently under evaluation, in order to increase the number of pixels to 20x20 THz and 100x100 VIS, and to make it more appealing for a wider number of applications.

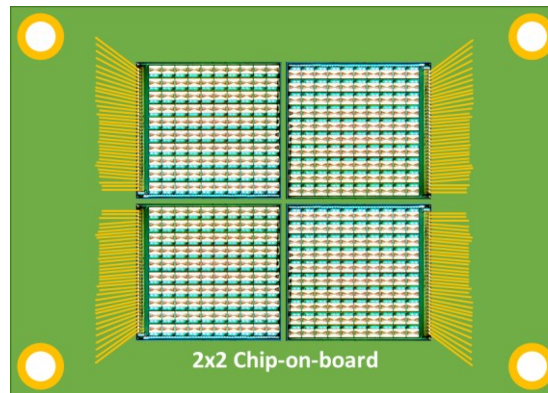


Figure 7.1. Envisaged chip-on-board configuration for a larger focal-plane array.

For what concerns the surrounding electronics and instrumentation, the analog controls can be easily integrated in a compact printed circuit board, while the digital controls can be given by an FPGA prototyping board (e.g. OpalKelly with Xilinx FPGA). Managing 4 sensors in parallel is perfectly feasible as all control signals can be shared, except the terahertz single bit digital outputs that are easily connectable to 4 FPGA inputs, and the visible analog outputs for which a 4-channel ADC chip is needed.

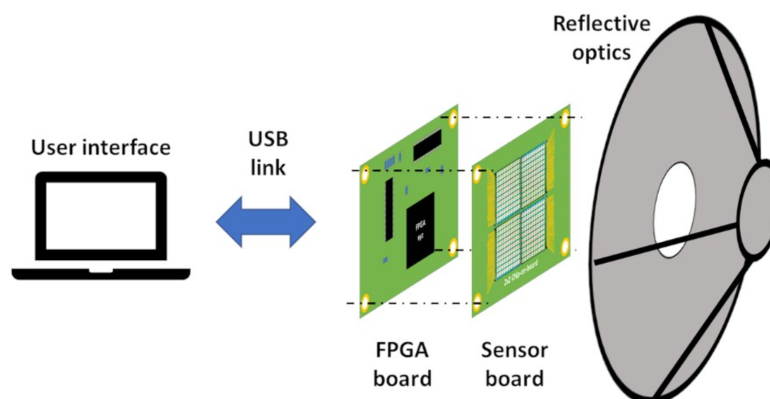


Figure 7.2. Possible configuration of a future compact THz+VIS camera prototype.

For the focusing system, a wideband reflective optics is already on its way, realized with quartz-coated aluminum mirrors and 3D-printed plastic baffles, with a large aperture (~20cm)

to enable collecting more radiation: experiments in terahertz reflection mode could become feasible. Finally, to complete the system, combining all these components with an easy to use graphical user interface for controlling and acquiring data via USB connection would achieve a compact and portable THz+VIS camera, as depicted in Figure 7.2.

On the other hand, during the characterization of the sensor it was possible to discover many issues and various aspects that could be improved: therefore, there is also room for a new and better version of the multispectral imager. Aspects to be explored include:

- *improved noise performance and response of the terahertz channel*, in order to reach the detection limit of the antenna-coupled FET;
- *inclusion of an analog-to-digital converter in the visible imager chain*, in such a way to obtain a fully digital multispectral image sensor;
- *improved quality of the visible image*, for example by including integrated calibration or by increasing the uniformity if the layout;
- *larger number of pixels*, perhaps targeting higher frequencies in the THz domain, or even multiple frequencies.

On the novel detectors' side, the THzSET results are promising and it deserves additional attention and new, improved versions: the objectives should be to seek higher electron-to-avalanche efficiency, realize integrated quenching, counting and counts differentiation, and trying to implement arrays of devices. Similarly, the realization of arrays of GFETs on top of CMOS seems at reach, as efforts continue in the integration trials: once the technological issues are solved, the results obtained in the readout (i.e. ΣΔ converter, THzSETdevice) can be reused and adapted to achieve GFET-based terahertz imagers.

7.3 Closing Remarks

As with many novel or emerging technologies, the scientific community diverges its efforts by researching in different directions. Afterwards, as technology consolidates, natural selection occurs and just few, valid, and robust solutions remain: surprisingly, often simplicity wins. Terahertz and multispectral imaging are no exception: currently, the field still seems to be in its expanding phase, and this thesis is one more contribution to the research diversity.

Nevertheless, there are good signs that the followed road may be a good one for achieving the underlying vision, and if not, I hope it may have triggered growth, improvement, and creative thinking towards new solutions and, eventually, a better world.

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