

6.2.3 Mixed Field irradiation

On July 2016 the Ferrara LHCb RICH Upgrade group performed an irradiation test on the CLARO ASICs at the CERN CHARM facility (Figure 6.14).

CHARM (CERN High energy AccelRator Mixed field) features a wide spectrum of radiation types and energies (called mixed-field radiation environments where protons, neutrons, pions, gamma photons etc. are present), and puts at user disposal the space to test large equipment ($2m^3$ 10^3 kg, along with the precise monitoring equipment needed) and even the possibility to adjust the environment using mobile shielding. In CHARM is possible to recreate any of the radiation environments found in the LHC accelerator chain. The radiation is created by colliding a beam against a fixed target (copper, aluminum or an aluminum sieve, depending on the required intensity). The facility is located just downstream of the IRRAD facility, exploit its proton beam, which would be otherwise dumped. The beam parameters are the same as the IRRAD facility parameters, since it's the same beam. In order to minimize radiation exposure, the equipment to be tested must be installed in the irradiated area without human intervention. This is made possible by using a custom semi-remote lifting and transport vehicle which drives the heavy equipment from the user accessible area into the irradiation area. The equipment service cables are attached to a rail on the ceiling which follows the same track and they will be connected through a patch-panel to the user's control and DAQ system. In the LHC tunnel there are two different radiation environments: one in the tunnel itself, where particles with very high energy are present, and the other in the contiguous shielded areas, where the energy spectrum is dominated by neutrons. CHARM is able to accurately simulate all these environments.

During the test 16 CLAROs have been exposed to the CHARM mixed field. They have been installed on an electronic board as shown in Figure 6.15. Like for the Legnaro ion irradiation and the IRRAD proton irradiation tests, the NI Compact RIO (CRIO) controller has been used for data acquisition. During the irradiation tests the three CLARO currents, the SEU and SEL have been monitored. The total dose absorbed by the chips during the test is 800 Gy, or equivalently $9 \cdot 10^{12}$ $1 \text{ MeV } n_{eq}$, and $3.7 \cdot 10^{12}$ HEH_{eq} . The total number of SEU per chip is reported in Table 6.6. No SEL occurred. The number of SEU occurred in these chips is much lower with respect to the ion and proton irradiation tests one because of the much lower absorbed dose, and the chips operations were not affected by the SEU.

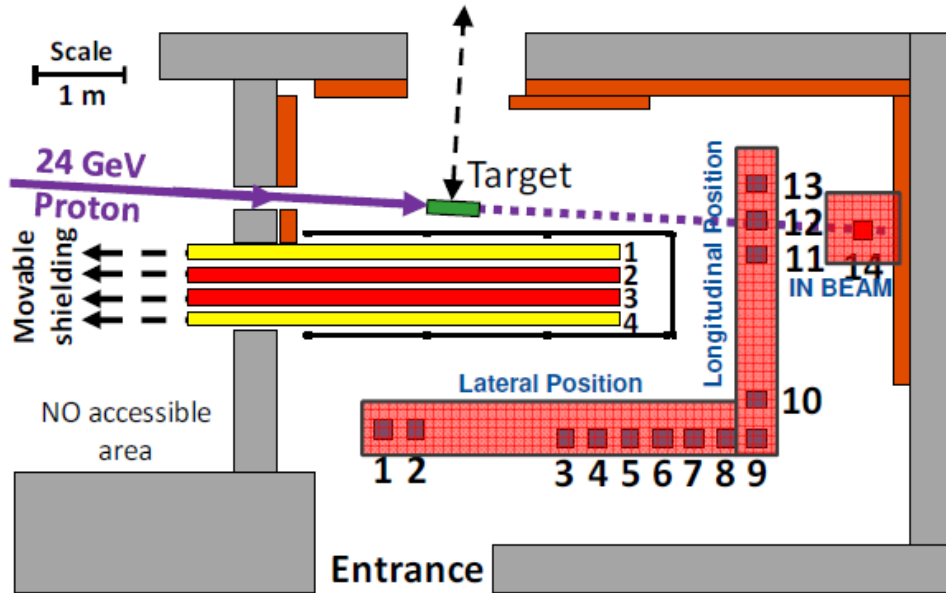


Figure 6.14: Schematic of the CHARM facility at CERN.

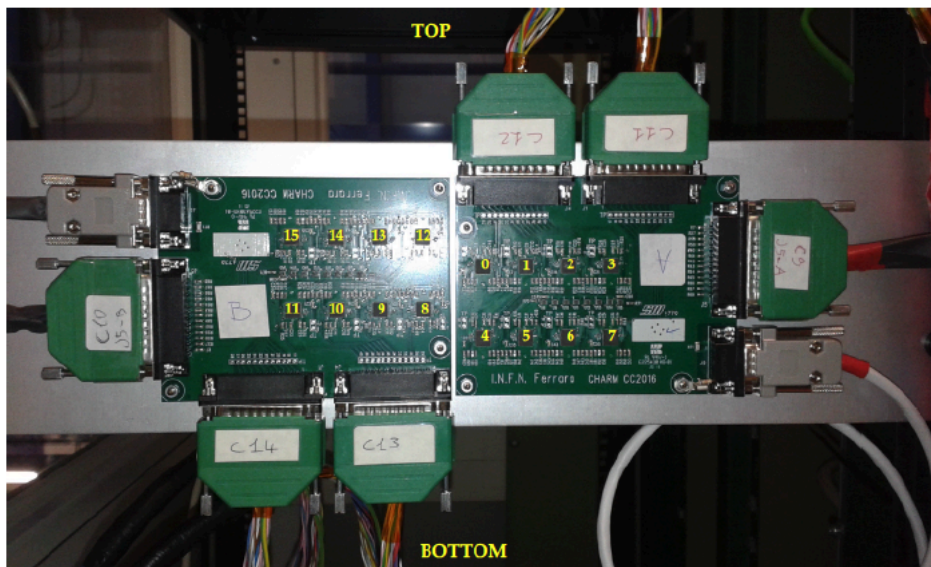


Figure 6.15: CLARO CHARM irradiation setup.

CLARO#	SEU
1	2
2	2
3	9
4	6
5	6
6	4
7	7
8	8
9	7
10	7
11	5
12	4
13	2
14	12
15	10
16	8

Table 6.6: SEU occurred in the CLARO chips used in the CHARM irradiation test.

6.3 Conclusions on the CLARO irradiations tests

The CLARO has been intensively tested using ions, protons and a mixed field as sources of radiation. The TID at which the CLAROs have been exposed during these tests ranges from 10^4 to 10^7 rad, delivered within a few hours/days. This has to be compared to the worst-case scenario of 2×10^5 rad expected for the whole upgrade phase (50 fb^{-1}).

Despite the extreme conditions in which the CLAROs have been tested, they were able to correctly operate and recover from every SEU. A limited amount of SELs occurred only for the highest LET ions and a power-cycle of the devices was able to restore their operations. The CLARO currents maintained a regular behaviour during the tests, increasing when the devices were exposed to the beam and returning to their nominal values once out of the beam.

From these results it can be stated that the CLARO satisfies all the radiation hardness requirements and will be able to correctly operate in the upgraded LHCb detector environment.

Chapter 7

RICH upgrade test-beam

In June and October 2017 two tests-beam have been performed at the H8 beam line at the SPS North Area (CERN Prévessin). The goal was the study of the performance of four fully populated final ECs using the prototype for the Upgraded LHCb RICH Detector. In particular, the MaPMTs, the mechanical housing and the CLARO v3 FE assemblies have been tested, together with the full optoelectronic chain and DAQ system in a realistic upgrade environment.

7.1 Setup

Several institutes contribute to the LHCb RICH collaboration: CERN, the University of Glasgow, the Imperial College, the Rutherford Laboratory, the H. H. Wills Physics Laboratory, the University of Birmingham, the University of Ferrara, the University of Genova, the University of Milano-Bicocca, the University of Edinburgh, the University of Oxford and the University of Cambridge.

In both tests-beam the setup was almost identical (Figure 7.1). In June four R-type ECs have been installed in the prototype, while in October two R-type and two H-type ECs have been initially installed but the test was concluded using four R-type ECs. The latest version of the FEBs (v3) mounting the CLAROV3, have been used in the ECs. The ECs have been mounted on a prototype Photon Detection Module (PDM) to simulate the ECs operational conditions in the upgraded RICH detector. The PDM is mounted on a water cooled cold-bar, which provides the mechanical support and the cooling to the four ECs installed. Moreover, the cold-bar is installed on a translation stage, MICOS MT-85 motion controller and stepper motor drive, with a load

capacity up to 20 kg. The setup temperature is constantly monitored by the ELMB interface and PT100 and PT1000 sensors. The CLARO data readout has been performed by two PDM Digital Boards (PDMDBs) connected to the EC Bkb. The PDMDBs then transmit the data to the DAQ system, called miniDAQ, via optical link. The ground connections for the test-beam is provided by copper braids installed on the cold bar. Both the DBs ground and the metal plate on the backboards are connected to the copper braids. The entire setup is enclosed in a light-tight polypropylene box (also named dark box) that provides thermally insulation for the system. The humidity level is controlled using molecular nitrogen injected in the box. The high voltage and low voltage hardware is composed of the CAEN SY1527 crate, the A1735N HV board with 12 floating channels 1.5 kV/7 mA for the MaP-MTs power supply and the A1517A LV board, with 6 floating channels 7 V/4 A for DBs power supply.

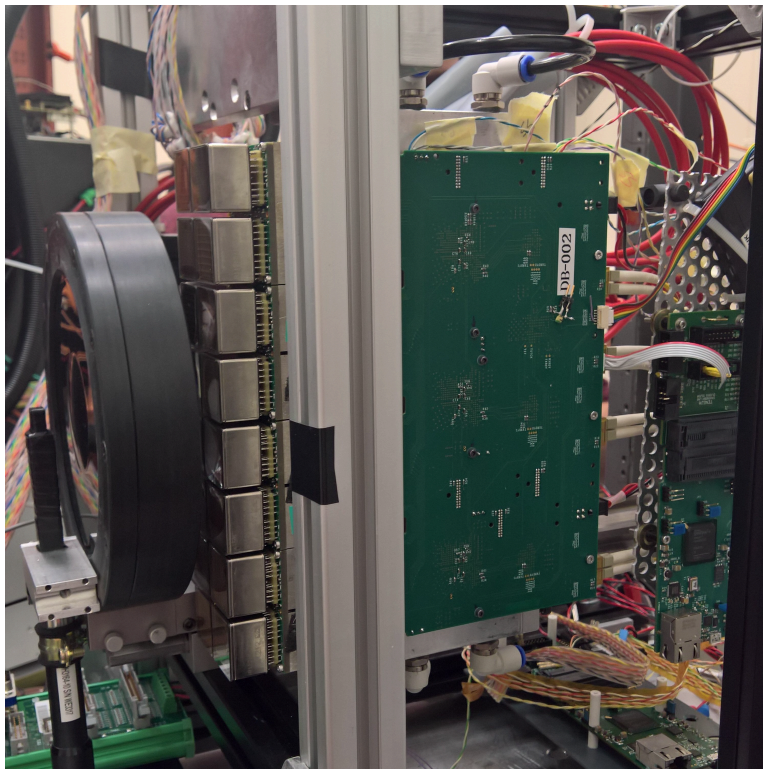


Figure 7.1: The cold bar with four R-type ECs. On the right the lens is visible, surrounded by its black plastic support. On the right the PDMDB is attached to the ECs backboards.

7.1.1 Particle beam and monitoring tools

The beam used for these tests-beam is a secondary beam generated by the collision of the CERN Super Proton Synchrotron beam with a target. This collision generates a beam of 180 GeV/ c positively charged hadrons: 67% protons, 30% pions and 3% kaons. A small background of muons is also present. The beam is divided in spills of about 10^5 - 10^7 particles and these spills last for 3-5 s. Two pairs of orthogonal scintillators are installed in the dark box, one upstream and one downstream the lens used as Cherenkov radiator. These scintillators, each with sensitive area of 8×12 mm² and overlapping area per pair of 8×8 mm², are used to generate beam trigger signals when the limit threshold is exceeded within a pre-set time window. During the data taking the LHCb VELO tracker was also present at a distance of 1230 mm upstream of the RICH prototype. This tracker provides information on the beam profile width and on the beam direction on the x - y plane, which is measured over 75 mm, that is the distance between the first and the last tracking stage of the VELO tracker. A second tracker has been used during the tests-beam. This tracker consists of two tracking stations with four read-out modules each plus a spare module (Figure 7.2). In each module two silicon strip sensors are present, rotated one respect to the other of 40 mrad stereo angle. The silicon sensors strips have an active area of 64×128 mm with 50 μ m x-resolution and 400 μ m y-resolution using the stereo angle. The sensors are from the ATLAS Silicon Tracker (SCT) and they are read out by the ATLAS ABCD ASICs connected to the LHCb RICH DBs equipped with an adapted firmware. The data are sent to DAQ system via 100 MBit Ethernet link connection. The beam trigger signals coming from the RICH scintillators, the RICH tracker and the VELO tracker are combined to obtain detailed information on the beam.

7.1.2 Cherenkov Radiator

The radiator element employed in the tests-beam is a plano-convex lens¹, in which Cherenkov photons are generated. The lens substrate is made of N-BK7, one of the most common technical optical glass, which shows good scratch resistance with low amount of inclusions and it is almost free of bubbles. This material has a high linear optical transmission in the visible range down to 350nm. Moreover, because of stable chemical properties of N-BK7, no special treatments are required to grind and polish the material.

¹<http://www.edmundoptics.com/optics/optical-lenses/plano-convex-pcx-spherical-singlet-lenses/large-pcx-condenser-lenses/27509/>

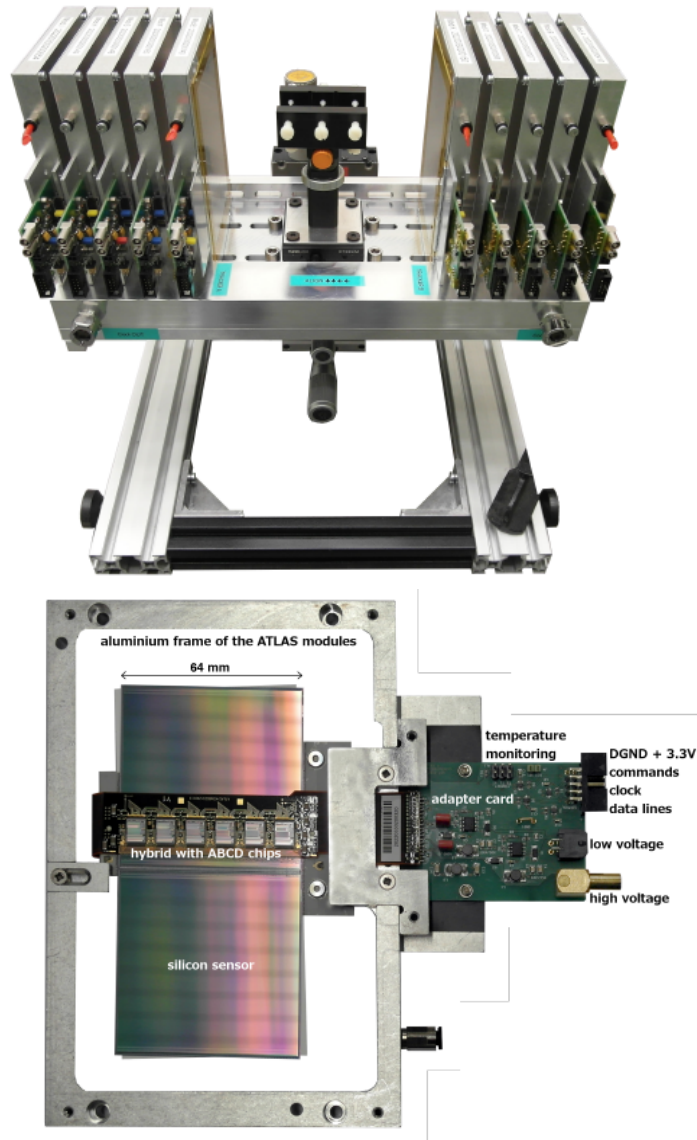


Figure 7.2: Top: the tracker developed by the LHCb RICH Upgrade group for the 2017 tests-beam. Bottom: detailed view of a silicon module and read-out electronics.

Its average refractive index is $n_{lens} = 1.57$. The beam enters orthogonally through the lens at its center. The photons generated in the region of the lens closer to the flat surface are absorbed by a circular layer of black coating attached to the flat surface of the lens. This feature enhances the resolution of the reconstructed Cherenkov angle. The photons generated in the first 12.5 mm

of the lens are internally reflected from the flat surface onto the focusing mirror surface attached to the spherical part of the lens, and then reflected on the upstream photodetector plane. The spherical reflective coating has an annular shape to minimize the background photon reflection, and black silicon covers the remaining area of the spherical part to absorb photons which do not hit the reflective coating. A schematic model of the lens is shown in Figure 7.3.

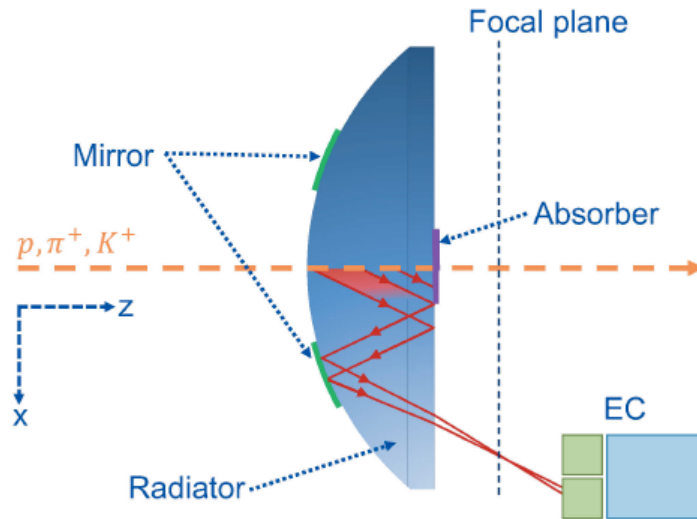


Figure 7.3: Schematic of the lens. The photons path inside the lens is represented by the black lines.

7.1.3 Test-beam DAQ

The LHCb Experimental Control System (ECS) contains the entire experiment control, the monitoring and all the components from the infrastructure equipment to the data acquisition. The LHCb ECS is a distributed system, based on a commercial Supervisory Control and Data Acquisition (SCADA) system, that is WinCC OA, and several custom developed components[58, 59]. WinCC provides several features which are very important for the LHCb ECS: user interfaces, data archiving, a centrally managed alarm screen to handle alarms. The WinCC open architecture makes possible to customize every aspect of the system to better fit the user needs. The LHCb ECS is built as a tree-like control hierarchy structure based on a Finite State Machine (FSM) tree. Commands which are sent from a level of the system are propagated all the way down to the lower leaves which ex-

ecute the actions requested. Then the state of the end-nodes at the bottom of the system is propagated up to the topmost node. The state of the entire LHCb experiment is always visible and can be controlled from a single place. The DAQ system for the tests-beam has been developed in the exact same way using WinCC and a dedicated user-friendly Graphical User Interface (GUI) has been designed to control and monitor the RICH Upgrade prototype in an efficient way. A GUI is an interface that allows users to interact with electronic devices through graphical icons. The top level of the RICH tests-beam WinCC project allows to control the system HV, the Detector Control System (DCS) and the DAQ system. From the top level panel the user can descend into the panels dedicated to each section of the system and operate specific actions for that section. The state of each part of the system is continuously propagated to the top level and the user can correct errors/problems by navigating into the section which is in ERROR state. The top level panel directly shows information on the actual data taking conditions so the user can easily monitor the data acquisition.

7.1.3.1 MiniDAQ

Many new electronics components and systems have been developed for the LHCb Upgrade. All of them will have to be controlled, monitored and integrated into the ECS. The MiniDAQ has been designed to be the development platform for all the monitoring and control activities of the new front-end and the new readout electronics of the sub-detectors. The LHCb MiniDAQ system has two levels: a hardware platform and the corresponding software suite to control and to monitor the hardware. The hardware consists of a CPU server housing a PCIExpress card named PCIe40. The PCIe40 is the core component of the upgraded LHCb Online system, providing the interface to the connected electronics and is used to read-out the data. The PCIe40 can have up to 48 bi-directional optical links implementing the GBT protocol, can operate at 4.6 Gbps and it's able to transmit up to 100 Gbps of data through the PCIe lanes. It's equipped with Arria 10 FPGA with 1.15 million cells. Thanks to the programmable component flexibility, depending on the firmware loaded into the FPGA, the PCIe40 board can be used for different tasks: readout board (TELL40); readout supervisor (Super ODIN); controls interface (SOL40) to the connected electronics. Thanks to the large number of logic cells in the FPGA the board can be programmed to execute all the above functions, but with a reduced number of instantiated links. The integrated firmware is called MiniDAQ firmware. The MiniDAQ is a powerful tool for stand-alone development which facilitates a

distributed and de-centralized development of the different detector groups control system. The technology developed by the different detector groups using the MiniDAQ framework can easily be integrated into the final LHCb ECS and this will facilitate the commissioning of the upgraded detector in 2020/21. For this reason the MiniDAQ has been used in the development of the RICH Upgrade test-beam control system. In June 2017 the MiniDAQ v1 (MiniDAQ1) has been used, while in October both the MiniDAQ v1 and MiniDAQ v2 (MiniDAQ2) has been used in a special setup: the MiniDAQ1 has been used to read the beam trigger information and to forward them to the MiniDAQ2, while the MiniDAQ2 was used for the PDMDDB data read-out. The LHCb RICH Upgrade group was the first group in LHCb to use a functional and complete upgrade acquisition system with the MiniDAQ in a realistic environment.

7.1.3.2 Cherenkov Ring display

The DAQ GUI includes an online monitoring system developed using Java which provides readout information from the MaPMT sockets and displays it on the monitor in real time, as shown in Figure 7.4. Each pixel is an MaPMT channel, which correspond to a CLARO chip channel, and the different colours shows the number of hits in each pixel in the integrated acquisition time. However, each MaPMTs has a different hits map colour scale. A Cherenkov ring is clearly visible on the MaPMTs. When the ring is deliberately de-focused it spreads over more channels. Some pixels outside the ring Cherenkov ring are red, which means the associated CLARO channels are detecting electronic noise. That is because a common threshold has been set to all the CLARO channels and the ones which are detecting the noise have the threshold set on the pedestal. The white pixels correspond to channels which could have not been configured properly.

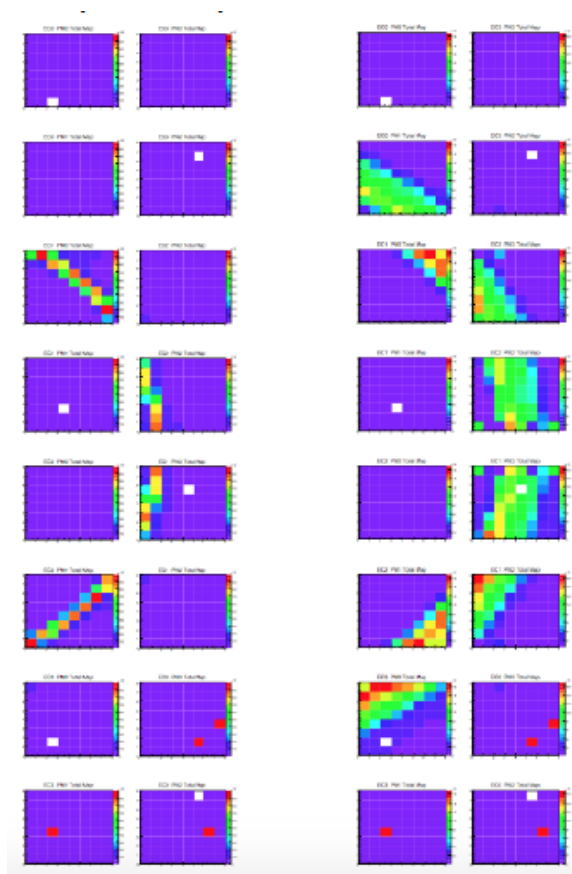


Figure 7.4: DAQ GUI used in the test beam. The Cherenkov ring is detected using the optimal optical setting on the left, while on the right it has been de-focused.

7.2 Measurements

In this section the reconstruction procedure for the Cherenkov angle and radius measurements and the CLARO characterization tests with the upgraded RICH prototype setup are presented.

7.2.1 Cherenkov ring radius and Cherenkov angle reconstruction

The study of the Cherenkov ring in the LHCb RICH Upgrade prototype is performed in two steps. The first step consists in a Monte Carlo simulation of the system using a dedicated software which replicates the geometry of the setup. In the simulation the Cherenkov photons are generated at a fixed Cherenkov angle depending on the setup geometry and on the radiator medium parameters, then a reconstruction procedure is implemented to obtain the Cherenkov angle from the simulated hits. The simulated Cherenkov angles and the reconstructed one are expected to be equal, within the uncertainties. From the reconstruction procedure it's possible to evaluate the three main Cherenkov angle contributions: the Emission Point error, the Chromatic error and the Pixel error. This last contribution arises from the different angle evaluation when considering the exact photon-hit coordinates in the MaPMT pixels (which is unknown for the real data) or the hit pixel centre. The data coming from the prototype are analyzed using the same software, after the simulation has been performed. The photon-hit map of the MaPMTs for a particular run is processed to measure the Cherenkov ring radius. For each event, that is a particle passing through the radiator and generating Cherenkov photons, the centre of the Cherenkov ring can be found by averaging over the photon-hits coordinates. Alternatively, the projection of the nominal z -axis, the beam axis, on the MaPMT plane can be considered as the centre. The Cherenkov radius is then measured taking the distance of a single photon hit from the circle center previously found. For each event a single radius value is found by averaging over all the photon hits in the event. Alternatively, the Cherenkov radius can be measured using the least-square circle fit method (Appendix B). The reconstruction procedure also provides the measurement of the Cherenkov angle. In Figure 7.5 is represented the reconstruction model used in the software. Before the data analysis is performed a simulation map is created which contains the sample of photon paths corresponding to each pixel in each MaPMT. This map provides the coordinates of the point E_T , the true Cherenkov photon emission point on the particle track, the internal reflection points T and M

in the lens, the photon exit point X and the true pixel photon hit point H on the MaPMT, together with the center P of the corresponding pixel hit by a photon for each pixel of the system. The true lens focal plane is the plane F shown in figure. Due to dimension constraint, the plane N is used instead. The fictitious plane G is the plane N translated to the true photon trajectory so that the path $X-H$ is equal to $X-K$. Using this information, the photon path projections D and K on the true focal plane F and the imaged MaPMT plane G are obtained. The point C is the actual center of curvature of the lens, E_M is the imaged Cherenkov photon emission point and E_R is the imaged radiator centre.

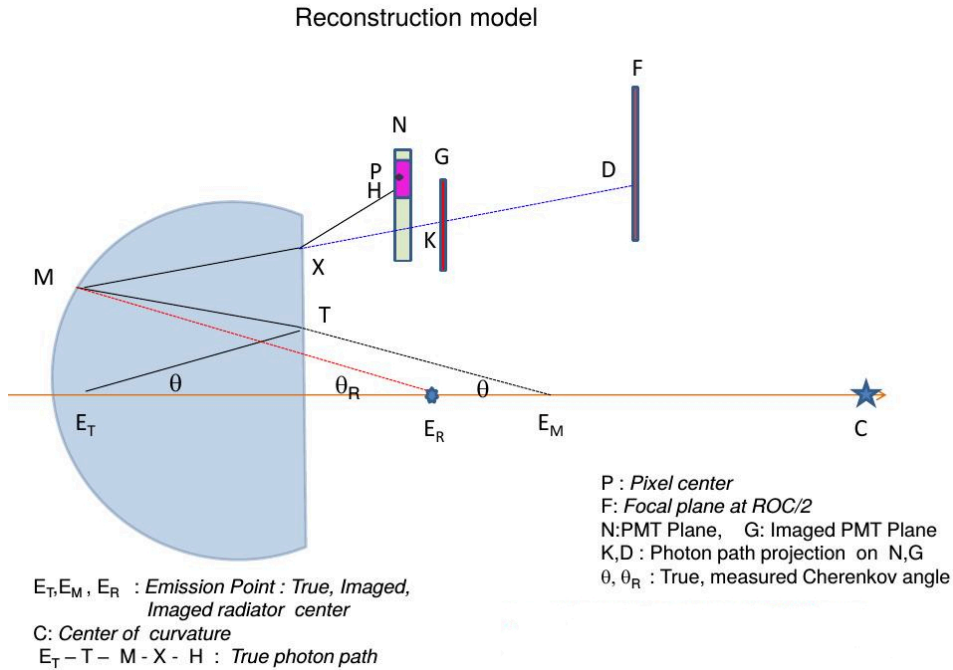


Figure 7.5: Schematic of the reconstruction geometry model used in the software to measure the Cherenkov angle from the LHCb RICH Upgrade prototype data.

The reconstruction procedure is identical for both the simulated and the real data. From the event photon hit map we obtain the point D for each pixel hit in the event. Since D, M, C and E_R are coplanar a quartic equation can be employed to obtain the point M for each photon track and consequently measure the Cherenkov angle θ_R between the beam axis and the line $M-E_R$. The true Cherenkov angle θ measurement cannot be obtained, at least for real data, because in the reconstruction process every photon is

assumed to be emitted from the center of the radiator medium, i.e. from E_R . The difference between the true and measured Cherenkov angle is accounted in the Emission Point error contribution. The Cherenkov ring radius is measured, for each photon hit, as the distance of that hit from the centre of the ring. The centre of the ring can be set to a nominal value (i.e. the z -axis) or can be evaluated using the average of the coordinates of the photon hits for each event. Alternatively, the Cherenkov ring radius can be obtained using the least square circle fit method (appendix B). The ring radius value is slightly different depending on the decision to consider the real or the imaged MaPMT plane. This is due to the refraction effect on the outgoing photons from the lens. Hence the Cherenkov ring radius measured in the real MaPMT plane is larger than the radius measured in the imaged plane. In order to obtain more realistic measurements of the Cherenkov radius and angle, a random point on the pixel hit by a Cherenkov photon can be considered instead of the pixel center, moving the points K and D accordingly.

The reconstructed Cherenkov angle is affected by the three main error sources described above, which can be evaluated using the simulated data.

The Emission Point contribution is due to the emission point approximation and to the unfocused reflected photons, since the true focal plane cannot be used and the photons are reflected onto a non-optimal (from the optical focus point of view) surface. This error contribution is evaluated by reconstructing the Cherenkov angle for Monte Carlo data using the true photon hit point (a parameter available only for the simulated data) and by setting the refractive index of the radiator lens to its average value (constant).

The Chromatic Error is due to the different wavelengths of the Cherenkov photons that experience different refractive indices in the radiator medium. To evaluate this contribution, the Cherenkov angle is reconstructed using the true hit point of the simulated data and their true emission point. Hence, the only uncertainty left can be ascribed to the chromatic contribution.

Lastly, the Cherenkov angle is reconstructed using both a random point on the pixel hit and the true hit point on the pixel and the distribution of the difference between the two measure is obtained. This error is defined as the Pixel contribution and it is used to evaluate the effect of the finite granularity of the photon detection system.

In Figure 7.6 the three distributions used to evaluate the Cherenkov angle resolution contributions are reported. In the Emission Point and in the Chromatic Error distributions a two-peak structure is visible, due to the pixel size effect being too dominant. Nonetheless, the Cherenkov angle contributions can be correctly evaluated by fitting the distributions with a

Gaussian PDF using ROOT. For each plot a stat-box is present, where several parameters are reported. The first three parameters are automatically generated by ROOT when creating an histogram: the number of data in the histogram (Entries), the histogram average value (Mean) and the data spread around it (RMS). Then the ROOT fit parameters are reported: first the reduced Chi-squared of the fit, then the three Gaussian PDF parameters with errors. In this case we have the Gaussian PDF amplitude (Constant), the average value (Mean) and the Standard Deviation (Sigma). The Standard Deviation parameter of the obtained fit function is the Cherenkov angle resolution contribution.

The Cherenkov ring radius has been measured on the image G plane using a random pixel point on the pixel hit, and the beam center has been calculated by averaging on the hit points coordinates. The obtained value from the real data is compatible to the one of the simulation. The Cherenkov ring radius has also been calculated using the least square circle fit method on the actual MaPMTs plane. The mean value for the radius in this case is bigger than the one of the previous measurement because of the refraction effect on the photons when exiting the lens. Its mean value is compatible with the one of the Monte Carlo data reconstructed Cherenkov ring radius on the actual plane. From both the simulated and the real data is possible to extract the average number of hit per event, that is the average number of emitted Cherenkov photon per particle that radiates in the lens. The values for the reconstructed Cherenkov angle, for the three Cherenkov angle contributions and for the Cherenkov radius in the different cases are reported in Table 7.1.

Measure	Real Data	MC
Cherenkov angle [rad]	0.8738 ± 0.02392	0.8787 ± 0.02387
Emission point contribution [rad]	/	0.01306
Chromatic contribution [rad]	/	0.01049
Pixel contribution [rad]	/	0.01696
Total contribution [rad]	/	0.02384
Cherenkov radius (image MaPMT plane) [mm]	57.15 ± 1.57	56.99 ± 1.46
Cherenkov radius (actual MaPMT plane) [mm]	61.05 ± 1.85	60.76 ± 1.79
Cherenkov photons per particle	33.3	32.8

Table 7.1: Cherenkov ring and angle measurements from the LHCb RICH Upgrade prototype data using the reconstruction software.

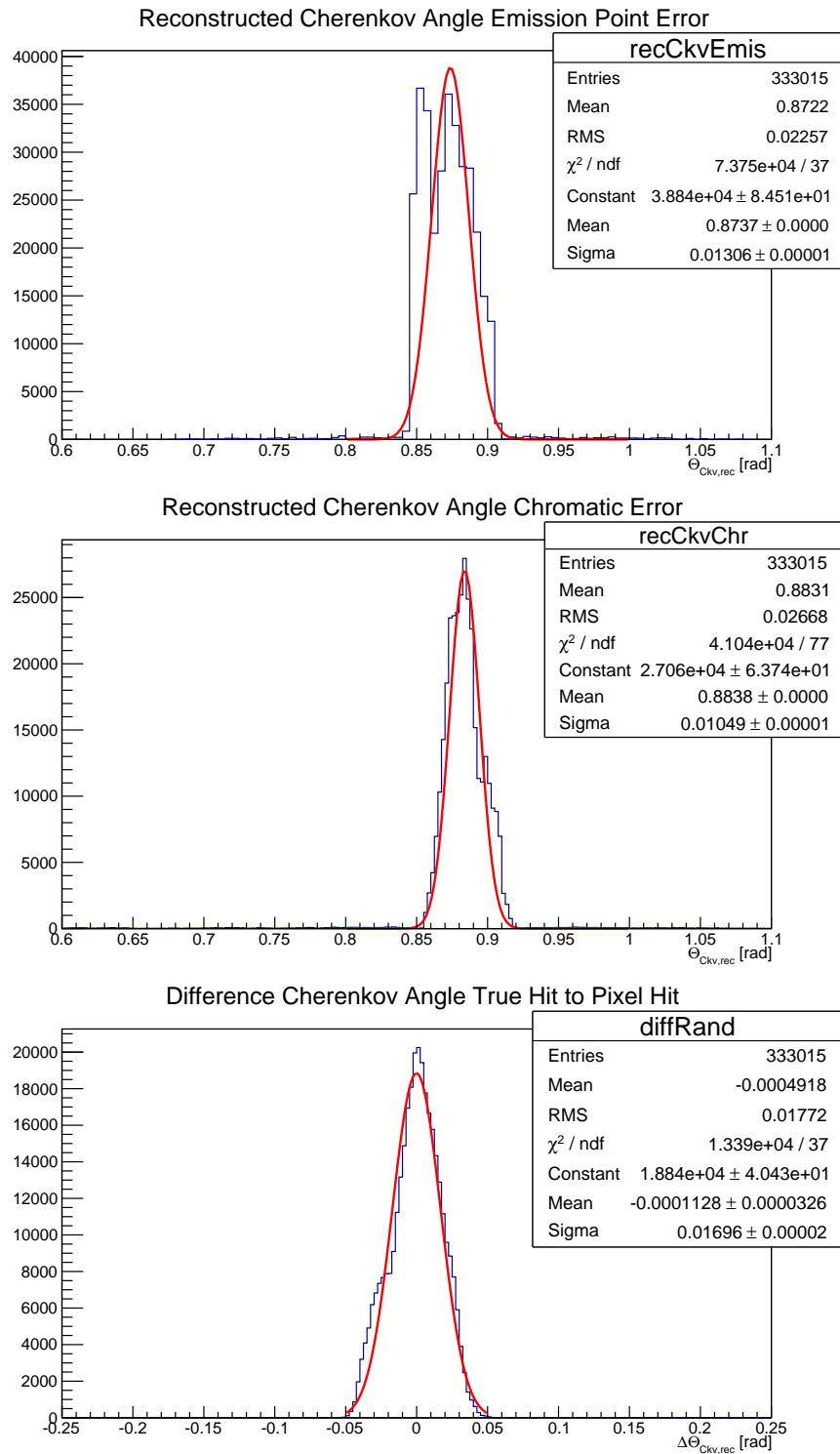


Figure 7.6: Cherenkov angle contributions obtained from the reconstruction software for the LHCb RICH Upgrade prototype.

7.2.2 Threshold scan

The Threshold Scans at the tests-beam have been performed using both the beam or a LED as a light source. The LED has been placed in the box in front of the MaPMTs, facing the wall of the box where a white sheet of paper was attached to uniformly reflect the LED photons onto the MaPMTs plane. The aim of this test is to find the optimal thresholds (or working point) for each CLARO channel in the prototype using the upgrade full opto-electronic chain in a realistic environment. The optimal threshold is the CLARO threshold at which most of the noise is cut-off and a very little portion of the true physical signal is excluded. Even though the measurement is performed in the same way with both the LED and the beam, the LED provides a uniform illumination on the MaPMTs plane and we can expect that each channel approximately register the same hits number. When using the beam the CLARO channels corresponding to the MaPMTs pixels on the Cherenkov ring will have a way bigger number of hits with respect to the others, albeit every channel will have a non-zero hits number for a long-enough Cherenkov light exposition. During the tests-beam both Threshold Scans with the beam and with the LED have been acquired, but the CLARO optimal threshold per channel has been extracted using the LED as light source to obtain uniform and high enough illumination over all the MaPMTs pixel. The Threshold Scans have been taken at the MaPMTs operative voltage of 950 V, 1000 V and 1050 V to analyze the variation of the MaPMTs gain with the voltage. The expected result is a shift of the first photoelectron peak to higher threshold values for increased voltage. Each scan starts at threshold zero and finishes at threshold 63. The threshold value is changed once the maximum number of trigger events has been collected. The number of trigger event is set in the DAQ GUI and its registered value in each run is based on the combined information coming from the VELO and the RICH trackers. For a precise study of the noise distribution (that is the pedestal), the Offset bit of the CLARO channels has been set to 1. This option performs a shift of the threshold value of -32. Only when using this option it becomes possible to obtain the detailed shape of the pedestal for every channel. For some channels a portion of the first photoelectron peak is visible as well. Without seeing the pedestal for a CLARO channel it's impossible to set the optimized threshold for that channel. In Figure 7.7 is reported a typical Threshold Scan histogram. Each bin correspond to a threshold value and its height corresponds to the number of times in which the channel has been switched on during an event (that is a trigger count). The histogram has been then normalized to the maximum number of collected events, as set on

the DAQ GUI, hence the maximum bin height becomes 1.

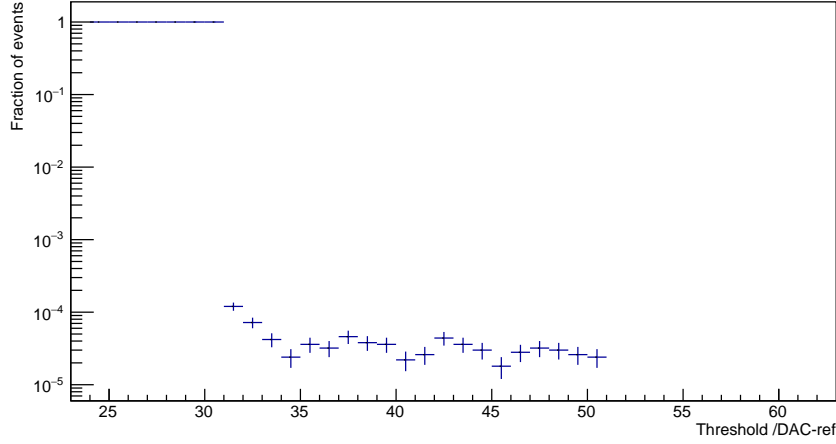


Figure 7.7: Typical threshold scan distribution obtained during the tests-beam.

The obtained threshold scan distribution is the integral form of the typical photoelectron spectrum shown in Figure 7.8. The expected distribution presents several peaks: the leftmost peak is the pedestal, generated by the electronic noise of the CLARO channel; at the right-hand-side of the pedestal there will be a peak corresponding to the signal generated by a single photoelectron emitted from the MaPMT's pixel when hit by a photon.

To obtain the parameters of the threshold scan distribution a fir procedure using ROOT on dedicated scripts has been developed. The fit function is a linear combination of Complementary Error Function (ERFC) Probability Density Functions (PDFs). The Error Function $\text{ERF}(x)$ PDF is defined in Equation (5.1) and correspond to the integral of the Gaussian PDF. The $\text{ERFC}(x)$ PDF is defined as:

$$\text{ERFC}(x) = 1 - \text{ERF}(x) = \frac{2}{\sqrt{\pi}} \int_x^{\infty} e^{-t^2} dt \quad (7.1)$$

A direct connection therefore exist between the Gaussian PDF and the $\text{ERFC}(x)$ PDF.

The PDF used to fir the Threshold Scans from tests-beam data has been built by taking into account one contribution for the pedestal and a contribution for each possible photoelectron peaks up to a maximum of three peaks. The four $\text{ERFC}(x)$ PDFs are weighted by a Poisson distribution probability coefficient proportional to the average number of photoelectrons produced in

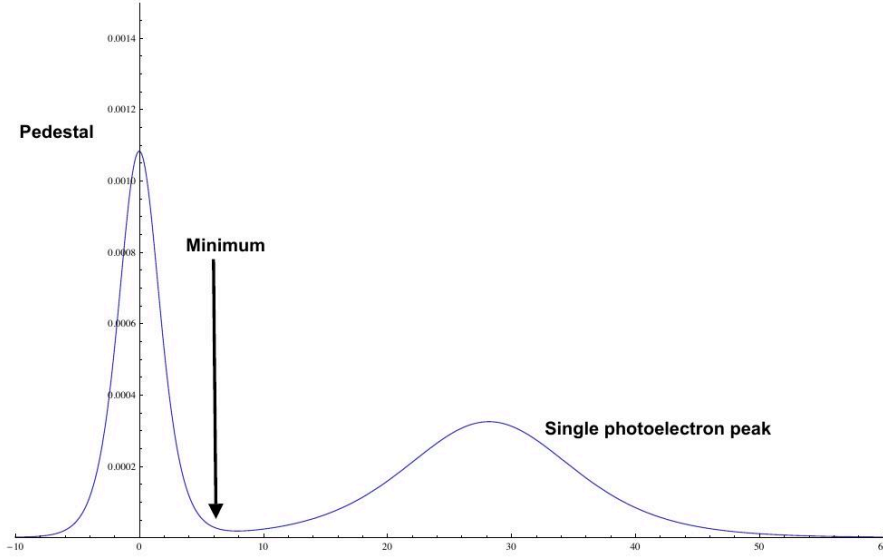


Figure 7.8: Schematic of the single photoelectron spectrum, that is the expected signal spectrum for the CLARO channels. Additional peaks can be found at higher threshold values, corresponding to multiple photoelectrons emitted per MaPMT photon hit.

the MaPMTs channels per photon hit in the entire test. The photoelectron number depends on the MaPMTs parameters like QE, cross-talk, conversion efficiency, as well as on the light source (LED) intensity. The FIT PDF equation is the following:

$$\begin{aligned} \text{FIT}_{\text{ThresholdScan}}(x) = & \frac{p6 \cdot P(0, p0)}{2} \text{ERFC} \left(\frac{x - p3}{p4} \right) \\ & + \sum_{n=1}^3 P(n, p0) \cdot \text{ERFC} \left(\frac{(x - n)p1}{p2\sqrt{n} + p5} \right), \end{aligned} \quad (7.2)$$

where $P(n, p0)$ is the Poisson probability to obtain n events given $p0$ average number of events.

The fit PDF has seven free parameters to be determined with the fit.

The parameter $p0$ is the average number of emitted photoelectron per photon hit. It has been calculated assuming a Poissonian emission probability for the photoelectrons inside the MaPMTs pixels.

The parameter $p1$ is the x -coordinate, that is the threshold, of the n -th peak transition point. The product $n \cdot p1$ is necessary to correctly fit the

multiple photoelectron peaks which are supposed to be found at constant distance $p1$ one from the others.

The parameter $p2$ is the slope of the photoelectron peaks, where the \sqrt{n} factor is considered since a bigger spread for the peak at higher signal intensity is expected.

The parameter $p3$ is the x-coordinate, that is the threshold, at which the pedestal, considered standalone, would reach half of its height. We can call this parameter the pedestal transition point, in complete analogy with an S-Curve test.

The parameter $p4$ is the pedestal slope. The sum in the equation runs on the possible number of photoelectrons emitted, up to a maximum of three.

Lastly, $p5$ and $p6$ parameters are respectively the vertical offset and the amplitude of the distribution.

The most important parameter obtained during the test is the pedestal transition point from which the channel optimized threshold can be set. However, given the complexity of the used function, the fit efficiency is less than 100% and for some channels it fails. The study of the Threshold Scan fit function is still ongoing.

A simpler analytical method to extract the channel optimized threshold is to identify the pedestal right-most edge, that is the threshold at which the distribution height goes from 1 to the user-set value <1 , then the optimized threshold is set as that value plus 5 threshold steps. The downside is that no other information on the channel spectrum is obtained from the test. This last technique is used in the EC Quality Assurance procedure that will be discussed later in the thesis.

7.2.3 S-Curve

The S-Curve test is necessary to study the behaviour of the CLARO channels and to check the expected proportionality between the applied threshold and the transition point position. The S-Curve is performed with the MaP-MTs switched off. The signal is injected in each CLARO channel from the DBs 8-bit DAC. The DAC step size is of about 16 ke^- (considering the internal capacity of the CLARO of $\sim 640 \text{ fF}$) for a total of 256 steps. The channels have a fixed threshold for each different acquisition, and acquisitions at different threshold have been taken. Per each test step the maximum number of signals, which has been set in the DAQ GUI panel, is sent to CLARO test inputs. The digital board registers the number of times that every channel has switched on for that DAC step compared to the total number of signals

injected and then increases the signal amplitude. What is expected is that the channels are more likely to be switched on as the signal amplitude increases. As a result we obtain an s-shaped signal distribution, the transition point of which can be used to adjust the optimal operative threshold of each channel. The distribution is normalized to the maximum number of signal injected per DAC step. If the threshold applied to the channel is increased, the transition point is expected to be found at higher signal amplitude. The linear response of the CLARO channel can be verified by reporting the transition point variation as a function of the channel threshold. The spread of the distribution is expected to increase as well when the threshold increases, since a higher injected signal means a higher noise in the system. In Figure 7.9 is shown the typical S-Curve distribution for a CLARO channel. The relative big error on the fit parameters is due to the very steep transition (usually one or two DAC steps) which makes it difficult to perform the fit: the distribution is more similar to a step function than to an S-Curve.

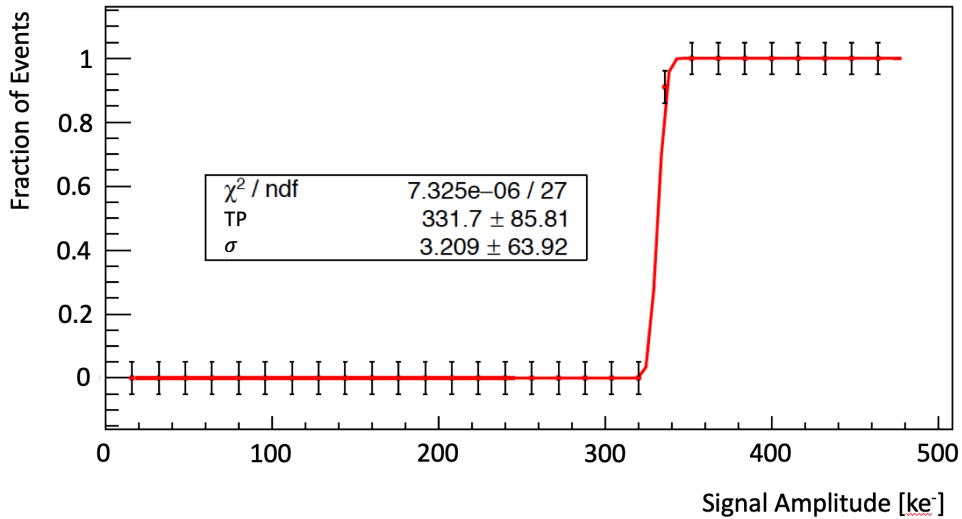


Figure 7.9: Typical S-Curve distribution obtained during the test-beam S-Curve tests.

The distribution is expected to be an S-curve, that is the integral of a Gaussian distribution. A fit technique as for the Threshold Scans can be used to extract the parameters of interest. The fit function used (red) is the translated ERF PDF reported in Equation (5.2). The error associated to each point has been evaluated to account for electronics oscillations and deviations from the expected distribution.

The S-Curve tests are performed at fixed threshold. Data at different

thresholds have been acquired to study the variation of the transition point as a function of the applied threshold. In Figure 7.10 is shown the linear behaviour of the transition point, obtained from the fit of the S-Curve at the corresponding threshold, as a function of the channel applied threshold. The error associated to each point is obtained from the fit itself. The linearity plot can be fitted with a linear function to obtain two parameters (in ke^-) per channel: the channel offset threshold, that is the fit y-axis intercept and it's named p0 on the plot, which is an intrinsic feature different per each channel; the slope of the linear fit which represent the number of ke^- per threshold step for that channel, p1 on the plot. The offset threshold is the reason why it's possible to see the pedestal only for some channels when running a threshold scan with the offset bit at 0. Two CLARO channels set at the same threshold with the same input signal amplitude might exhibit a different behaviour because the offset thresholds they have are very different from one another. It is therefore important to fully characterize the CLARO channels and register all of their parameters.

Even if the function used to obtain the S-Curve transition point and slope is simpler with respect to the Threshold Scans one, the fit may not succeed 100% of the time. This might happen for different reasons: the channel might be problematic (non monotonous distribution, the channel is dead and doesn't count, the channel is noisy and register a number of counts higher than the maximum set in the DAQ GUI...) or, as it can be seen in Figure 7.9, the distribution obtained is so steep that a correct evaluation of the parameters can't be performed. In particular, the slope is

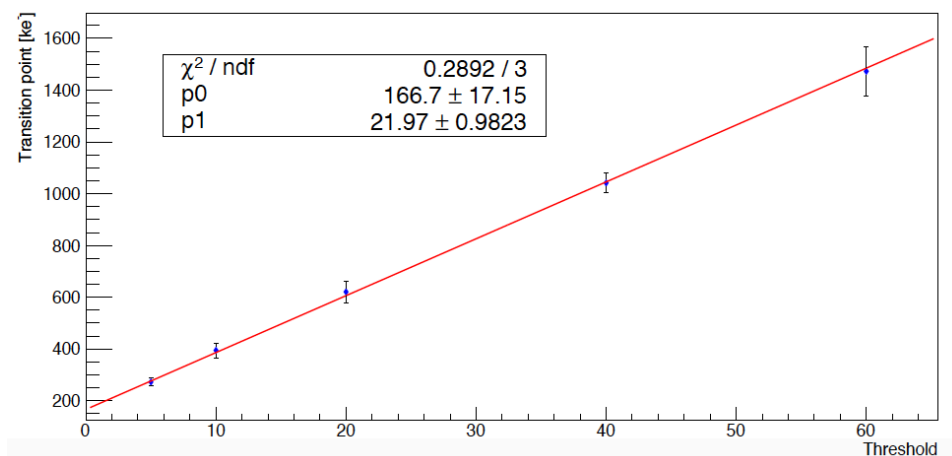


Figure 7.10: Linearity plot obtained for a CLARO channel during the tests-beam S-Curve tests.

underestimated. In the data acquired during the tests-beam all the S-Curve tests shows this feature, and that is due to the DB DAC resolution. For this reason a different evaluation method for both transition point and slope has been developed, called Pattern Recognition.

As reported in Figure 7.11, two limits are set in the S-Curve transition region. The transition point for that channel will be the x-coordinate of the point in between the last point below the lower limit and the first point above the upper limit. An upper limit for the slope is then evaluated by counting in how many DAC steps the transition happens (usually one or two DAC steps). The Pattern Recognition method is more reliable because it doesn't require to converge like a fit. The downside is that eventual problems have to be found "manually" by adding controls and exceptions to the analysis algorithm, while with the fit we can use the reduced Chi-square parameter to spot possible problematic channels.

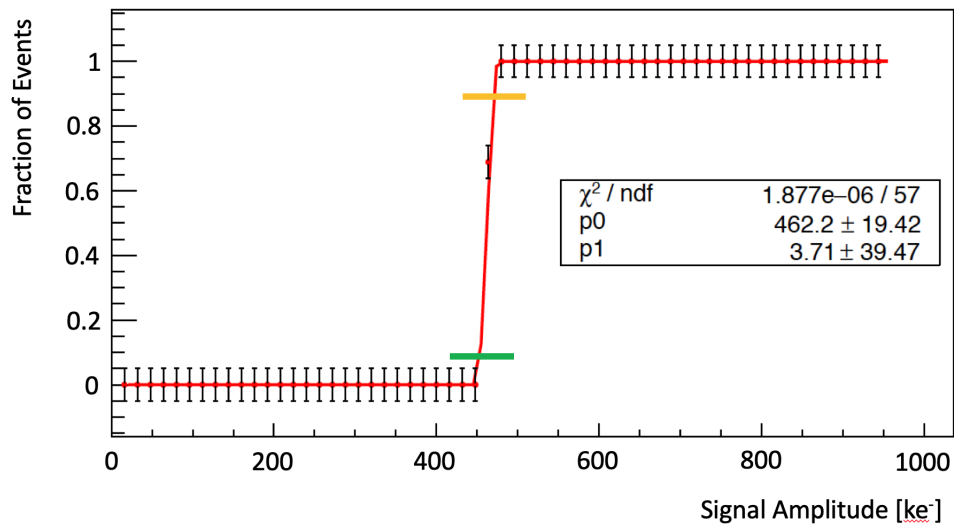
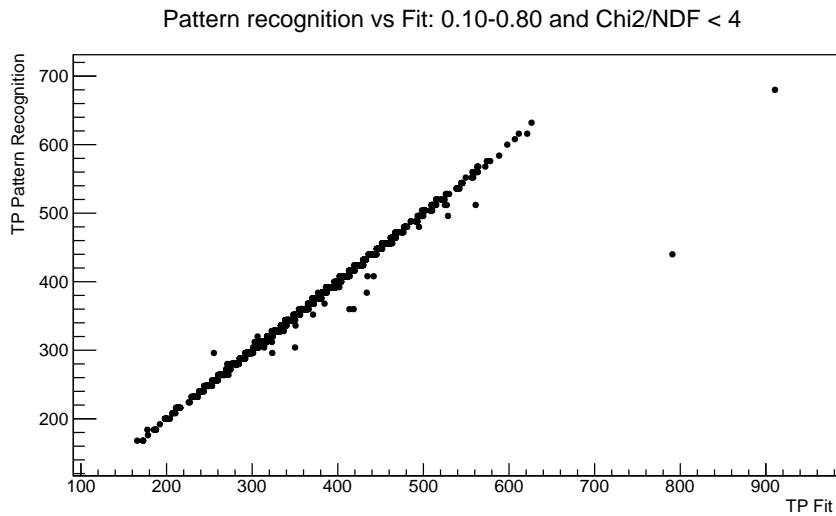


Figure 7.11: Visualization of the Pattern Recognition method, with the lower limit (green) and the upper limit (yellow).

A comparison between the transition point obtained from the fit and this method has been performed. For the Pattern Recognition method different limits have been set. Only channels for which the reduced Chi-square < 4 from the fit have been taken into account. In Figure 7.12 the transition points evaluated with the Pattern Recognition are plotted as a function of their correspondent value obtained from the fit. Two different pairs of upper and lower limits are set while the condition on the reduced Chi-square is fixed. If the transition point is found to be identical in the two methods the

obtained distribution would be a line. We can see few outlier channels in the distribution with Pattern Recognition limits 0.10-0.80 (top plot), probably being underestimated in the Pattern Recognition method with respect to the fit. When the limits are reduced to 0.20-0.70 (bottom plot) the distribution converge to a line, except for two problematic channels for which the fit failed, while the value found with the Pattern Recognition method is in the same range as the others.



Both method can be used when analyzing the S-Curves. The Pattern Recognition method is more reliable and easier when it comes to evaluate the transition points, but can't be used to correctly evaluate the S-Curve slope. Possible problematic channels can be spot by controls and exceptions handling inserted manually in the analysis algorithm. The fit gives a complete overview of the S-Curve parameters, when enough DAC resolution is available, but requires a correct initialization of the parameters to converge. The reduced Chi-square is a powerful tool to check for errors and problematic channels but an in-depth analysis of the problems is required anyway.

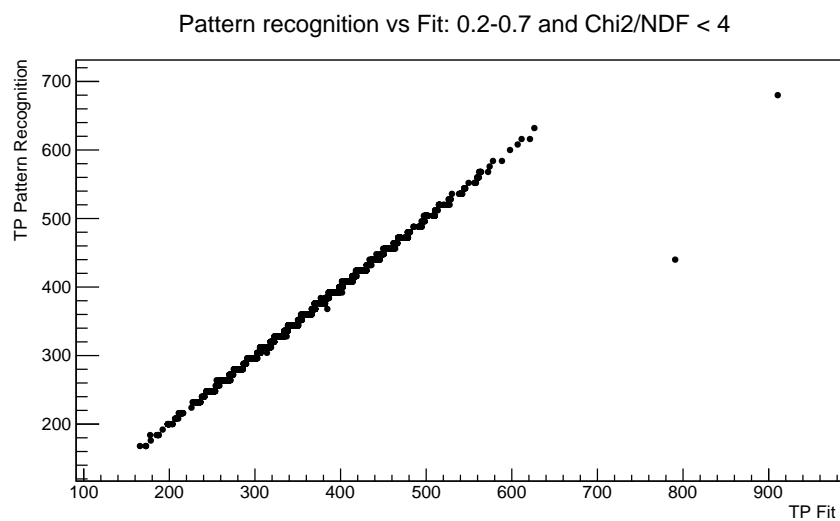


Figure 7.12: Distributions obtained for the comparison of the transition point evaluated using the Pattern Recognition and the fit. By choosing different upper and lower limit for the Pattern Recognition method the transition point value obtained can be adjusted.

Chapter 8

The LHCb RICH Upgrade Quality Assurance procedures

The Ferrara LHCb RICH Upgrade Group has been accounted responsible for the Quality Assurance procedure on the entire CLARO ASIC and FEBs production for the experiment upgrade. In addition, the group has been accounted responsible for the QA procedure on half of the ECs production for the upgrade. The Edinburgh RICH Upgrade group is responsible for the QA on the other half of the RICH EC production. For the upgrade the total number of CLARO needed is 32'000, and 40'000 have been produced taking into account spare components. After being tested with a dedicated QA procedure, the ASICs have been sent to Studioemme[®], the italian company¹ responsible for the FEBs production, where they have been soldered on the FEBs. The boards have then been tested at the company site using the QA setup and procedure developed by the Ferrara RICH Upgrade group, and then they have been sent at CERN where a random sample quality check has been performed. For the EC QA procedure the required components (MaPMTs, metal chassis, FEBs, Bkbs and Bbs) are sent to Ferrara where the ECs are assembled using a well-defined mounting protocol and then tested. The EC which pass the QA procedure are then shipped at CERN where they will be installed in the new RICH detectors.

In this chapter first the CLARO QA procedure, then the FEB QA procedure and finally the EC QA procedure will be presented in details.

¹<https://www.studioemme.it/en/>

8.1 The CLARO QA procedure

The validation of the entire CLARO production for the LHCb RICH Upgrade took place in Ferrara using two identical test stations and a dedicated test protocol.

The QA procedure is performed by a pick-and-place test station (Figure 8.1) controlled by a Windows OS based PC running the control software designed using National Instrument LabVIEW (Figure 8.2). The hardware part of the station consists of a motorized XY (horizontal plane) gantry system, model G-LSQ450B450B-T4-K0048², and a motorized linear stage used for the Z (vertical) direction, model LSM050B-T4³. Both the XY and the Z systems are produced from Zaber[®] company. The XY system is able to move for 450 mm×450 mm with an accuracy of 45 μm per movement, with accuracy of 4 μm when repeating the movement. The maximum movement speed is of 120 mm/s. The Z system can travel for 50 mm with an accuracy of 15 μm per movement, with accuracy of 4 μm when repeating the movement. The maximum movement speed is of 104 mm/s. The ASICs to be tested are placed on a tray put on the test station floor. The QA test is performed on one chip at a time. The movable stage travels to the selected chip position and pick it up using a pneumatic suction cup (produced by SMC[®], model ZPR06UNK6-06-A8⁴), releasing it on a socket designed to improve the alignment of the chip with the test socket. After being picked up again, with an improved XY alignment, the chip is released onto the test socket where the QA test is performed. The setup pressure sensor regulates the force exerted on the chips during the procedure in order to avoid any kind of damage. The test socket is housed in a custom CLARO burn-in card, an electronic board designed by the institutes INFN Ferrara, INFN Milano-Bicocca and the AGH of Krakow. The board is then read-out by an Altera MAX10 FPGA development kit board connected via ethernet to the control PC. A plastic peg has been used to keep the CLAROs under test in the correct position in the test socket. The use of the peg has been proven useful to reduce communication/contact problems between the ASICs and the burn-in card.

The test protocol has been developed in such a way that all the CLARO parameters are analyzed to spot any possible problem. During the QA test all the data acquired are recorded in a dedicated log file per chip.

²<https://www.zaber.com/products/xy-xyz-gantry-systems/G-LSQ/details/G-LSQ450B450B-T4>

³<https://www.zaber.com/products/linear-stages/LSM/details/LSM050B-T4/features>

⁴<https://uk.rs-online.com/web/p/suction-cups/2273705/>

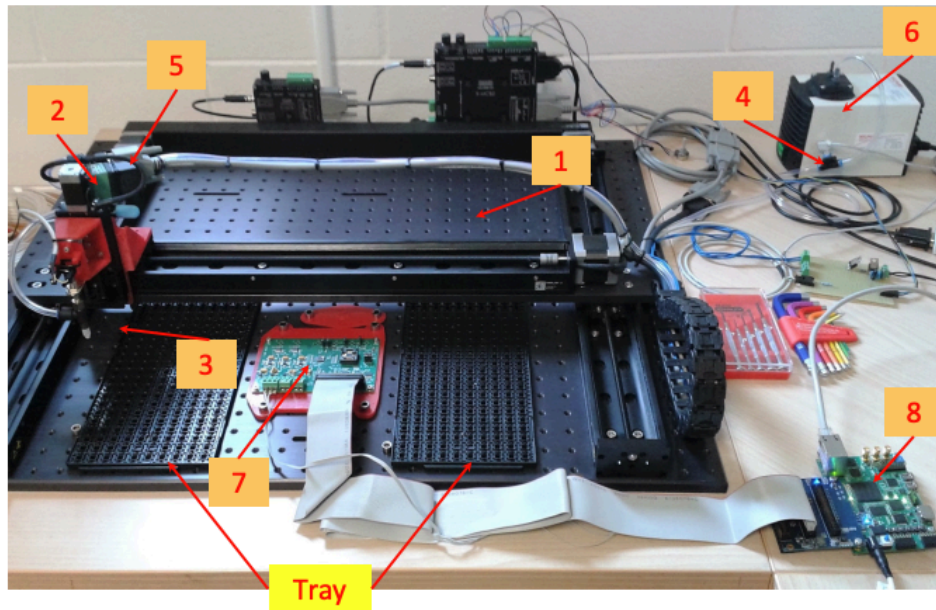


Figure 8.1: CLARO QA station (Station1) for the validation of the LHCb RICH Upgrade ASIC. The XYZ motorized system for the pick-and-place procedure (1) uses a pneumatic suction cup (2), an air compressor (6) and a pressor sensor (3) to move the CLAROs from the left-hand side tray to the test socket on the CLARO burn-in card(7). The system vacuum is regulated by a dedicated valve (4) and pump (5). The DAQ is driven by the ALTERA MAX10 FPGA development kit (8).

1. Power Up and current measurement:

right after the ASIC is put on the test socket it is powered up and the three currents (analog, digital, digital core) are measured as the average of three samples of each current acquired in two seconds. If any of the current measurements exceeds the limit threshold, set at 10mA for the analog current and 4 mA for the two digital currents, then the eight channels level out, that is the voltage measured at the channels output, is measured by taking 10 sample in 1 second, the configuration channels configuration is read-out (it should be zero for all the channels since no configuration has been sent to the channels yet) and saved. The chip is then powered off and put aside, since the test is considered failed. If the current measurements don't exceed the threshold the test can continue.

2. Configuration R/W:

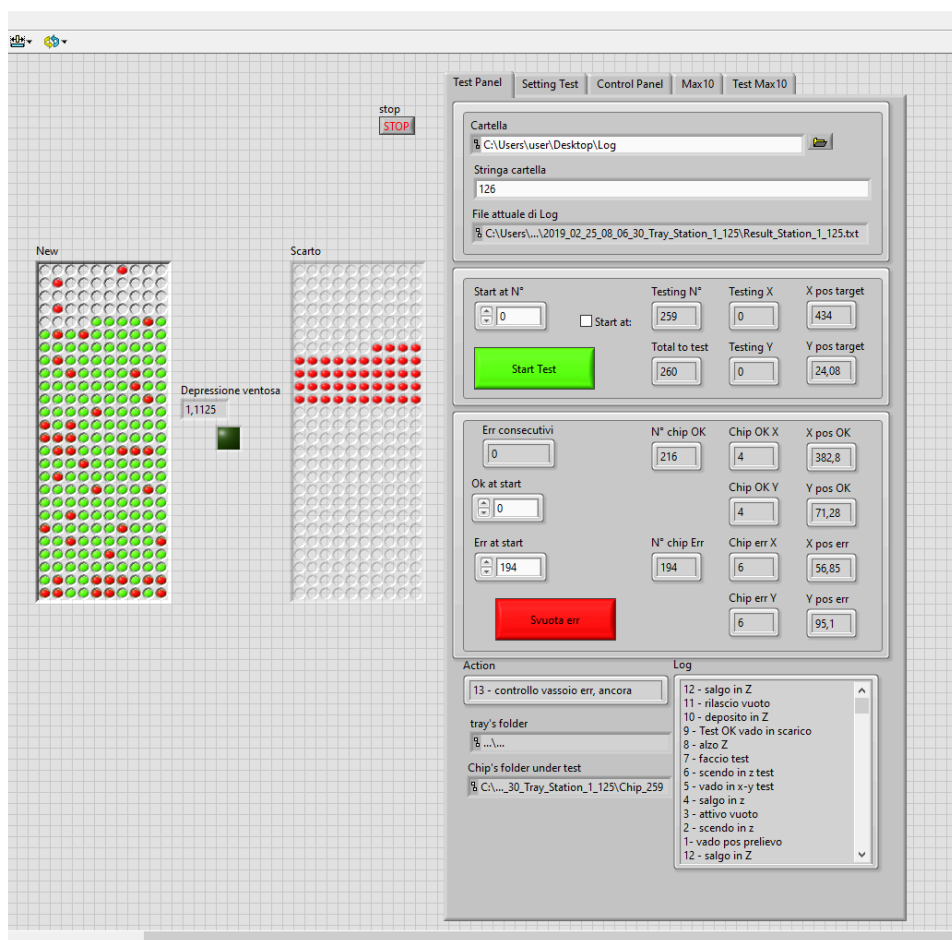


Figure 8.2: CLARO QA test software overview. On the left-hand side of the panel an overview of the current tray test is reported: the chips are picked from the left-hand side tray and the ones which don't pass the test are put in the right-hand side tray, flagged as red in both trays. On the right-hand side of the panel the control/monitor tool allows to check the status of the current test, of the actual set parameters and allows to change parameters of the test setup (XYZ system) and of the test protocol.

the chip channels configuration is read-out (as before, it is expected to be zero for all channels but the test is not considered failed if otherwise) and the first configuration is sent to all the channels. The hexadecimal configuration code used for the 12-bits of the register is 0x314. As reported in Table 5.1, this configuration enables the channel, set its Hysteresis on and its threshold at 20. Any time a WRITE command is sent to the configuration register, during the entire test, a read-back

cycle is performed and a communication error message is generated if the read-back data doesn't match the data sent in the WRITE command. If this happens the chip QA test is considered failed.

3. Current measurement:

the next step is the measurement of the three currents, using the same method and limit threshold as before. If any of them is above the corresponding threshold the chip QA test is considered failed. It is important to measure the currents again because this time the CLARO channels are configured, which means the driven current is expected to be higher than in the previous evaluation. The eight channels level out are also measured and they must be above 2.1 V for the test to continue.

4. SEU simulation:

after these measurements a Single Event Upset (SEU) simulation test is performed. During this test a fixed number of SEUs are simulated in the chip register and the CLARO SEU counter has to detect a number of SEU identical to the number of simulated events. If that is not the case the chip QA test is considered failed.

5. Pulse test:

at this stage of the test a pulse test is performed in two steps. In the first step charge is injected in all eight CLARO channels in trains of 1000 pulses. Several patterns of enabled channels are used during this phase of the QA test: first all channels are enabled with configuration 0x314; then only the channels 0, 2, 4 and 6 are enabled with configuration 0x314 while the disabled channels configuration is set to 0x23F (that is channel disabled, Hysteresis on and threshold 63); after that only the channels 1, 3, 5 and 7 are enabled with configuration 0x314 while the disabled channels configuration is set to 0x23F; lastly all channels are disabled with register configuration set at 0x214, that is channel disabled, Hysteresis on and threshold 20. These different configurations and patterns are useful to check In the second step a single pulse is sent via the dedicated CLARO *tp_input* pin with all the CLARO channels enabled. A rising edge of the CMOS 2.5V signal connected to this pin triggers the injection of charge at the input of the enabled channels. The test is considered passed if all CLARO channels register the correct number of pulses sent (0 if the channel is disabled). The chip QA test is considered failed otherwise.

6. POR test:

a Power-On Reset (POR) cycle is performed through SPI. The POR generator has been designed to reset the flip flops of the TMR protected part of the configuration registers. After the action is completed the configuration is read-back and, if not all CLARO channels have configuration at 0, the chip QA test is considered not passed.

7. S-Curve test:

the QA test continues with the S-Curve test. The test is performed for only one channel at a time, set at threshold 20, while all the other channels are disabled. 1001 pulses are sent to the CLARO channel per each DAC step, ranging from 0 to 1000 (0-1000 mV) with 1 mV step and 0.5 pF input capacitance. However, the range on which the channel transition point has to be found is reduced to the values 100-280 mV. This range has been set since the majority of the channel transition points is found between these two values, as shown in the CLARO QA data analysis section. Channels with a transition point out of this range would contribute to inhomogenize the CLARO production performances. The algorithm to find the S-Curve parameters has 3 steps: first a binary search is performed in the range 100-280 mV to search a number of hit count different from 0 and 1001; starting from that value a fine scan is performed, decreasing the DAC value in steps of 2 mV until the output count is found to be 0 for two consecutive steps; lastly the scan is performed as above but increasing the DAC value in step of 2 mV, searching 1001 pulses. The S-Curve test is considered passed if the transition point found on that channel, obtained by fitting the distribution using a LabView routine, is between 100 and 280 mV, and then a file is generated containing the DAC values and the hitcounts in the fine scan range together with the transition point and slope (also obtained by the fit) values of the channel.

8. Offset scan test:

the next step is the Offset scan test, used to evaluate the optimal threshold for the CLARO channels by detecting the electronic noise pedestal. It's equivalent to a Threshold Scan but without the MaPMT signals. The test is performed on one channel at time. The DAC value fixed at 1280 mV but no signal is injected in the CLARO channel. The procedure is the following: one channel at a time is enabled, Hysteresis on, configured with Offset bit 1 and threshold 37 (0xB25 in hexadecimal) while the other channels are disabled (0x23F as be-

fore). The threshold of the channel under test is lowered (in steps of 1 threshold) until the output of the CLARO channel goes into saturation (hitcount read is FFFF). That threshold is defined as the Offset threshold for the channel. The Offset scan test is considered passed if the point of saturation is between 37 and 23 threshold value. At this point, if no errors occurred, the test is finished and the chip is placed in the tray it came from.

If during a chip test an error of any kind occurs (some value is over the limit threshold, or a test fails) the test is performed again on the chip from the start, and this can be repeated other two times. The CLARO chip is not moved by the pick-and-place robot arm between the tests, but it is released and re-pressed on by the plastic peg which is keeping it in position. If the CLARO chip fails the test for 3 consecutive times it is moved to a second tray, named error tray, placed next to the first tray, and it will be fully tested again up to a maximum of two times. The time needed to perform the full test sequence is: 10 s for power on sequence and pulse testing, 8 x 10 s to perform the S-Curve test, 10 s for the Offset scan and 60 s for all the movements and the alignment procedure, for a total of 160 seconds if no errors occur.

8.1.1 CLARO QA data analysis

Before starting the CLARO QA procedure an analysis has been performed to validate the two test stations and to ensure that the results coming from one station are comparable to the other station results. A tray with 180 chips has been tested using the QA procedure in both stations and the results have been compared. In Figure 8.3 are reported the transition point distributions for the two stations. The number of entry is the number of tested channels. The parameters Mean and Std Dev in the stat-box are given by ROOT when creating the histogram. The parameters Overflow and Underflow are calculated by ROOT and they simply are the number of data out of the histogram x-axis limits, respectively over the maximum or above the minimum histogram x value. These parameters are useful to check that all the analyzed data are reported in the histogram. Some CLARO channels were problematic during the test in one of the two stations, and only the channels which have been correctly tested on both stations are reported in the distributions. The average value for the transition point is almost identical in the two stations, while on the station named Station2 the distribution presents a slightly bigger width due to about ten outlier channels.

However, except for those channels, all the transition points are in the limit 100-280 in the DAC ref. scale which correspond to 100-280 mV, hence the threshold imposed in the QA procedure. A similar plot can be obtained also for the S-Curve spread, or sigma (Figure 8.4). This last distribution suggests that for a tens of channels in Station2 the measured electronic noise is slightly higher with respect to the noise in Station1. However the transition point is correctly evaluated also for the channels with an higher sigma, and no selection criteria is applied on the channel noise during the QA procedure.

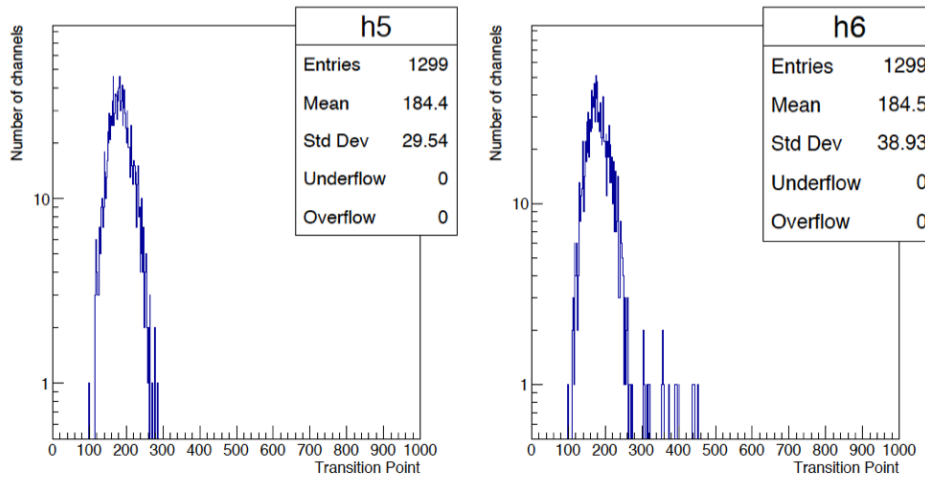


Figure 8.3: Pre-QA data analysis on the CLARO chips, transition point distribution obtained using C++ ROOT script. Left: Station1 data. Right: Station2 data.

The S-Curve transition points and the sigmas reported in these plots are obtained by a dedicated analysis C++ script with CERN ROOT, which fits the S-Curve distributions using the function (5.2) reported in Section 5.1.2.1. The same plots can be obtained using the LabVIEW routine implemented in the CLARO QA procedure (Figure 8.5 and Figure 8.6). This type of analysis has been performed to ensure that the LabVIEW routine is correctly evaluating the S-Curve parameters by comparing it to an analysis tool of well-known efficiency that is ROOT. The distribution obtained using the LabVIEW report the exact same MEAN value for the transition point with a difference of $\sim 0.3\%/4\%$ on the distribution spread for Station1/2. We can therefore use the LabVIEW routine for the S-Curve parameters extrapolation.

The results coming from the two CLARO QA test stations have been considered comparable, hence the QA procedure has been performed using them both.

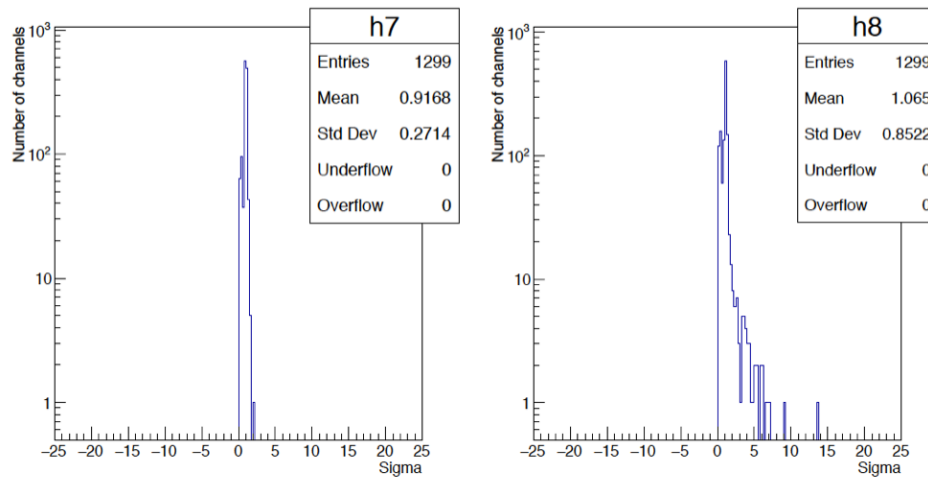


Figure 8.4: Pre-QA data analysis on the CLARO chips, sigma distribution obtained using C++ ROOT script. Left: Station1 data. Right: Station2 data.

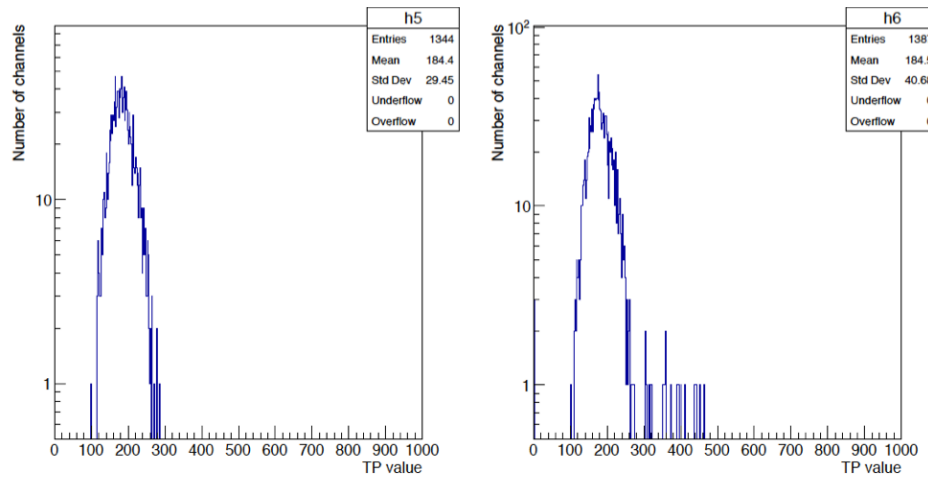


Figure 8.5: Pre-QA data analysis on the CLARO chips, transition point distribution obtained using LabVIEW routine. The results are almost identical with respect to the C++ ROOT script analysis. Left: Station1 data. Right: Station2 data.

A detailed analysis has been performed on 9044 CLARO ASICs tested using the QA procedure. In Figure 8.7 are reported the transition point and sigma results from the analysis of the chips, which have been correctly tested at the first try during the procedure. In the transition point distribution (left-

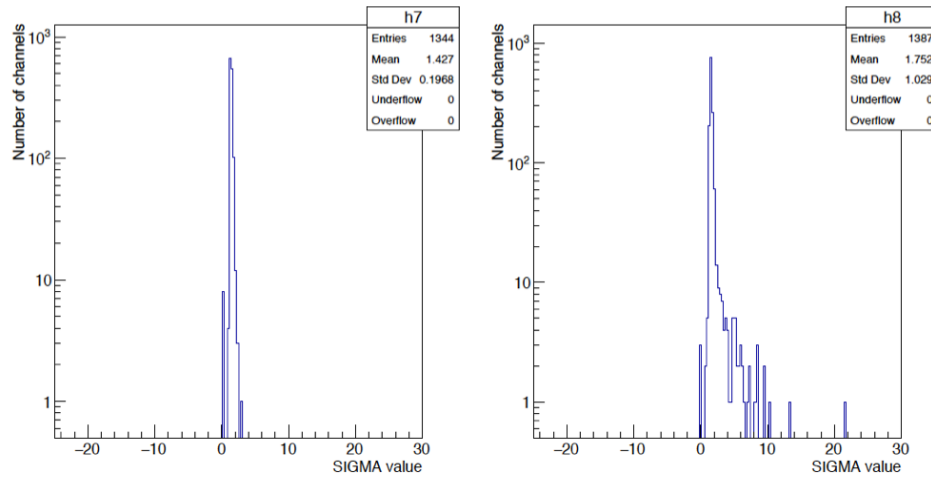


Figure 8.6: Pre-QA data analysis on the CLARO chips, sigma distribution obtained using LabVIEW routine. Left: Station1 data. Right: Station2 data.

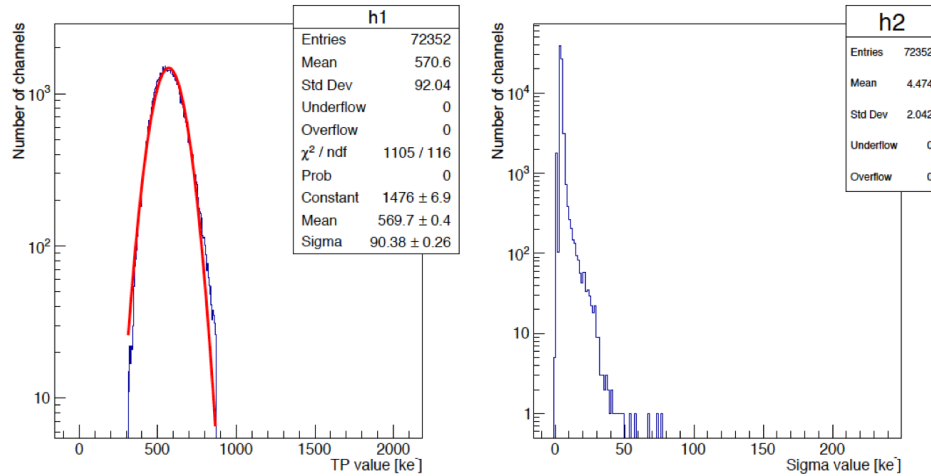


Figure 8.7: CLARO QA data analysis on 9044 CLARO chips tested using the QA procedure. Left: transition point distribution, which has been fitted with a Gaussian PDF to extract the average value. Right: sigma distribution.

hand side) we can see the cut edges at the 100-280 mV limits, or, in charge, $\sim 312\text{-}874 \text{ ke}^-$. It is important to notice that all the chips which failed the QA tests have been tested again up to a maximum of two times in case they continue to fail the test. The re-tests are performed days later one from another. This procedure has been applied to avoid the discard of good chips

which fail the test because of causes independent from the chips (e.g. dust on the test socket or natural parameters oscillations). In numbers, 75.61% of the CLARO chips have passed the QA test on the first try and 58.54% of the retested chips passed the QA test after a single re-test. Therefore after a single re-test iteration the good chips yield is of 89.89%. The final CLARO chip yield is close to 95% when considering two retest iterations.

8.2 The Front-End Board QA procedure

The CLAROs passing the QA procedure are assembled on the FEBs, which are the components used in the LHCb RICH Upgrade ECs. The FEBs produced are validated using a test setup developed by the Ferrara RICH Upgrade group before being assembled in the ECs. The FEBs are inserted in the Bkbs, which are then plugged into the test setup socket. The test setup (Figure 8.8) consists of four DBs, each one hosting two ALTERA MAX10 FPGAs. This type of DB is also used in the EC QA procedure, explained in the next section. Each FPGA controls two FEBs, hence up to four Bkbs (16/8 FEBs depending if the Bkbs are R/H-type) can be tested at once. The DBs are equipped with a 12-bit, 8-channels ADC per FPGA used to monitor the total current in the two corresponding FEBs, the temperatures of the two FEBs, of the Bkb and, once the ECs is assembled, of the Bb, and lastly to monitor the `vdd_core` tension (CLARO power tension) of all the CLAROs per each FEB.

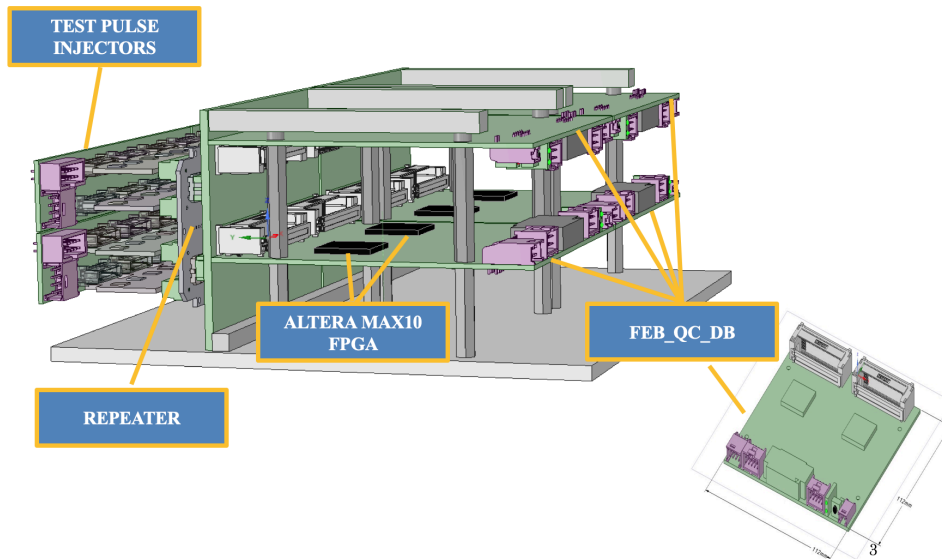


Figure 8.8: 3D model of the FEB QA setup with all its components. The repeaters are connectors used to avoid the deterioration of the DB connectors. On the left-hand side of the figure the DB measures are reported.

The communication between the FEBs and the MAX10 FPGA is performed via SPI protocol through the Bkb. A system controller works as the main controller for two DBs using high-speed mezzanine card connectors (HSMC) and an external cable-adaptor board. The system controller,

based on Cyclone V GT FPGA development board (5CGTFD9E5F35C7N, 1152-pin FBGA) is connected to the Host PC via Gbit Ethernet interface. The DB dialog with the system controller through an interconnection UART module. UART (Universal Asynchronous Receiver/Transmitter) is a physical circuit in a microcontroller which main purpose is to transmit and receive serial data. Each DB is equipped with two UART module, one per FPGA. Lastly, to perform S-Curve tests on the FEBs, a custom board called Test Pulse Injector (TPI) has been designed to feed signal into the CLARO channels. A single TPI board provides signal for four FEBs on two half Bkbs, as shown in Figure 8.9. It's possible to control the setup from the PC using dedicated python scripts which send the appropriate commands to perform each action. Three identical setup have been produced and distributed: one is in Ferrara, one at CERN and one at the production site, Studioemme[®] company. The CLAROs are sent from Ferrara to the company which solder them on the FEBs and produces also the Bkbs. Then the FEBs assembled on the Bkbs are tested using the setup provided by the Ferrara group. The valid ones are sent to CERN where a random sample check is performed.

All the FEBs main parameters are examined during the QA test by following a dedicated test protocol.

1. Power Up:

in the first test step the CLARO chips are switched on.

2. STATUS_1:

the FEBs current (measured for the FEBs couple for that UART), the temperatures and the VDD tensions (which is the CLAROs operative tension) are read-out by the DB ADC and the values are registered. The typical value for the CLARO VDD is 850 mV, while the typical value for the FEB currents with non-configured CLAROs is ~ 3 mA, increasing to ~ 30 mA when the CLAROs are configured. Higher values for these parameters trigger errors and the test is not passed.

3. CONFIG:

the third step is necessary to check that all the CLAROs are correctly configurable. The configuration 0x314 (threshold 20, channel enabled and Hysteresis on) is sent to each channel and then the channel configuration is read back to check that it has been correctly configured. In addition, a reset is sent to the nPOR pin of all CLAROs to reset the chip channels configuration, after which a read back of the channels

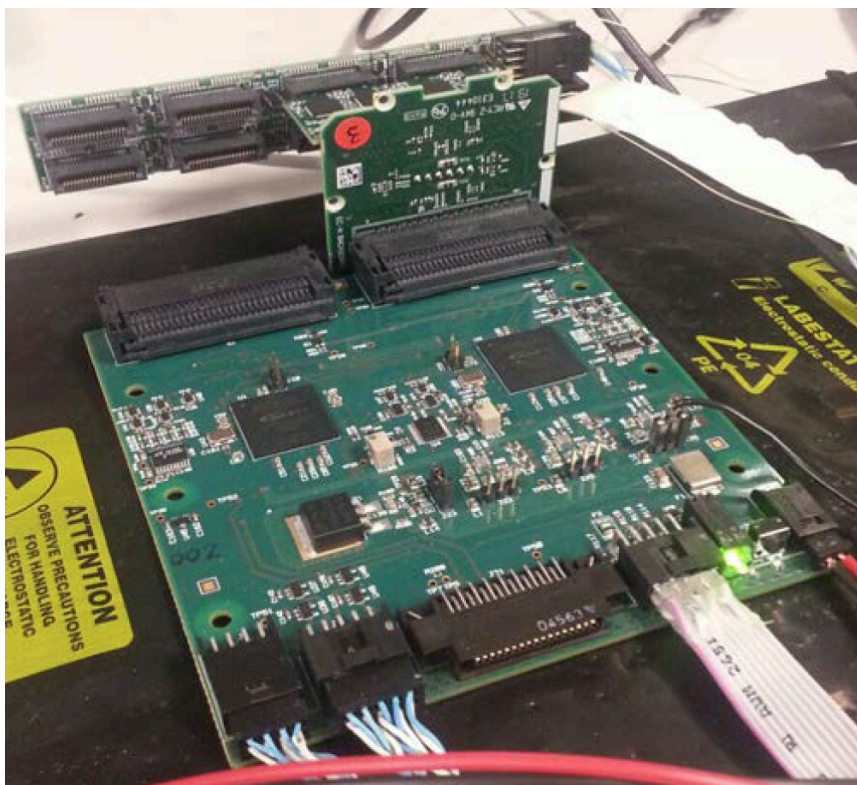


Figure 8.9: A digital board used in the FEB QA procedure. A Bkb with a FEB is connected to the FPGA UART connector on the right-hand side of the picture, and the TPI is attached to the FEB.

configuration is performed to check that the reset has worked correctly. If not, the test is not passed.

4. STATUS_2:

the fourth step performs the same actions as STATUS_1.

5. S-Curve test:

an S-Curve test is performed, in two parts, in parallel on all the MAX10 FPGA on up to 8 FEBs. A single chip per FEB is tested so that a maximum of 8 chips at a time are tested. First the signal is injected only in the even channels of the selected CLARO (S_CURVE_EVEN). The injection is performed through the even input pins and the value of the hitcounts through all of the CLARO channels output pins is read out. 1000 pulses are sent for each DAC step in the range 0x000-0x0F8 (0-300 mV, where 300 mV corresponds to approximately 2 Me⁻ injected

with a 1pF input capacitance) with a step size of 0x002 (~ 2.4 mV). A fit using the error function PDF is performed on the obtained S-Curve distribution. Warning messages are generated by the data processing function if the counts on the first DAC step are not 0 and/or on the last step are not 1000, or if the fit fails. However, these warnings do not stop the execution of the test but they are used to determine the outcome of the acceptance test. The transition points of the S-Curves for each active CLARO channel are registered in an output summary file. During this part of the test, the presence of crosstalk is verified by monitoring the odd channel hitcounts, which have to be zero. The S-Curve test, with the same parameters, is then performed on the odd channels. If one or more channels don't have the transition the test is considered not passed.

6. S_CURVE_TP:

an S-Curve test is performed on 8 channels at a time by injecting signal in them using the TP_IN pin, on the Bkb side, and then reading out the value of their hitcounts. A total of 1000 pulses per DAC step are sent. All the channels are configured with configuration 0x314, the signal is injected in the range 0x03C-0x192 (72-500 mV) with a DAC step of 0x002 (~ 2.4 mV). If one or more channels don't have the transition the test is considered not passed.

7. SEU simulation:

a SEU simulation test is then performed, where a fixed number of events is simulated in each chip and a check is performed to verify that the CLARO internal SEU counter correctly registered them.

8. STATUS_3:

equal to STATUS_1 and STATUS_2 but with the channels configured. The FEBs current is expected to higher at this stage of the test with respect to the first step.

The required time to test four Bkbs is 15 minutes. This time is independent on the Bkb type, R or H, and on the correspondent number of FEBs tested because the test parallelization is on the eight FPGAs.

A dedicated analysis has been performed on the S-Curve data coming from 36 of the first produced FEBs. For the test a 10-bit DAC, with a 1pF injection capacitor, as been used. Four type of S-Curve, named A,B,C and D, have been performed on each chip with different enabled channels

combination and different range and resolution of the injected signal: the A/B S-Curves are defined as a coarse scan, where 1000 pulses have been injected in the range 0x000-0x0F8 with a DAC step of 0x008 (0-1.2V, DAC step 40 mV), while C/D are defined as fine scan with 1000 pulses and signal range 0x001-0x030 with DAC step 0x002 (5-234 mV and DAC step 10 mV). All channels are enabled during the test but on A/C S-Curves the signal is injected only in odd channels while on B/D S-Curves the signal is injected in the even channels. The transition point distributions obtained for the CLARO channels of these FEBs in both fine and coarse scans are reported in Figure 8.10. In the coarse scan distribution (left) it's possible to see that the number of entries, i.e. of channel transition points, corresponds to almost 37 FEBs and not 36. This effect is due to the crosstalk between a odd and an even channel: only one of the two is pulsed at a time but if the signal injected has a very high amplitude, as in happens at the end of the coarse S-Curves, the signal propagates in the non-pulsed channel and a transition point is registered even if it should not. If the signal injected has a lower intensity, as in the fine S-Curves, the number of detected transition points is the nominal one. A fit using a gaussian PDF has been performed to extract the average transition point and to compare it with the CLARO QA value. The results are reported in Table 8.1. While the transition point value difference is of the order of 1% in the two tests, the distribution spread on the FEB QA results is 15% larger with respect to the CLARO QA tests, probably because of small differences in the signal injection parameters.

Test	Transition average value [ke^-]
CLARO QA	569.7 ± 90.4
FEB QA	576.9 ± 106.3

Table 8.1: Average transition point value comparison between the CLARO QA and the FEB QA results.

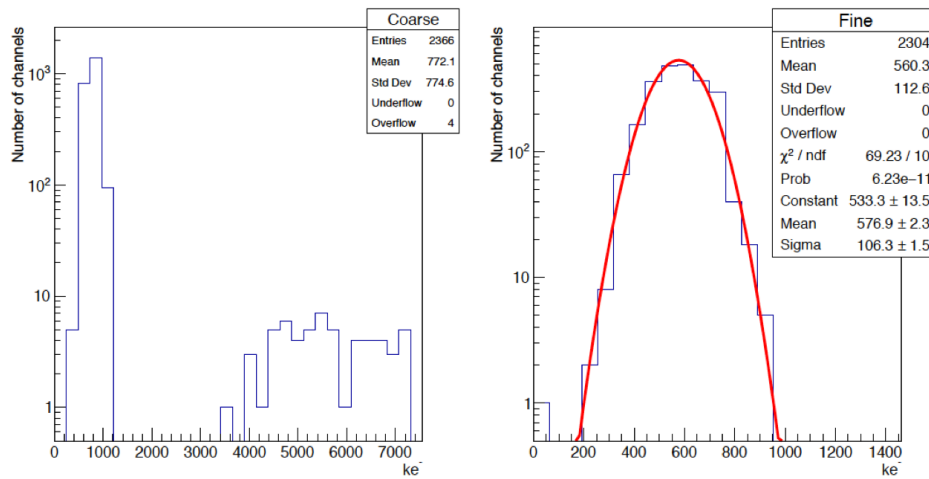


Figure 8.10: Results from the S-Curve data of 36 of the first produced FEBs for the LHCb RICH Upgrade. Left: coarse scan results, where the crosstalk is happening. Right: fine scan results. The transition point for a malfunctioning channel was close to zero, as it can be seen in the left corner of the right-hand plot.

8.3 The Elementary Cell QA procedure

The EC is the main component for the LHCb RICH Upgrade. It consists of the MaPMTs (4/1 R/H-type), of several electronic components (the FEBs, the Bb, where the MaPMTs are housed, interfacing them with the CLAROs, the Bkb interfacing the CLAROs with the DBs) and an aluminum case to contain them. Each electronic component of the EC and the MaPMTs are labeled using an adhesive QR code containing an ID code for that component. The electronic components and the case are assembled together following a well-established assembling procedure. After being assembled the QA test is performed on the EC to validate it. If the EC pass the test it is sent to CERN to be installed on the new RICH detector. The ECQA is performed using two identical test stations in both Ferrara (Station ID 1 and 2) and Edinburgh (Station ID 3 and 4). Each test station consists of a light-tight box (dark box) in which the ECs are mounted during the test. It has to be light-tight since the MaPMTs are switched on during the procedure. Inside the box up to four ECs can be mounted at the same time, as shown in Figure 8.11. They are connected to the same setup used for the FEB QA procedure (four DBs, eight UART connectors, a system controller placed outside of the box), which has been installed on the middle wall of the box. This wall stops possible photons coming from the service holes in the back of the box from reaching the MaPMTs placed on the other side of it. However, light is injected inside the box, in a controlled way, using an LED driver placed outside of it to perform tests with the MaPMTs. Four optic fibers are connected to the LED driver, entering the box and ending in the area of the box in which the ECs are mounted, facing the box wall. A mirror is mounted on that wall, so that the photons injected trough the fibers are reflected by the mirror onto the EC MaPMTs. The MaPMTs are connected to the high voltage (HV) crate, ISEG ECH 242⁵ equipped with an ISEG crate controller model CC24 Master⁶ and two 8-channels HV power supply ISEG boards EHS 8020n_SHV⁷. A single crate is used in each test location to pilot the HV for the two test stations. A load of 4 ECs uses 4 channels of the HV board, one per each Bb. The MaPMTs are air-cooled by a fan system providing a continue airflow: air flows in the vertical direction directly onto the MaPMTs and on the Bbs from the lower part of the box, being then aspirated from the upper side of the box just right-after it passes the MaPMTs. The cooling is also provided for the DBs. The fans, together with the DBs, are powered

⁵https://iseg-hv.com/files/media/iseg_manual_ECH24x_en_20.pdf

⁶https://iseg-hv.com/files/media/iseg_manual_CC2x_en_14.pdf

⁷<https://iseg-hv.com/en/products/detail/EHS>

by a low voltage (LV) power supply, Aim TTi EX354RT⁸, placed outside the box. The environmental temperature and humidity are monitored using a Raspberry Pi system which creates a log file on which the environmental parameters are registered every 10 seconds. The entire system is controlled by a CENTOS7 OS PC running a DAQ control software designed in National Instrument LabVIEW 2017 64-bit.

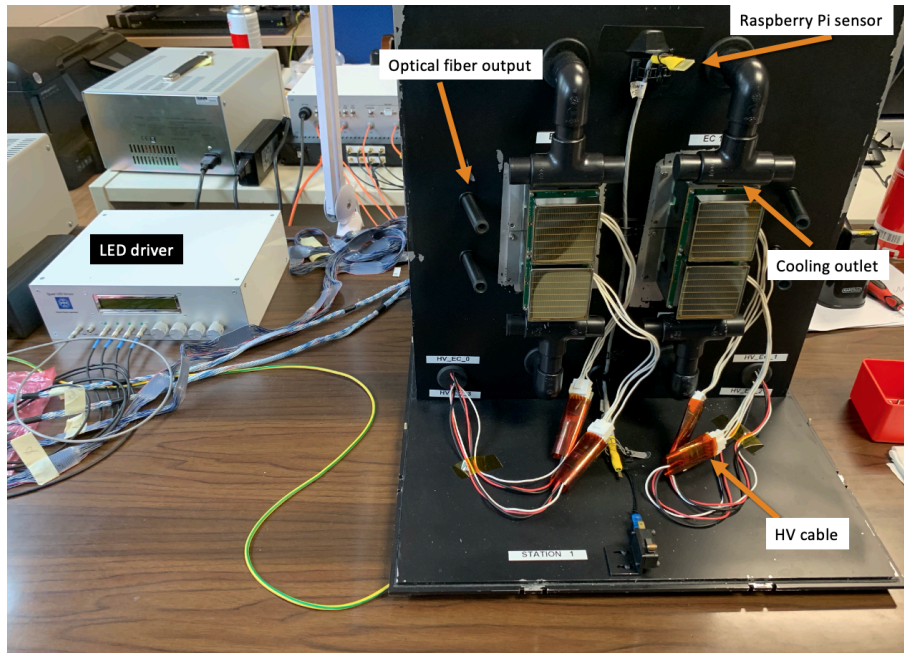


Figure 8.11: Picture of the ECQA setup, Station1, where four EC H-type are mounted in the box. On the left, the LED driver is visible.

In Figure 8.12 the numbering scheme for the ECQA setup is reported, while in Figure 8.13 the numbering scheme of the CLAROs on the FEB is reported. The QR code of the FEB is always placed on the CLARO 7.

Every set of ECs tested in the box is called "Load" and a four-digit sequential Load Number is associate to it. The Load Number sequence is separate for each of the four stations. Up to four ECs of the same type can be tested in the same load (to test a full four-ECs load is preferable to an incomplete load, for testing-time efficiency) and the QA data are saved in a load-specific folder, the name of which also specify the test station used and the type of EC tested (e.g. Load_0000_R_S1 is the folder for the Load Number 0000 of R-type EC tested on the station 1, which is in Ferrara). When mounted in the dark-box, the ECs are numbered from 0 to 3 based on

⁸<https://www.aimtti.com/product-category/dc-power-supplies/aim-ex-rseries>

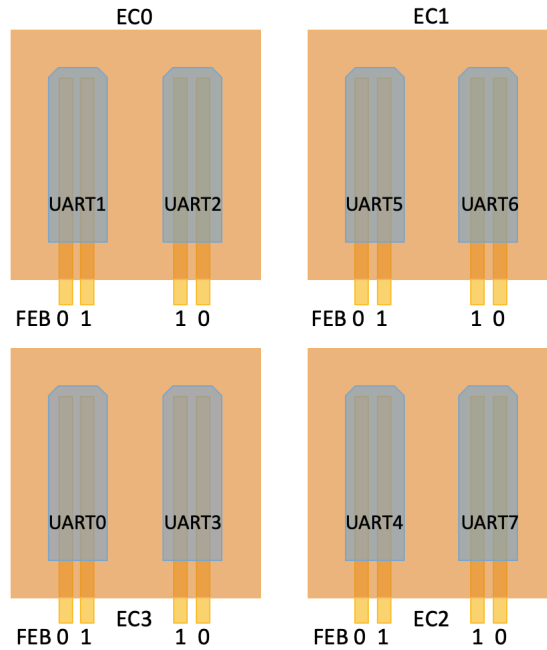


Figure 8.12: Schematic of the numbering scheme for the ECQA main components. The ECs of the load are numbered from 0 to 3 starting from the top-left going clockwise, the UART are named from 0 to 7 and each one of them is connected to two FEBs, 0 and 1, the numbering of which is inverted for UART connectors rotated of 180° one respect to the others.

their position, from the top-left going clockwise. The MaPMTs of an R-type EC are also identified based on their position, from A to D or from 0 to 3 starting from the top-left one going clockwise. For an H-type MaPMT this identification is not needed.

Inside the load folder two subfolders are present: QR_Codes and PDF. In the QR_Codes folder a file per each EC of the load is generated containing all the service and hardware info of the cell. This file is created during the assembling procedure when scanning the components QR codes. First date, time and location of the assembling are reported, together with the name of the person assembling the EC. Then the QR codes of Baseboard, FEBs and Backboard are written, after which the Load Number, the Station ID and the EC position in that Load are reported. Lastly, the QR codes of the MaPMTs are written. In the PDF folder all the plots produced during the data analysis are stored, and they are checked by the users to control no errors are present. In every data file generated the date and time of the test is registered, together with the most relevant setup settings used for the test

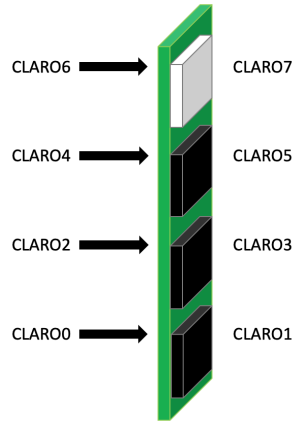


Figure 8.13: Scheme representing the numbering convention for the CLAROs on the FEB. Since it is in perspective, half of the CLAROs are hidden in the scheme but they are soldered on the FEB in a specular way with respect to the visible ones. On the CLARO7 the QR code is present.

after which the data file has been created.

Before describing the ECQA test protocol, the Signal Induced Noise (SIN) test measurement will be described.

8.3.1 Signal Induced Noise measurements and LED driver calibration

The MaPMTs produced for the LHCb RICH Upgrade are affected by after-pulses, named SIN. This effect is more evident in the anodes numbered 1-8 and 57-64, following the scheme reported in Figure 8.14, and almost absent in the central anodes. To evaluate the after-pulse magnitude a dedicated test has been developed and implemented in the ECQA procedure. This test can be performed on the full ECs load. The MaPMT operative voltage is set to a fixed value in the range 850-1000V. The system perform a scan: starting from a delay of 0 ns, it reads the CLARO hitcounts registered in an integrated interval of 25 ns, then in the next step the delay is incremented of 25 ns, covering a time range from 0 to 6.4 μ s (256 steps). The LED driver is used as signal source and it is set to send 100k pulses at a rate of 100kHz for each test step. The result is reported in Figure 8.15. The highest peak of the distribution is present at the steps 14, with a second high peak in the step 15 (these two steps correspond to the 350-375 ns interval), and corresponds to the true signal from the LED driver. The counts after it are SIN, and

they last until the very end of the time range.

R-Type Top Left & H-Type								R-Type Top Right							
64	63	62	61	60	59	58	57	8	16	24	32	40	48	56	64
56	55	54	53	52	51	50	49	7	15	23	31	39	47	55	63
48	47	46	45	44	43	42	41	6	14	22	30	38	46	54	62
40	39	38	37	36	35	34	33	5	13	21	29	37	45	53	61
32	31	30	29	28	27	26	25	4	12	20	28	36	44	52	60
24	23	22	21	20	19	18	17	3	11	19	27	35	43	51	59
16	15	14	13	12	11	10	9	2	10	18	26	34	42	50	58
8	7	6	5	4	3	2	1	1	9	17	25	33	41	49	57
57	49	41	33	25	17	9	1	1	2	3	4	5	6	7	8
58	50	42	34	26	18	10	2	9	10	11	12	13	14	15	16
59	51	43	35	27	19	11	3	17	18	19	20	21	22	23	24
60	52	44	36	28	20	12	4	25	26	27	28	29	30	31	32
61	53	45	37	29	21	13	5	33	34	35	36	37	38	39	40
62	54	46	38	30	22	14	6	41	42	43	44	45	46	47	48
63	55	47	39	31	23	15	7	49	50	51	52	53	54	55	56
64	56	48	40	32	24	16	8	57	58	59	60	61	62	63	64
R-Type Bot Left								R-Type Bot Right							

Figure 8.14: Numbering scheme for the MaPMT anodes on the EC, where the observer is imagined facing the MaPMTs window. To notice that the numbering scheme for the R-type top-left MaPMT is the same as for an H-type MaPMT. The Anode 1 is always at the centre of the R-type EC. This implies that, going from 0 to 3, one MaPMT is rotated of 90° clockwise with respect to the previous one.

Several tests have been performed and it has been found that the highest number of counts is, in almost all the tests, at the step 14. For a very small number of anodes it has been found that the step 15 was the one with the highest number of counts. Hence the LED signal is considered as the sum of the hitcounts in the steps 14 and 15. In the steps 0-13 (0-325 ns) zero to few counts are detected, and they are counts due to the natural noise inside the MaPMTs (dark counts). Everything else, in the range 16-255 (400 ns - 6.4 μ s) is considered SIN. Two main parameters are extracted for each MaPMT anode during the ECQA procedure: the signal intensity and the SIN intensity, defined as the integral of the hitcounts in the SIN test step range 14-15 and 16-255, respectively. A useful visualization of the SIN

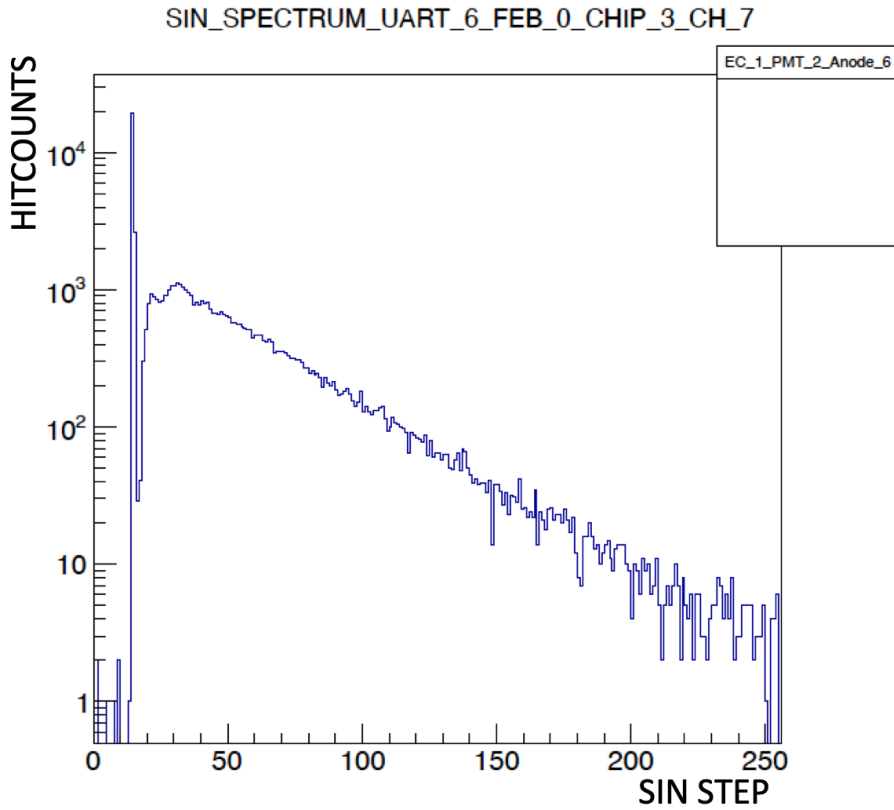


Figure 8.15: SIN distribution for a MaPMT anode. The association between CLARO channels, MaPMT anode and EC is explicitly reported in the distribution and histogram titles.

effects on the MaPMTs can be obtained using a 2D histogram representing the MaPMTs anodes where each histogram bin height is the ratio defined in Equation (8.1):

$$\frac{SIN_{Intensity}}{SIN_{Intensity} + Signal_{Intensity}}, \quad (8.1)$$

that is the SIN fraction on an anode with respect to the total signals registered in the full time window. An example is reported in Figure 8.16. The SIN fraction is high on the anodes 1-8 and 57-64, on the neighboring rows is at half of that value and in the center is almost absent. The value of the SIN fraction on the MaPMTs anode is not a parameter for which an EC can be considered faulty. The EC with the highest SIN fraction will be placed in the RICH regions at lower occupancy. the Hamamatsu[®] company already produced 150 new SIN-less MaPMTs which have already been tested

in Padova University and they will arrive in Ferrara for an in-depth SIN analysis. These new MaPMTs will replace the ones already produced with the highest SIN fractions.

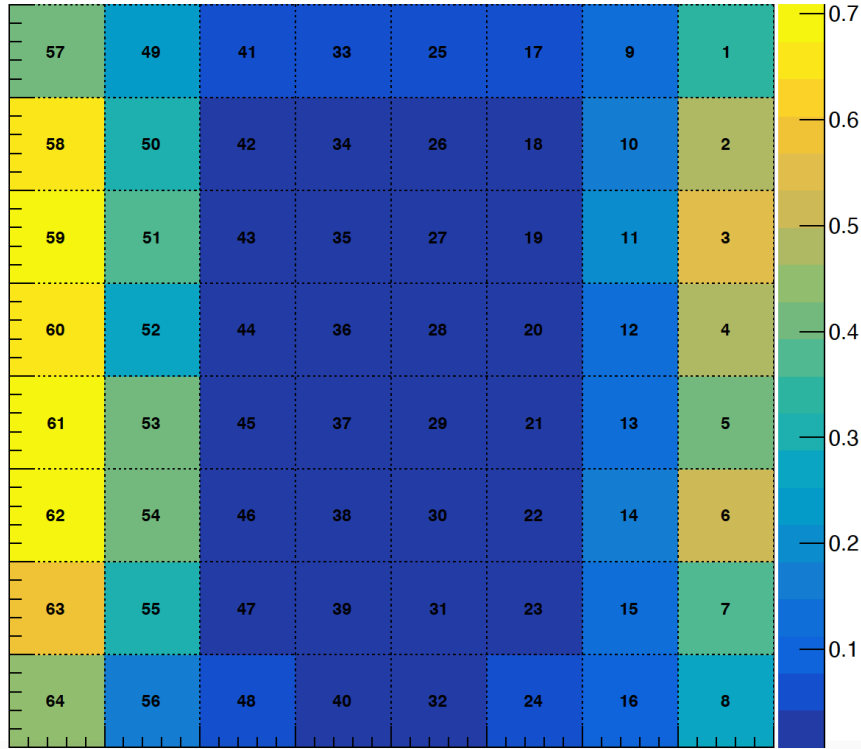


Figure 8.16: 2D histogram for an R-type MaPMT showing the SIN fraction per each anode. The number reported on each histogram bin is the anode number following the scheme of figure 8.14.

Using the data obtained from the SIN measurement it has been possible to calibrate the LED driver operative voltage in order to suppress the 2-3 photons emission events in the LED. For an R-type EC the average signal intensity (hitocunts in SIN test step 14-15) on the four MaPMTs has been measured as a function of the LED operative voltage and reported on a graph, together with the four-MaPMTs average. The results are shown in Figure 8.17, where the signal intensity increases as the LED voltage increases, as expected. The photon emission for an LED is regulated by the Poisson distribution. By setting the expected number of occurrences to 0.1, that is a 10% efficiency, the number of events with >2 photon emitted is almost zero. Therefore, since the number of pulses set for the LED driver is 10k, the optimal value for the LED operative voltage is the one at which we register,

on average, 1k pulses. This voltage is found to be 1.8V, which has been applied to all four the LED driver channels.

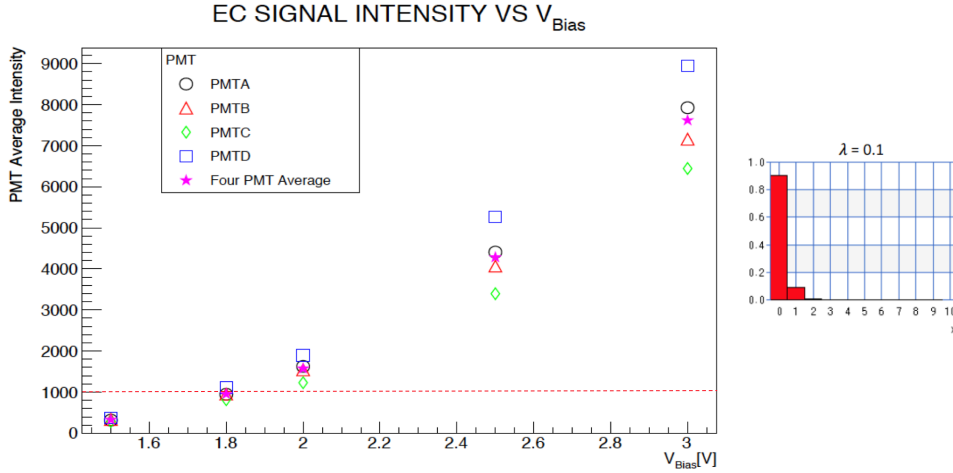


Figure 8.17: On the left, average signal intensity per MaPMT of the EC as a function of the applied LED driver voltage. On the right, the Poisson distribution optimized to suppress events of multi-photons emission.

8.3.2 The ECQA test protocol

After being assembled, a new load of ECs is mounted on the dark box without MaPMTs. The control software open the connection between the PC and the system controller, starts the python daemon (which allows to send commands to the system controller to perform the tests) and power on the CLAROs. Also it establish the connection with the HV crate and with the Raspberry Pi system, which start monitoring the voltages and currents of the MaPMTs and the environmental parameters, respectively.

1. S-Curve Comm Check:

the first test performed is a very fast coarse S-Curve (step 0x032, ~ 60.5 mV), named S-Curve Comm Check, whose sole purpose is to verify that a transition happens in every CLARO channel, hence assuring that no communication problems with the ASICs are present. A dedicated C++ scripts verifies that the first point (low signal intensity) has less than 5 counts and the last point (high signal intensity) has more than 950 counts, where 1000 pulses are the maximum number of pulses sent per DAC step, in every channel S-Curve. The thresholds of 5 and 950 have been chosen to account for possible counts oscillations in the

channel during the test. The script checks also if a channel is dead, that is counts always 0, or if its noisy counting always 1000 or more, or if the S-Curve is not monotonous and oscillations are present in the distribution. If any of this problem appears in one or more channels the corresponding EC is dismounted from the box, their connectors are cleaned using compressed air and the test is performed again. A communication error in electronic devices might only be due to a little bit of dust on the connectors, but if the problem persists the FEB corresponding to the defective channel is replaced (its QR code in the file is replaced as well) and the test is performed again. The defective FEB is then put aside for a future test on the FEB QA setup.

2. POR, SEU reset and ADC channels read:

a SEU counter reset and a Power-On reset are sent to the CLARO chips and the eight FPGAs ADC channels (FEB0 and FEB1, Bkb and two Bb temperatures, the FEB couple current and the CLARO VDD for the two FEBs) are read out and their value are registered in a file named LV_noconf.txt in the correspondent load folder. The file is named noconf since no configuration has been applied to the CLAROs yet. Then a configuration (0x314, but it doesn't really matter since no data from CLAROs is acquired) is sent to the CLARO channels and the ADC channels are read out again, this time being saved in a file named LV_conf.txt, since this time the CLAROs are configured.

3. HV measurement (without MaPMTs):

on the next step of the test protocol the HV is switched on at 1000V. After a waiting of 1 minute, to let the currents stabilize, the Bbs currents are measured and registered in a dedicated file, named HV_nopmt.txt, since no MaPMTs have been installed yet. The tension of the four HV channels is registered as well. Then the HV is switched off.

4. MaPMTs mounting + S-Curve Comm Check:

the MaPMTs are mounted in the ECs, after their QR codes have been scanned. An S-Curve Comm Check is performed to ensure that the mounting of the MaPMTs has not created communication problems with the CLAROs. If the test is ok the dark box is finally closed, otherwise the problem has to be investigated as before.

5. HV measurement (with MaPMTs):

the HV is switched on at 1000V (40V/s ramp-up speed) and the Bbs currents are monitored for 1 minute, after which the average value of

the currents for the four HV channels are calculated and registered in the HV_pmt.txt file together with the HV tensions. Then the HV is set to 1050V (40V/s ramp-up speed) and the currents are monitored for 1 minute. Then the average value for the Bb currents at 1050V is extracted and will be used to set the HV crate current limit during the night. Then the HV is switched off.

6. S-Curve test:

an S-Curve test is performed on all the CLAROs (range 0-725 mV, step 1.2 mV) using six different configurations: the channels are always enabled, as well as the Hysteresis, but the channel thresholds are sent to 10, 20, 30 with Offset bit 0 (configuration 0x30A, 0x314 and 0x31E respectively) and 42, 52, 62 with the Offset bit 1 (configuration 0xB2A, 0xB34 and 0xB3E respectively). Right after the data have been acquired a python script finds the transition point for each channel using the fit method. It also produces PDF plots of the S-Curve for each channel and cumulative distributions of both transition point and S-Curve spread for all the channels of the load per each different CLARO configuration. If a channel doesn't have the transition an error message is produced but the procedure doesn't stop. Only at the very end of the test the user checks the data and decide if an EC is to be put aside or not. The channels transition points and spreads are also stored in a dedicated text file. More details on the data analysis will be given in the next section.

7. 1050 V stand-by:

after the S-Curve test the ECs are left with the HV set at 1050V for 10 hours. This procedure is necessary to reduce the electronic noise (dark counts) inside the MaPMTs, since they have been tested 2-3 years ago in the Photon Detector Quality Assurance (PDQA) and since then they have been in boxes waiting for the ECQA.

8. Threshold Scan test:

the first test to be performed after the 10 hours at 1050V is the Threshold Scan. The HV is set at 1000V, all the channels are enabled, the Hysteresis bit is 1 and the threshold ranges from 63 to 0. This test is performed twice, with Offset bit at 0 and 1. The LED driver is set to send 100k pulses at 100kHz per threshold step. A C++ script is launched at the end of the test to analyze the data and extract, for each channel, the threshold corresponding to the pedestal.

From there, five threshold steps are added and that is considered the channel working point, which is registered in a dedicated text file. For the Offset bit 0 threshold scans only a small number of channels will have the pedestal, while for the others the working point evaluation cannot be done using this script. A separate script may provide the pedestal position also for the Offset bit 0 files. The procedure is explained in the Threshold Scan data analysis section. As in the S-Curve tests, also in the Threshold Scan test a channel without transition or which gives another error doesn't stop the procedure, but triggers an error message.

9. Dark Count Rate measurement:

the MaPMTs Dark Count Rate (DCR), that is the rate of registered counts without any light source on the PMTs, is measured with the HV set at 1000V. First all CLAROs are configured with threshold 7 and the DCR is measured in a 100s time window, then the CLARO channels are configured at their optimal threshold obtained from the previous Threshold Scan test and the DCR is measured in a 100s time window. A C++ script perform the data analysis and produces 2D histogram plots with the DCR of the MaPMTs. A threshold is set for which the DCR of a channel has to be lower than 1 kHz, otherwise an error message is generated. This threshold is given by the production parameters guaranteed by the Hamamatsu[®] company.

10. SIN test:

lastly the SIN test is performed at four different MaPMTs operative voltages (1000V, 950V, 900V, 850V), since the SIN intensity strongly depends on the MaPMT tension. In this test the CLAROs are configured at their optimal thresholds. After the data have been taken, a C++ script is launched which performs the analysis and produces the PDF plots containing the MaPMTs 2D histograms and the SIN spectrum for every channel. No limit threshold is set on the SIN or signal intensity in this test.

The operator, at the end of the test, can check the data plots and the system log to decide whether or not to accept or reject an EC. A log file is generated at the beginning of the test and all the outputs from all the several sub-VIs of the control software are registered in it. The total time of the test is ~ 12 hours but, since a 10 hours waiting time is set and 2 hours are needed to assemble the ECs and mount them, together with the MaPMTs, an entire day is required to test a full load.

8.3.3 DAQ software

The DAQ control software has been developed in NI LabVIEW 2017 64-bit. A python daemon is launched when the control software starts so that dedicated DAQ python scripts can be executed via LabVIEW through low-level functions specifically built for this purpose. The python scripts are the same used in the FEB QA setup and provide the basic functions to operate with the system controller and the CLAROs (e.g. open/close connection between PC and system controller, CLARO power on/off, CLARO configuration register read/write, ADC channels read). These low-level functions are the core of the Virtual Instruments (VI) used to performed the QA tests on the ECs. In the first step of the software development a standalone VI for each type of measurement present in the test protocol has been developed: ADC channels read, S-Curve tests (Comm Check and standard), Threshold Scan, SIN and DCR measurement. These VIs perform the measurement for which they have been developed and then they stop, no automatization in the ECQA process has been implemented in this stage of the software development. Hence, the user has to run all the VIs separately and manually to perform all the tests in the test protocol. In addition to the standalone measurement VIs, a VI has been developed to scan the components QR codes and generate the files containing the ECs information, together with a configurator VI. This Vi has been developed to read the file containing the working points for all the Load channels found with the threshold scans data analysis and to configure each channel to its optimal threshold, so that the ECQA tests with the optimized thresholds can be performed. The connection to the system controller and the python daemon start are manually initialized using the `syscmd_open_ECQA.vi` and the `command_NET_OPEN_ECQA.vi` low-level functions reported in Figure 8.18. The `syscmd_open` function launches the python daemon and has to be executed first, then the `command_NET_OPEN` can be executed, in which the system controller IP address has to be inserted together with the communication ports.

Before the test starts the user has to set several parameters in the VIs, some of which are present in every standalone VI and others are specific for each test.

The Load Number, the EC Type and the Station are parameters to be set in every VI and they determine the path at which the data file is saved, because the load data folder name depends on these parameters. Since an H-type EC load has a complete different anode/CLARO channels mapping scheme and 1/4 of the channels with respect to an R-type load, the information on the EC type is propagated to the analysis script running at the end

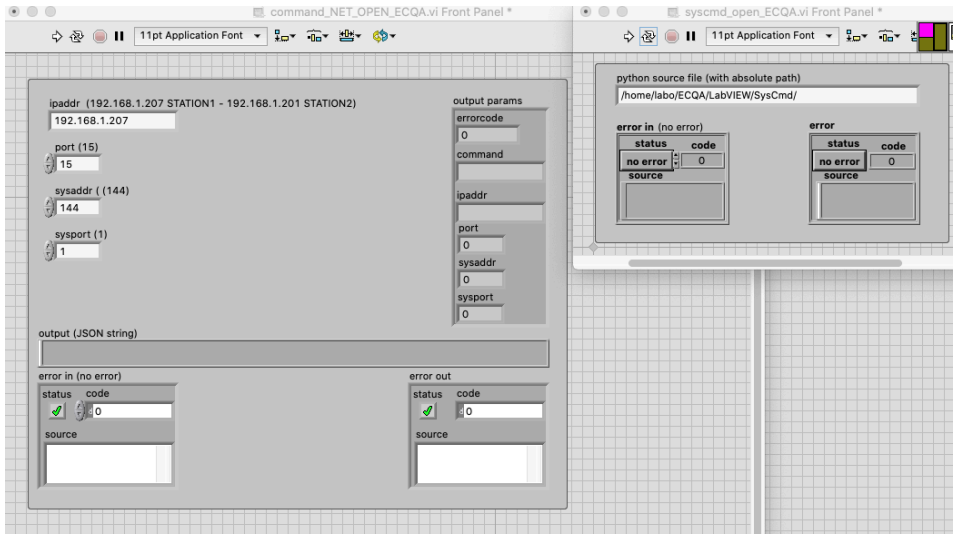


Figure 8.18: The control panel of the two low-level VIs used to open the connection with the system controller (left) and to start the python daemon (right).

of the test so that the correct number of the channels is analyzed and the right mapping scheme is applied. Two LED driver parameters can be set for the tests using it (SIN and Threshold Scan): the number of pulses to be sent in each test step and the frequency. The LED driver parameters are also set for the DCR measurement, even if the light is not used for the test, to define the temporization of the test (e.g. setting 100k pulses at 1kHz set the DCR acquisition time to 100s). The values of these two parameters are written in the data file header for reference. For Threshold Scan, DCR and SIN measurements the voltage at which the test is performed is to be set. However, this does not act as a control for the system voltage, but just as an indicator. The value set there is written in the data file header for reference. For this first phase of the ECQA DAQ software development the system HV is controlled using the ISEG crate web browser interface.

In Figure 8.19 the control panel of the standalone VI for the ADC channels and HV channels read is shown. In the "Voltage Type to measure" control is possible to select LV or HV. Selecting LV the DBs ADC channels are read out, while using HV the ISEG crate channels are read out and the current and tension values are reported in the eight indicators in the bottom left corner. Also, selecting LV/HV will change the first part of the data file name (LV_ or HV_). The second part is determined by the two boolean selectors under the "Voltage Type to measure" control. The upper

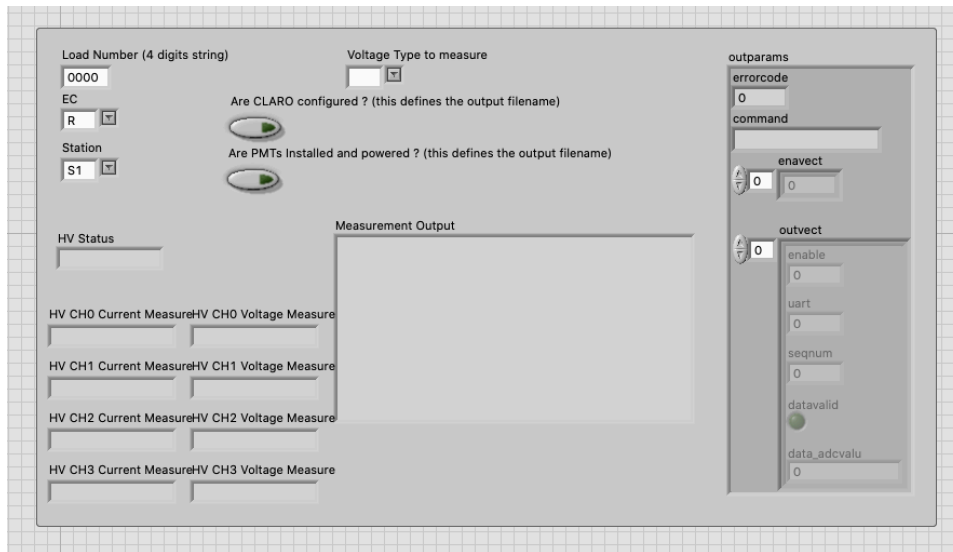


Figure 8.19: The control panel for the ADC channels and HV channels read standalone VI.

boolean ("Are CLARO configured?") control refers to the ADC channels reading, which is performed before and after the CLAROs configuration. If the CLAROs are not configured (control is 0), the ADC channels are read out and the data are written to the file `LV_noconf.txt`. If the CLAROs are configured (control is 1) the ADC channels are read out and the data are written to the file `LV_conf.txt`. The lower boolean ("Are PMTs Installed and powered?") refers to the HV channels reading, performed at 1000V with and without the MaPMTs on the ECs. Depending on the boolean state (0/1) the HV data are written to the file named `HV_nopmt.txt`/`HV_pmt.txt`. The indicator "Measurement output" will show the data written to the data file, header included. The "outparameters" cluster contains the ADC channels reading, together with the error state of the acquisition (0 means no errors).

In Figure 8.20 the control panel of the standalone VI for the S-Curve Comm Check test is shown. The only parameters to be set are the general Load information and the output files names: the raw data file (named `"S_Curve_Comm_Check.txt"` in the figure) contains the S-Curve data for all the channels, while the log file (named `"S_Curve_Comm_Check_log.txt"` in the figure) contains the analysis script output which is also shown in the "S-Curve Check errors" window. The "concatenated string" indicator is used to check the command line executed to run the C++ script to analyze the raw data file, in case there are problems with the path. The "Channel configuration" indicator shows the channel threshold applied for the test (in

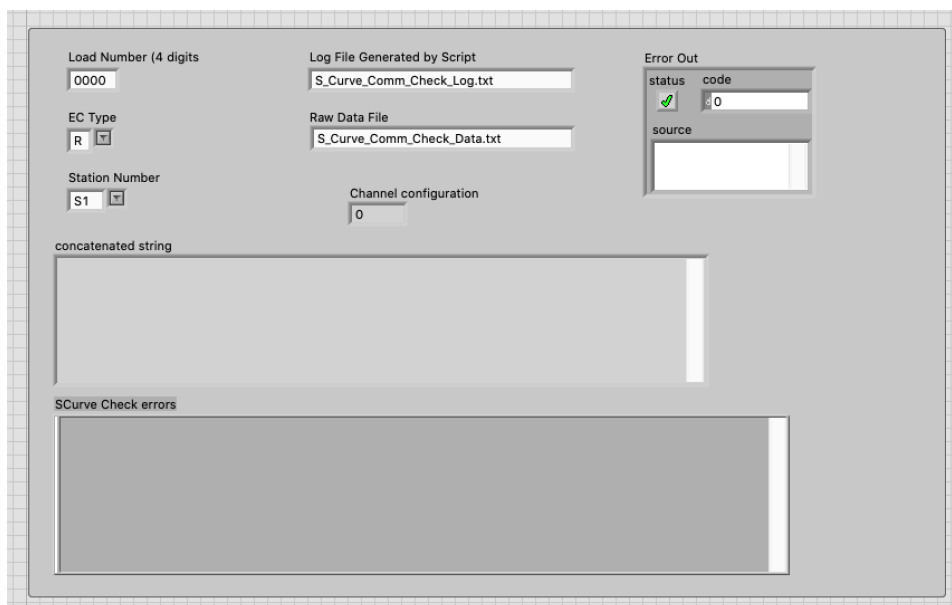


Figure 8.20: The control panel for the S-Curve Comm Check test standalone VI.

decimal code) and the "Error Out" window returns the error state of the test execution.

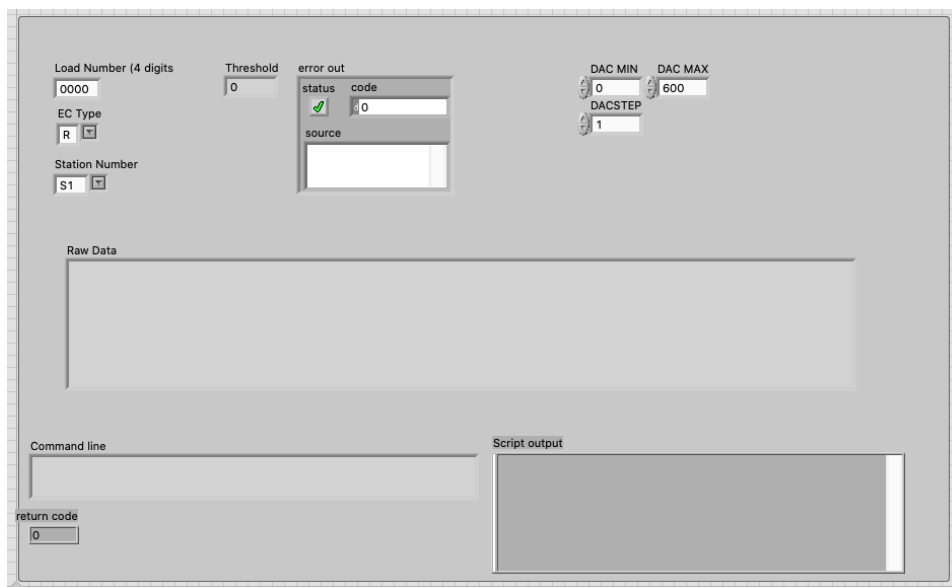


Figure 8.21: The control panel for the S-Curve test standalone VI.

In Figure 8.21 the control panel of the standalone VI for the standard S-

Curve test is shown. The minimum and maximum DAC limits have to be set, together with the DAC step. The "Threshold" indicator shows the applied threshold to the CLARO channels. "error out" returns the test execution error state, while "return code" returns the analysis script execution error state. The indicators "Raw Data" and "Command line" report the raw data to be written on the data file and the command line executed to run the C++ script to analyze the raw data file, respectively, and "Script output" reports the analysis script output.

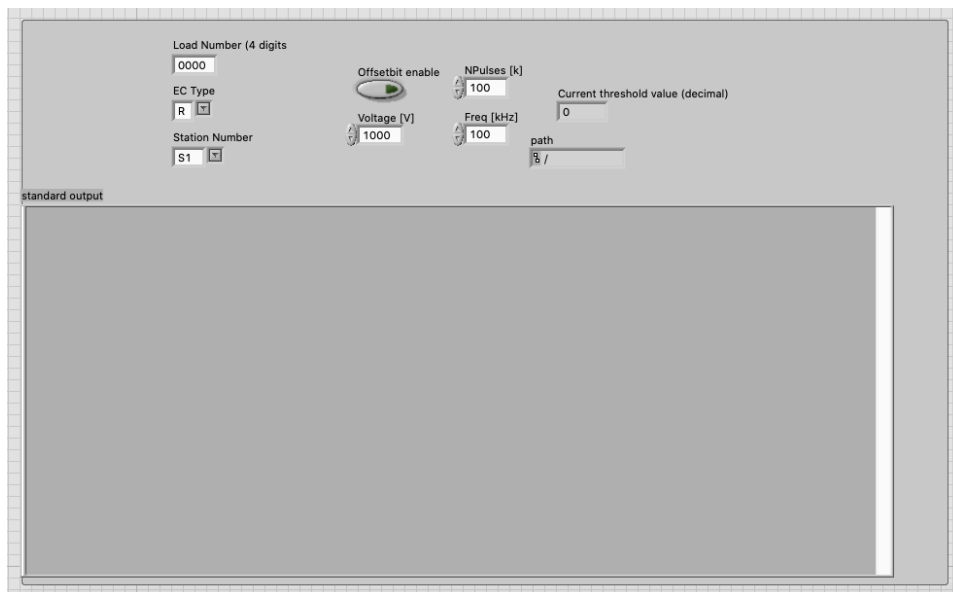


Figure 8.22: The control panel for the Threshold Scan test standalone VI.

In Figure 8.22 the control panel of the standalone VI for the Threshold Scan test is shown. The CLARO Offset bit can be set to 0 or 1 using the dedicated boolean control, while the threshold applied, shown in the "Current threshold value" indicator in decimal code, is always from 0 to 63 with a step of 1. The "path" indicator shows the path used to save the optimized threshold file generated by the analysis script, the output of which is reported in the "standard output" window.

In Figure 8.23 the control panel of the standalone Vi for the SIN test is shown. The number of 25 ns steps in which the test is performed can be set in the "Number of Steps" control. The "SIN step" indicator shows the current step number, to monitor the progression of the test. The CLAROs for this test can be configured to a common threshold using the "CFG (decimal)" control and setting the "Configure" boolean to the true state. The threshold value applied in this case is reported in the "Threshold value applied" indic-

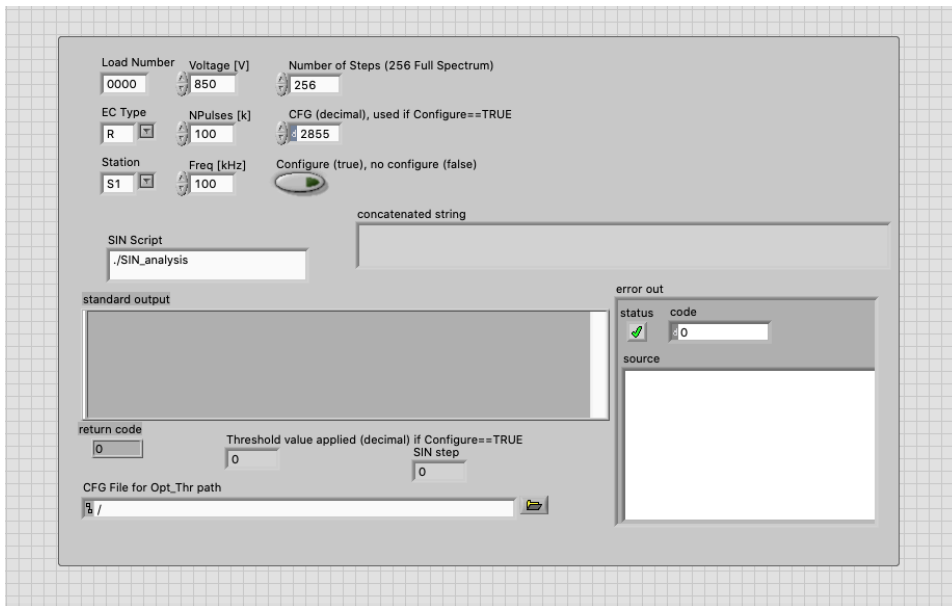


Figure 8.23: The control panel for the SIN test standalone VI.

ator at the bottom of the panel. If the boolean control is in the false state, no configuration is sent to the CLAROs, so that the optimized threshold configuration can be used (sent before starting the SIN test using the dedicated configurator VI). The path to the optimized threshold file used to configure the CLAROs before the SIN test can be put in the "CFG File" control path window at the bottom of the panel, and that path will be inserted in the data file header for reference. The "SIN Script" control allows to specify the analysis script to be used, the output of which is reported in the "standard output" window and the "return code" indicator returns the analysis script execution error state. In the "concatenated string" window the command line executed to run the C++ script to analyze the raw data file is reported. The "error out" cluster contains information on the status of the test.

In Figure 8.24 the control panel of the standalone Vi to perform DCR measurement is reported. As for the SIN VI, a common CLARO configuration can be set for all the chips using the "Configure" boolean control, and the configuration set in the "Configuration" control is set for all the ASICs. The analysis script name is set in the "DCR Script" control, while the script output and its execution state are reported in the indicators named "standard output" and "return code", respectively. The "concatenated string" indicator shows the command string sent to execute the analysis script.

In Figure 8.25 the configurator VI control panel is shown. Two files have

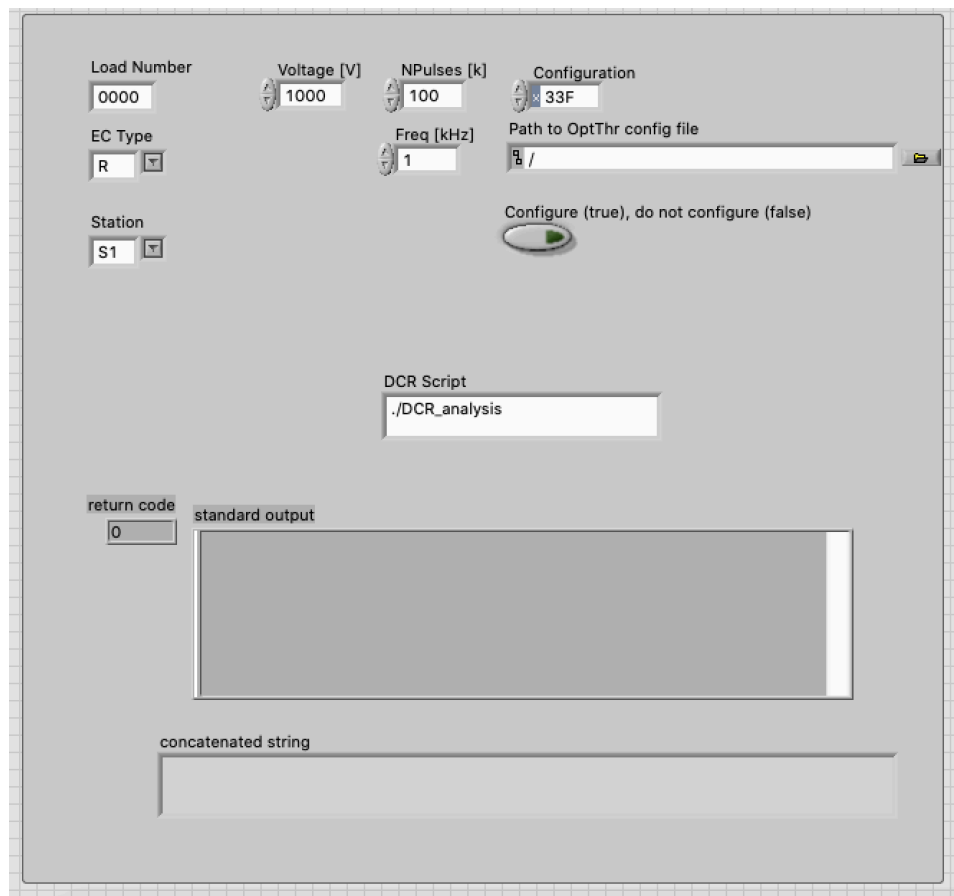


Figure 8.24: The control panel for the DCR test standalone VI.

to be selected: the file in the upper control is a default configuration file, while the lower one is the optimized threshold file to load into the setup. The VI reads these two files and write the appropriate configuration to each chip. The EC type has to be specified. After all the chips have been configured, their configuration is read out and compared to the one that has been sent to them. The "WRITE CFG" and "READ CFG" indicators show in real time which configuration has been sent to a chip and what is read out from it. The chip being read out is identified using the three indicators "UART", "FEB" and "CHIP". If for one or more channel the configuration sent and the configuration read out don't match an error is generated in the "Error" window.

After all these standalone VIs have been developed and used to perform the ECQA tests on 50 loads using the two Ferrara test stations, a state machine has been developed (always with LabVIEW) to perform the full test

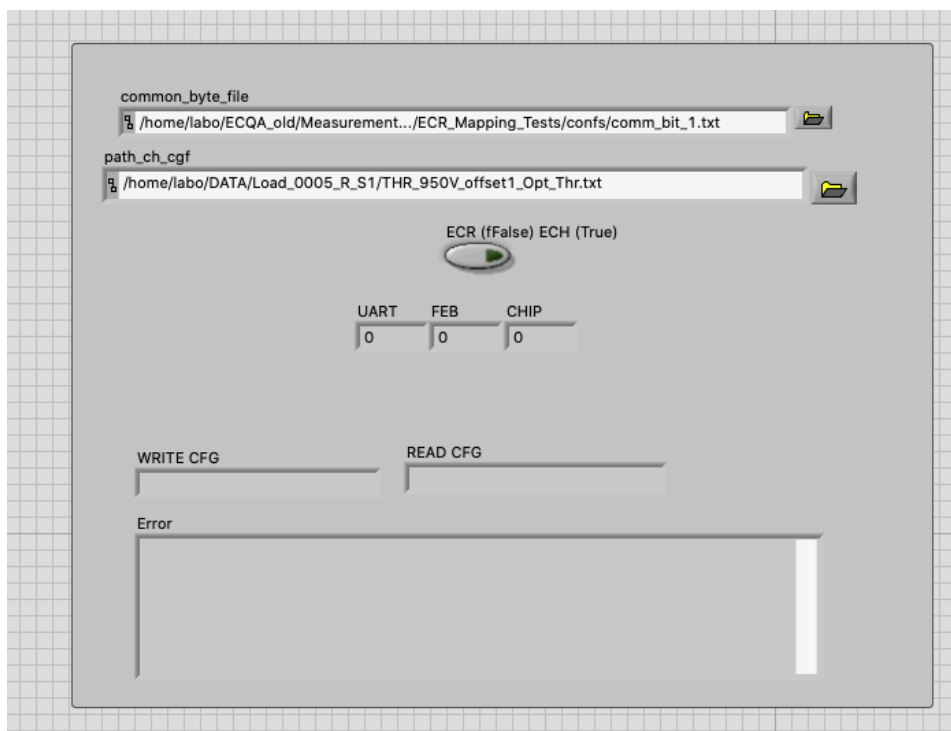


Figure 8.25: The control panel for the configurator VI.

protocol in an automatic way. The state machine uses the standalone VIs as sub-VIs, so the file output and the data analysis don't change, but every measurement is launched automatically following the test protocol without the user intervention. The user has to assemble the EC scanning the component using the `EC_scan` standalone VI (Figure 8.26), mount them on the box, start the state machine and wait until the measurements without the MaPMTs are performed. If everything is ok (currents under limit threshold, CLARO communication is fine) then the MaPMTs can be scanned directly from the state machine control panel and their code will be appended to the appropriate EC file containing all its component QR codes. After this operation the box can be closed and the tests continue until completion, the next day. The main upside of the state machine is that all the system parameters are constantly monitored like the CLARO configuration register, which is read out every time a new one is written (this was not implemented in the standalone VIs for time constraints) or the system HV, controlled and monitored directly from LabVIEW. The automatization of the procedure also reduces the possibility of errors by the users and the dead times between the measurements.

In Figure 8.27 the control panel of the ECQA state machine is shown. Each phase of the test protocol has a separate tab in the bottom-left window, from the MaPMTs scan to the measurements, for which dedicated indicators have been inserted in the correspondent tab to show possible error messages during the tests. After a test protocol step has finished, the "CONFIRM STEP" control has to be pressed to pass at the next step. In the top-left corner the "MAIN CONTROL" panel allows to select which phase of the test execute, when running in MANUAL mode, and to change from MANUAL to AUTO. Every test can be repeated as many time as the user needs, in case of problems. If the AUTO mode is selected, the state machine will perform all the steps reported in the window on the right-hand side of the "CONFIRM STEP" control. The test protocol steps to be performed, together with the setup parameters, are chosen before the test starts using the dedicate panel shown in Figure 8.28, where all the measurements parameters, the threshold for the LV and HV currents, the system controller, LED driver and Raspberry Pi settings can be modified following the user needs. On the left-hand side of the "CONFIRM STEP" button the Load information have to be inserted before starting the test. On top of this panel, the environmental information (temperature and humidity of the two sensors in the box with maximum and minimum values registered) are reported and constantly monitored throughout the test. On the left-hand side of the window the system controller and HV control/ monitor panels are present, which report the state of the connections with the system controller and with the ISEG crate, respectively. The python daemon state (which has been launched automatically when the test starts, as well as the system controller communication opening) is monitored as well. Three log windows are used to check the system controller activity, the ISEG crate activity and the test general activity. The logs are written in the Load folder in dedicated log files.

Operator: Igor
Location: Ferrara
EC Type: [dropdown]
Load Number (4 digits): 0000
Station Number: 1
EC Position: [dropdown]

ELEMENTARY CELL

Backboard: [input]
FEB I: [input] FEB II: [input]
FEB III: [input] FEB IV: [input]
Baseboard: [input]
ID EC (Backboard): [input]

PMT A: [input] PMT B: [input]
PMT D: [input] PMT C: [input]

Figure 8.26: The control panel of the VI for the scan of the QR codes of the EC components.

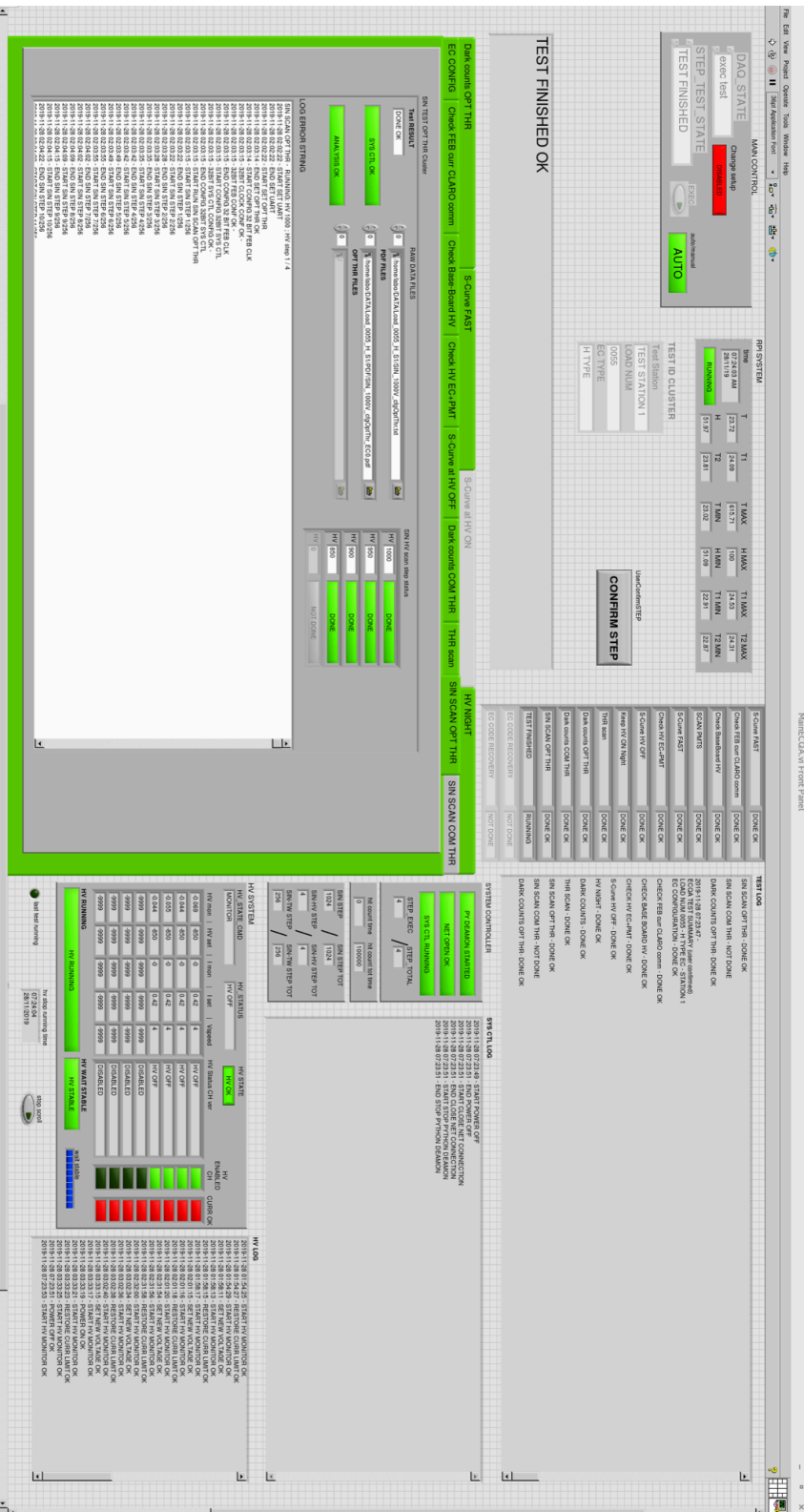


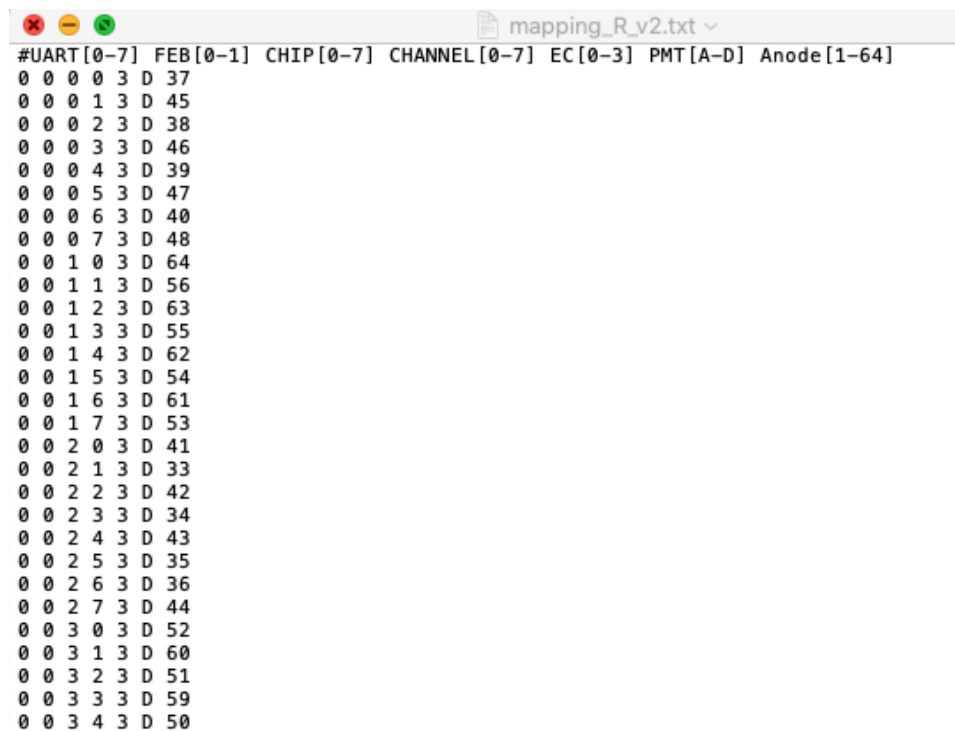
Figure 8.27: The control panel of the finite state machine for the automatic ECQA procedure.



Figure 8.28: The finite state machine parameters settings panel.

8.3.4 Data analysis

The data analysis on the ECQA measurements is performed right after a test has finished using a dedicated script for each different measurement. The scripts are launched directly via LabVIEW. All the scripts use two mapping file, one for the R-type ECs and one for the H-type ECs, to correctly associate a CLARO channel to the right MaPMT anode on the correct EC. A portion of the R-type mapping file is shown in Figure 8.29. A one-line header is put to facilitate the file readability. The channel ID (UART FEB CHIP CHANNEL) is associated to its anode (1-64) of its MaPMT (A-D) of its EC (0-3). The H-type file is almost identical, except for the fact the only one MaPMT is present per EC so there is no need for the sixth file column. Using these files the 2D histogram plots can be produced with the correct physical anode-CLARO channel (optical-electronical) association.



```
#UART[0-7] FEB[0-1] CHIP[0-7] CHANNEL[0-7] EC[0-3] PMT[A-D] Anode[1-64]
0 0 0 0 3 D 37
0 0 0 1 3 D 45
0 0 0 2 3 D 38
0 0 0 3 3 D 46
0 0 0 4 3 D 39
0 0 0 5 3 D 47
0 0 0 6 3 D 40
0 0 0 7 3 D 48
0 0 1 0 3 D 64
0 0 1 1 3 D 56
0 0 1 2 3 D 63
0 0 1 3 3 D 55
0 0 1 4 3 D 62
0 0 1 5 3 D 54
0 0 1 6 3 D 61
0 0 1 7 3 D 53
0 0 2 0 3 D 41
0 0 2 1 3 D 33
0 0 2 2 3 D 42
0 0 2 3 3 D 34
0 0 2 4 3 D 43
0 0 2 5 3 D 35
0 0 2 6 3 D 36
0 0 2 7 3 D 44
0 0 3 0 3 D 52
0 0 3 1 3 D 60
0 0 3 2 3 D 51
0 0 3 3 3 D 59
0 0 3 4 3 D 50
```

Figure 8.29: The R-type EC mapping file used by the analysis scripts to correctly map the CLARO channels and produce 2D histograms.

The S-Curve Comm Check analysis is performed using a C++ script which reads the raw data file. The purpose of the analysis is just to check that every channel has a transition and that all the channels are behaving properly. For this reason the script check that the channel hitcounts at the first DAC step are smaller than 5 and that at the last DAC step are bigger than 950, over a total of 1000 pulses sent per DAC step. As said in the test protocol explanation, these limits are set to account for possible small fluctuations in the channel hitcounts. The script also checks if a channel is always at 0 hitcounts or at >1000 hitcounts, being dead in the first case and noisy in the second case. If any of these cases happen a text error is generated and propagated to the VI error window and saved in the log file. No plots/distributions are produced in this analysis.

The standard S-Curve analysis is performed using a python scripts which reads the raw data. Using the standard S-Curve fit function (Equation (5.2)) with ROOT, the transition point and the sigma for each channel are obtained. The fit Chi-square parameter is used to spot possible problems in the channels. The script generates a PDF file for each raw data file (in total six S-Curve data files, for six different configurations, are produced during the ECQA procedure). The title of these files is SCURVE_cfgXXX_dist.pdf, where XXX is the CLARO channel configuration for that raw data file (0x314, 0x30A, 0x31E, 0xB2A, 0xB34, 0xB3E). In the file two histograms are produced, which are the transition point and sigma distribution for all the channels of that load. Then the S-Curve distributions for all the channels are produced in the file. In Figure 8.30 the transition point and sigma distributions for a load are reported. The configuration applied in this case was 0x30A (threshold 10). The number of entries is 1024 that is all the channels had a transition. In Figure 8.31 the S-Curve distribution for a single channel is reported. A log file is generated by the script, containing any errors found in the test (no transitions, noisy/dead channels), together with a parameter file containing, per each channel, the transition point and the sigma (in DAC units), the errors on these two parameters given by the ROOT fit and lastly the four channel ID parameters. A further analysis is performed on the S-Curve data to extract the linearity parameters of the channels: the channel transition points at different thresholds are reported in a graph as a function of the applied threshold, then a linear fit with ROOT is performed to find the slope and the y-axis intercept of the line. The slope of the line is the gain of the channel, that is the number of ke^- per threshold step, while the y-axis intercept is the channel offset in ke^- . Both parameters are extracted for each channel for its full characterization.

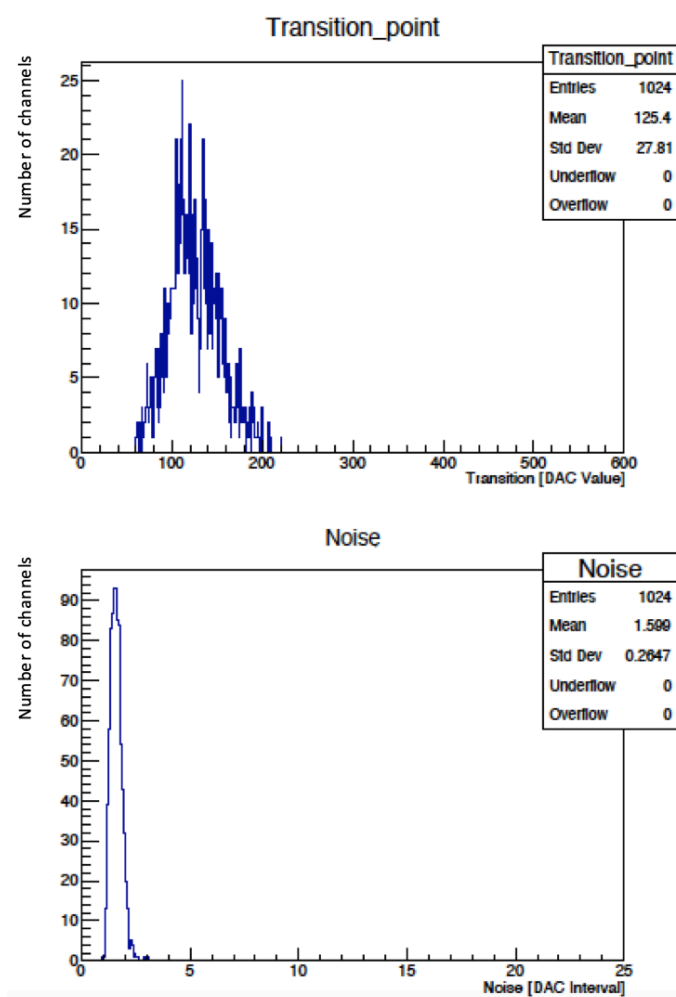


Figure 8.30: Transition point and sigma distribution for a full 4 ECs load R-type, generated by the S-Curve python analysis script.

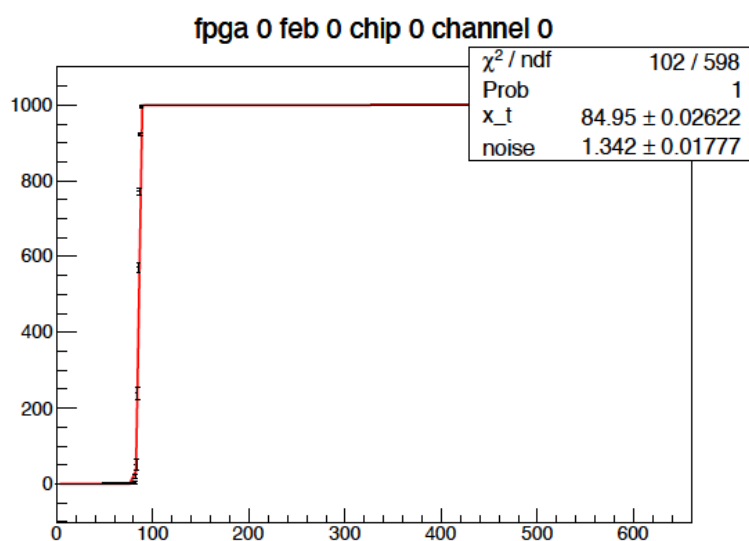


Figure 8.31: S-Curve distribution for a single CLARO channel obtained during the ECQA procedure. The channel ID is in the title of the graph. The fit parameters are reported in the top-right corner.

The Threshold Scan analysis is performed using a C++ script. The main purpose of this test is to find the optimized thresholds (or working points) for all the channels of the load. This is done by searching for the channel pedestal edge in the threshold scan distribution and setting five threshold steps above that point. In addition, checks are performed to ensure that every channel is active (no 0 counts), that the transition happens in all channels, that there are no channels with a normalized number of counts > 1 . The output of the script consist of a PDF file for each MaPMT of the load, a PDF containing the errors overview for the entire load and two text files, a log and the optimized threshold file. The error overview PDF (Figure 8.32) is a single plot containing a 2D 8×8 ROOT histogram for each MaPMT of the load. If during the test a channel has a problem (no pedestal found, dead/noisy channel) the correspondent bin on the histogram is filled, otherwise it stays blank. This allows the user to quickly check the data quality of the test.

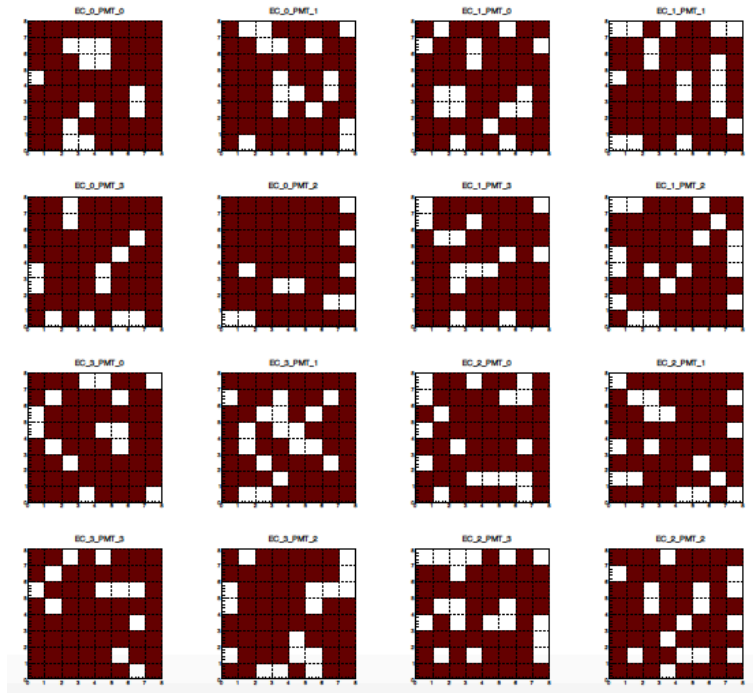


Figure 8.32: 2D histogram error overview for a threshold scan test. This test was performed with the CLAROs Offset bit at 0, hence most of the channels do not exhibit the pedestal and they are marked as defective in this plot.

In the single-MaPMT PDF files a 2D histogram with the found working point per channel is reported, as shown in Figure 8.33. This plot helps the

user to have an overview of the system behaviour in this test. After that, the single channel Threshold Scan distributions are reported (Figure 8.34). The association between electronics (UART FEB CHIP CHANNEL) and optics (ANODE MaPMT EC) is explicit in each plot to check that no mapping error is performed.

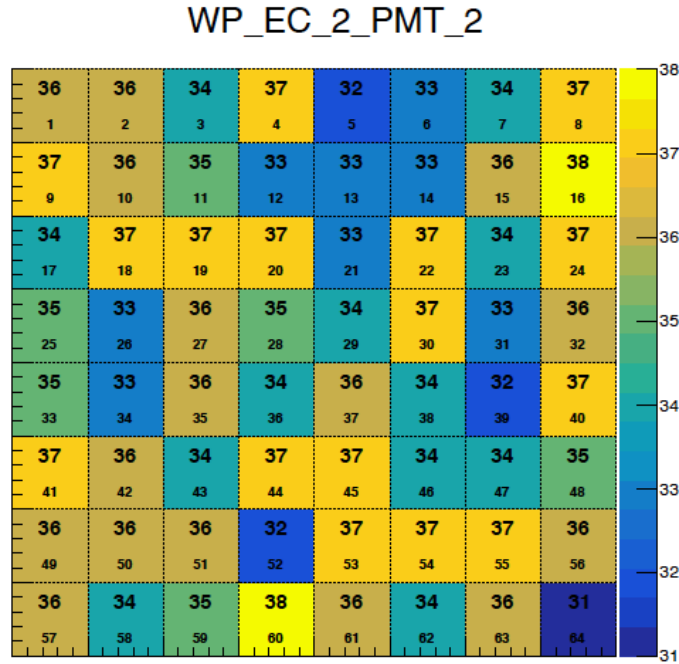


Figure 8.33: 2D histogram showing the found working points for all the channels of the MaPMT 2 (C) of the EC 2 (bottom-right).

The log file text file contains any errors found in the test (no transitions, noisy/dead channels). The optimized thresholds file contains a line for each channel. In each line the channel ID parameters are written, followed by the configuration (in decimal) to set that channel at the previously found optimized threshold with the Offset bit 1. The last element is the optimized threshold explicitly written, to help the user to read the file. The configurator VI reads this file and set the channel identified by the first four line parameters at the configuration found in column "CHANNEL-CFG".

The optimized thresholds are calculated also for the Offset bit 0 threshold scan files, even if the pedestal is not present in most channels. This is done using a dedicated algorithm which compares the Threshold Scan distributions for each channel obtained at Offset bit 0 and 1 and searches for the threshold at which the two distributions better overlap. The algorithm op-

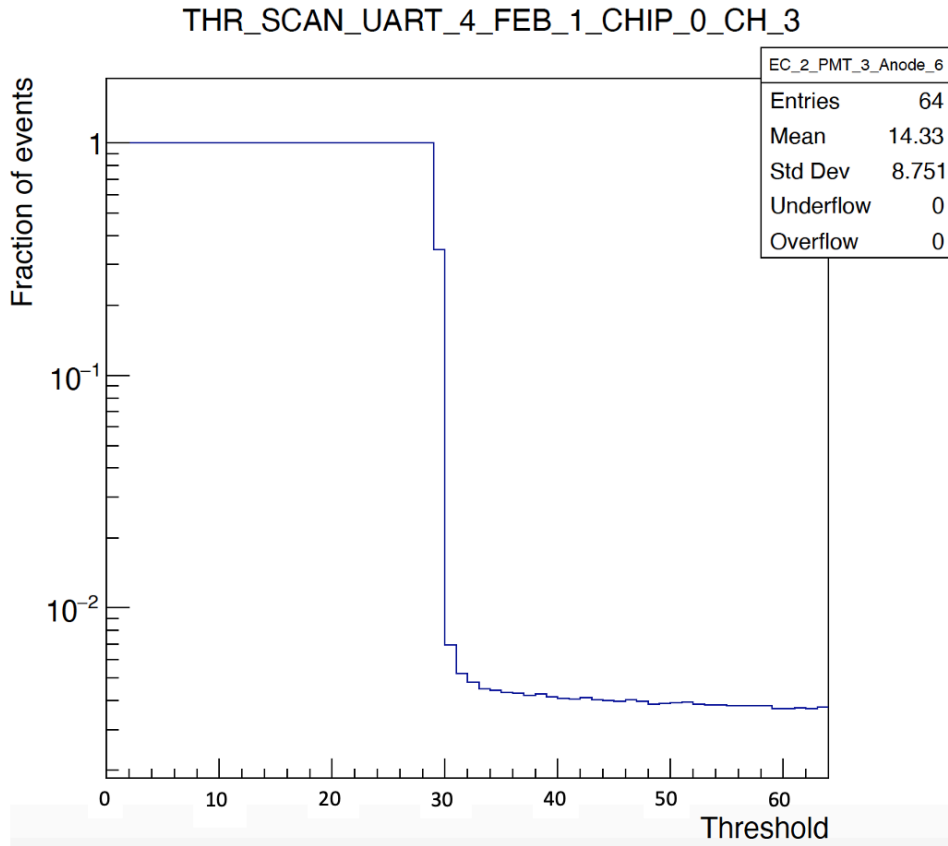


Figure 8.34: Typical Threshold Scan distribution for the CLARO channels in the ECQA procedure.

erates on the threshold range [19,42] for the Offset bit 1 distribution and [1,20] on the Offset bit 0 distribution. The content of the bin of the Offset bit 1 distribution C_1 is compared to the content of each bin in the Offset bit 0 distribution range C_0 using the formula:

$$\sum_{k=1}^{20} \frac{(C_1 - C_0 k)^2}{C_1}, \quad (8.2)$$

and the value obtained is put in a histogram for the bin referred to the C_1 bin threshold reference in the range [19,42]. The result is shown in Figure 8.35. The threshold at which the minimum in the distribution is found corresponds to the threshold offset of the channel, that is the actual shift operated by the Offset bit. Using this value is possible to evaluate the optimized threshold for the Offset bit 0 Threshold Scan distributions from the Offset bit 1 distributions.

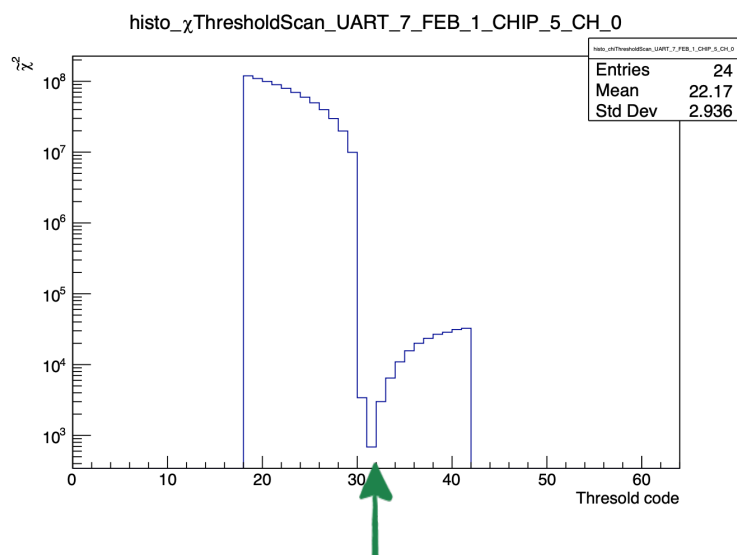


Figure 8.35: Distribution obtained for a CLARO channel for the threshold offset calculation. For this particular channel the action of the Offset bit is to shift the threshold by 32, that is the standard value.

The SIN data analysis is performed by a C++ script. The output consist of a PDF file per each MaPMTs in the load and of a single text file. The PDF contains three 2D histograms 8×8 which represent the MaPMT. The height of each bin is a different SIN parameter for each histogram: in the first one the "TOTAL" intensity is used, that is the sum of all the counts in the entire SIN spectrum for that channel; in the second one, the "SIGNAL" intensity is used, that is the total number of counts in the steps 14-15, corresponding to the true LED signal; lastly, the "SIN" fraction is used, defined in Equation 8.1. Using these three overview plots it's possible to monitor the SIN contribution for the MaPMTs while also monitoring the anodes uniformity. Then the SIN distributions for all the channels of that MaPMTs are reported in the PDF. AN example of these plots are shown in Figure 8.36.

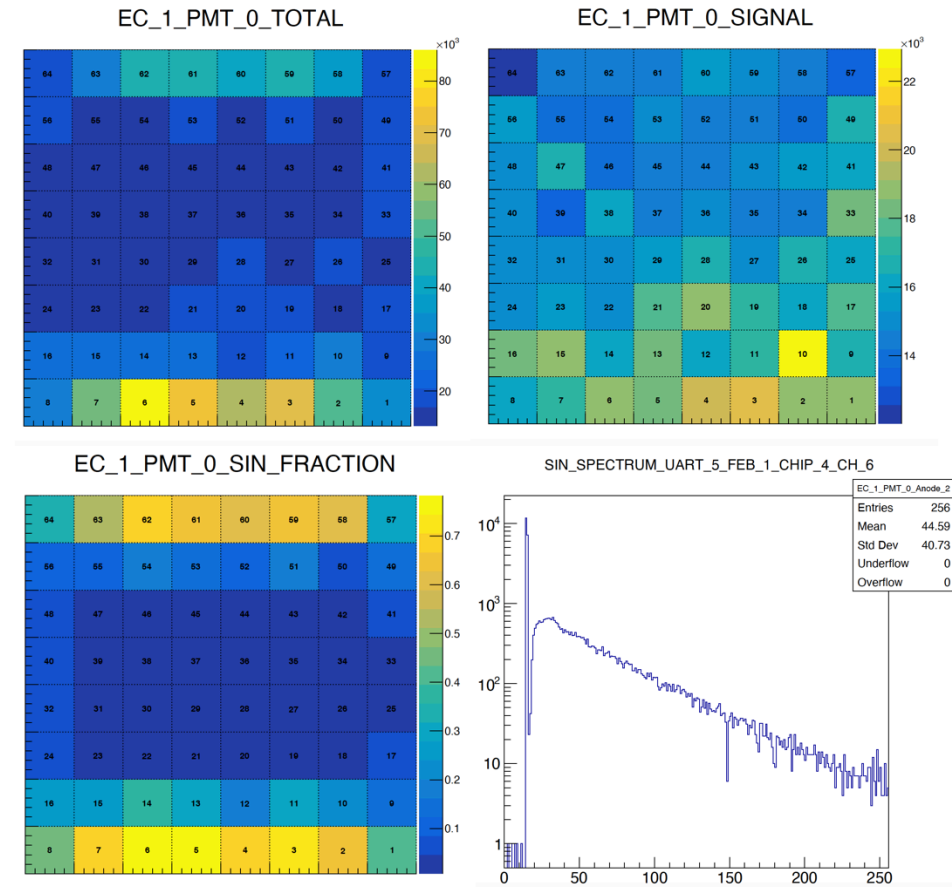


Figure 8.36: The three overview 2D histograms produced for the SIN analysis of a MaPMT, together with the SIN spectrum for a channel. Also here the connection between channel ID and MaPMT anode is explicit in the histogram title.

The DCR data analysis is performed by a C++ script. The script produces an error message if the DCR for a channel is over 1kHz. The output consists of a PDF file per EC of the load and a the log text file in which the script output is registered. The PDF file contains two set of 2D histograms representing the MaPMTs of the load. The first set of histograms is an error overview histogram, like the one in Figure 8.32, in which the MaPMTs anodes are colored only if the DCR for that anode is $> 1\text{kHz}$. In the second set of histograms the DCR for all the MaPMTs anodes are reported (Figure 8.37).

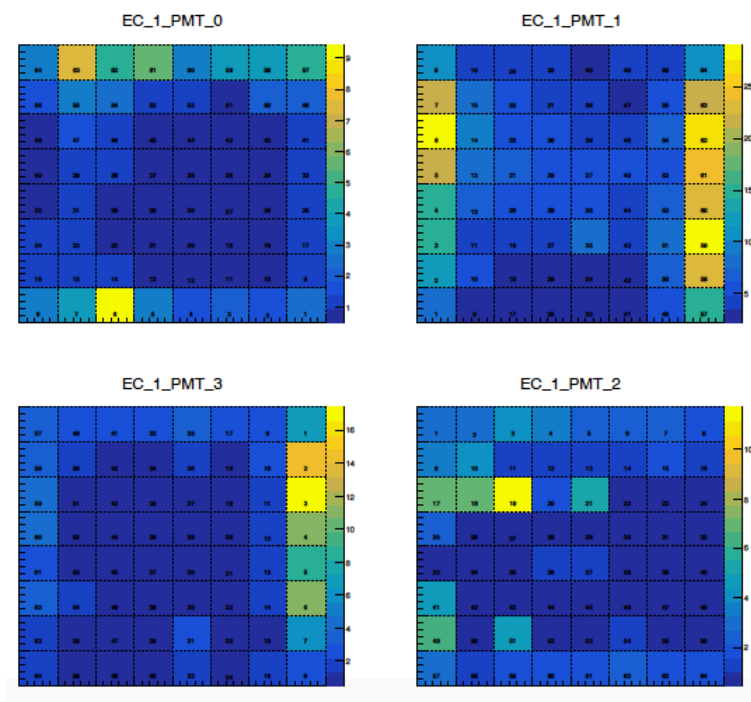


Figure 8.37: DCR plot for an R-type EC. The SIN contributions on the outer channels are present also in this kind of measurement. The number of the anode is reported on the corresponding bin.

8.3.5 EC boxing and delivery

After an EC has been tested and no problems have been spotted on it, a barcode is attached to its side (for a fast identification of the cell) and it's put in a plastic jar⁹ which has been customized so that the EC aluminum

⁹<https://export.rsdelivers.com/product/rs-pro/jwp0500p/rs-pro-lab-bottles-storage-bottle-pp-500ml/4781703>

case back part can be screwed to the jar cap. The jar is then kept always with the cap facing the floor and the MaPMTs facing upwards, as shown in Figure 8.38. This prevent the MaPMTs to detach due to possible vibrations/movements during the transport. The jar are then put in a Korrvu cardboard box¹⁰ equipped with a support with plastic membranes (Figure 8.39) which keep the EC spaced from the box. A maximum of two ECs can be put in the same box. A maximum of 40 boxes (80 ECs) are then shipped to CERN using a wooden box, in which the EC are always kept in the correct orientation.



Figure 8.38: The H-type EC screwed to the plastic jar cap ready to be sent to CERN. The barcode is visible on its side and a label with the EC load number and the station used to test it is placed on the jar bottom, which is facing upwards.

8.3.6 Database

The ECs main parameters are saved in text files which will be loaded into the LHCb database. A file per each EC is provided at the end of the ECQA procedure, and the file name is the barcode attached to the EC at the end of the tests, so that the EC parameters can be quickly retrieved.

In the file the general information on the EC are first reported, a line for each different element: EC barcode; date, time, place of the test, operator assembling the cell, station number ID, EC position in the load and Load Number. Then the EC components QR codes are reported: Bkb, FEBs and Bb following the scanning order, followed by the MaPMTs codes. The environmental temperature average registered during the tests is then inserted. After that, the eight ADC channel values taken from the LV_conf.txt measurement file are inserted. Lastly, the DCR for each MaPMT of the EC is reported. After these EC parameters the parameters per single channel are

¹⁰<https://sealedair.com/product-care/product-care-products/suspension-packaging>



Figure 8.39: EC jar in the Korrvu packaging ready to be sent to CERN.

inserted: S-Curve linearity slope and y-axis intercept for both the Offset bit 0 and 1 measurements (4 parameters); pedestal and optimized threshold for both the Offset bit 0 and 1 measurements (4 parameters); the Signal Intensity and the SIN intensity for the four SIN measurements, taken at 1000V, 950V, 900V, 850V (8 parameters). The different channels parameters line are separated by a default string.

Chapter 9

Conclusions

In this thesis I presented the validation tests performed on the optoelectronic chain which will be used in the LHCb RICH upgraded detector.

The CLARO ASIC, the core component of the RICH Upgrade electronics, has been tested in the most advanced European irradiation facilities using charged ion beams, proton beams and mixed irradiation field to ensure that it is able to operate on the foreseen environment of the upgraded LHCb experiment, for which the Total Ionizing Dose (TID) expected in the Run III + IV (2021-2029) is 200 krad, 3×10^{12} 1 MeV n_{eq}/cm^2 . The CLARO has been tested for Single Event Effects (SEE) in the ions test, performed at the Heavy Ion Facility (HIF) of Louvain-La-Neuve (BE) and at the Silicon and RADiation (SIRAD) facility in Legnaro (IT). From the data analysis of these ion test the Single Event Upset (SEU) and Single Event Latchup (SEL) cross-sections of the CLARO as a function of the ion Linear Energy Transfer (LET) have been measured. The LET threshold for SEU cross section has been found to be 20 MeV/mg/cm² in both tests. SEL occurred in the Louvain-La-Neuve tests with a LET > 50 MeV/mg/cm², but in Legnaro no SEL happened in the same LET range. At the IRRAD facility (CERN) the ASIC has been tested using a 24 GeV/ c proton beam up to a TID of ~ 14 Mrad. The SEU rate per Mrad has been measured for each tested CLARO, with values in the range 130-160 SEU·Mrad⁻¹. No SEL happened during this test. Lastly, the CLARO has been exposed to a mixed radioactive field in the CERN CHARM facility. The field, recreating a realistic LHCb environment possible, was mainly composed of protons, neutrons, pions and gamma photons but suffers from low particle rates, limited by the radiation protection rules. The TID absorbed by each CLARO was 80 krad. Due to the low TID the number of SEU was low (maximum 12) and no SEL

occurred. Given the performances in the aforementioned irradiation tests, the CLARO has been defined as suitable to operate in the required post-upgrade conditions in LHCb.

The LHCb RICH Upgrade prototype has been tested at the North-Area at CERN using a 180 GeV/ c charged hadron beam. Aim of the test was to test the full opto-electronic chain in a realistic environment using the miniDAQ as a data readout system. The prototype was composed of four full Elementary Cells (ECs), the compact structure with the CLAROs and the Multi-Anode Photo Multiplier Tubes (MaPMTs), mounted on a movable water-cooled structure placed inside a light-tight box, in which a borosilicate-glass lens is used as a radiator medium for Cherenkov photons. Using a dedicated software was possible to reconstruct the Cherenkov ring radius and angle and obtain an estimate of the three main contributions to the Cherenkov angle resolution (Chromatic error, Pixel Size error and Emission Point error). Then several runs of S-Curve tests and Threshold Scan tests have been performed on the setup and the data have been analyzed to fully characterize the CLARO behaviour in a system structurally close to the upgraded LHCb RICH setup.

In the last part of the thesis the validation tests on the CLARO chips, standalone and mounted on the Front-End Boards (FEBs), and on the ECs are presented. The components have been validated using dedicated Quality Assurance (QA) procedures. The entire CLARO production has been tested in Ferrara using two identical pick-and-place test stations, designed and produced in Ferrara, and a dedicated test protocol. The data from the preliminary QA tests have been analyzed to ensure both stations produced the same results and to characterize the tests stations, together with the CLARO so that the appropriate parameter's cuts during the procedure could have been applied. Then an analysis on the QA data of $\sim 1/4$ of the CLARO production has been performed to ensure everything was performed correctly. The results from this analysis were in agreement with the expected results from the used QA test protocol. The CLARO passing the QA procedure have been sent to the company responsible for the FEBs and Backboard (Bkb) production. The CLARO have been soldered on the FEBs and the boards have been tested on the company site using a dedicated setup designed and produced by the Ferrara RICH Upgrade group using a dedicated test protocol. The CLARO data coming from a portion of the first FEBs produced have been analyzed and compared to the results obtained from the CLARO QA data analysis results. This analysis has shown a good agreement between the results obtained from the two QA tests. All the electronic and optical

components have been assembled in ECs which are being tested in Ferrara and Edinburgh. Two test stations are present in Ferrara, each one composed of a light-tight box, a DAQ system and a LED driver to perform tests on the ECs with light. Up to four ECs can be tested at the same time using a test station. The DAQ software has been designed using NI LabVIEW, first developing standalone VIs to perform single measurements of the QA procedure and then developing a state machine able to perform the full test protocol sequence in an automatic way. Dedicated analysis scripts have been developed for each different measurement and the data obtained from the analysis have been collected in dedicated files per each EC to collect its most important parameters to be loaded into the LHCb database. These data represent a first level characterization of the ECs, which of course has to be performed again once the EC is mounted on the upgraded RICH detector.

All the tested ECs will be mounted on the upgraded RICH detectors (some of the RICH2 ECs have already been mounted) and during 2020 the upgraded RICH commissioning will start. Following this schedule it will be possible to start the data taking on March 2021, as expected.

Appendix A

Irradiation data analysis tools

The data from the irradiation tests on the CLARO chips have been analyzed following the European Space Components Coordination (ESCC) guidelines[57]. The Total Ionizing Dose (TID) D in rad absorbed by a silicon device when irradiated with an ion is calculated from formula (A.1):

$$D = F_{eff} \times LET_{eff} \times 1.6 \cdot 10^{-5}, \quad (\text{A.1})$$

where F_{eff} is the effective particle fluence, measured in ions/cm², and LET_{eff} is the ion effective Linear Energy Transfer expressed in MeV/mg/cm². For the proton irradiation the dose D in rad has been calculated using the formula (6.2):

$$D = F_{eff} \times 2.666 \cdot 10^{-10} \text{Gy} \cdot \text{particle/cm}^2 \quad (\text{A.2})$$

where F_{eff} is the effective particle fluence, measured in ions/cm² [60].

The Single Event Effects (SEE) cross-section σ is given by equation (6.2) already seen in section 6.2.1:

$$\sigma_{SEE} = \frac{N_{SEE}}{F_{eff}}, \quad (\text{A.3})$$

where N is the number of events and F_{eff} the effective fluence. The uncertainty on this cross-section is given by equation (A.4):

$$\frac{\delta\sigma}{\sigma} = \sqrt{\left(\frac{\delta N}{N}\right)^2 + \left(\frac{\delta F}{F}\right)^2}, \quad (\text{A.4})$$

which can be also written as equation (A.5):

$$\delta\sigma \times F = \sqrt{(\delta N)^2 + (N \times \frac{\delta F}{F})^2}, \quad (\text{A.5})$$

The term $\delta F/F$ is the uncertainty on the measured fluence, which was set to 15% for this thesis calculations. The term δN is the variance on the measured number of SEE. Assuming that SEE are random, the probability for one of them to happen follows a Poissonian distribution. Hence the variance on N is calculated from the Chi-Square distribution for a given confidence level. The variance has been calculated using the Excel functions reported below as a function of the confidence level CL. For the calculations in this thesis the CL was set to 95%. The lower limit of the confidence interval on N , Lower- N , is calculated as following:

- If no SEE occurred ($N = 0$), the lower limit Lower- N is set to 0;
- If $N > 0$, Lower- N is given by equation (A.6):

$$\text{Lower-N} = 0.5 \times \text{CHISQ.INV}((1 - \text{CL})/2, 2 \times N); \quad (\text{A.6})$$

the function CHISQ.INV returns the inverse of the left-tailed probability of the chi-squared distribution¹.

The upper limit of the confidence interval on N , Upper- N , is calculated as following:

- For all cases, that is $N \geq 0$, Upper- N is given by equation (A.7):

$$\text{Upper-N} = 0.5 \times \text{CHISQ.INV.RT}((1 - \text{CL})/2, 2 \times (N + 1)); \quad (\text{A.7})$$

the function CHISQ.INV.RT returns the inverse of the right-tailed probability of the chi-squared distribution². If $N=0$ the Upper- N depends on the confidence level.

¹<https://www.excelfunctions.net/excel-chisq-inv-function.html>

²<https://www.excelfunctions.net/excel-chisq-inv-rt-function.html>

Appendix B

Least-square circle fit

The following method allows to find the best circle, using the least square method, that fits a set of points $\{(x_i, y_i | 0 \leq i \leq N)\}$ [61]. Define

$$\bar{x} = \frac{1}{N} \sum_i x_i, \quad \bar{y} = \frac{1}{N} \sum_i y_i, \quad (\text{B.1})$$

and let $u_i = x_i - \bar{x}$, $v_i = y_i - \bar{y}$ for $0 \leq i \leq N$. The problem is first solved in the (u, v) coordinates and then it's transformed back into (x, y) coordinates. The circle center coordinates are (u_c, v_c) and its radius is R . We have to minimize the parameter $S = \sum_i (g(u_i, v_i))^2$, where $g(u, v) = (u - u_c)^2 + (v - v_c)^2 - \alpha$, $\alpha = R^2$. To do that, we differentiate $S(\alpha, u_c, v_c)$:

$$\frac{\partial S}{\partial \alpha} = 2 \sum_i g(u_i, v_i) \frac{\partial g}{\partial \alpha}(u_i, v_i) = -2 \sum_i g(u_i, v_i). \quad (\text{B.2})$$

The derivative is zero if, and only if,

$$\sum_i g(u_i, v_i) = 0. \quad (\text{B.3})$$

Using (B.3), we can obtain

$$\begin{aligned} \frac{\partial S}{\partial u_c} &= 2 \sum_i g(u_i, v_i) \frac{\partial g}{\partial u_c}(u_i, v_i) \\ &= 2 \sum_i g(u_i, v_i) 2(u_i - u_c)(-1) \\ &= -4 \sum_i u_i g(u_i, v_i) + 4u_c \sum_i g(u_i, v_i). \end{aligned} \quad (\text{B.4})$$

In presence of (B.3), $\partial S / \partial u_c = 0$ is verified only if

$$\sum_i u_i g(u_i, v_i) = 0, \quad (\text{B.5})$$

and, in a similar way, for $\partial S/\partial v_c = 0$

$$\sum_i v_i g(u_i, v_i) = 0. \quad (\text{B.6})$$

By expanding equation (B.5) we can obtain

$$\sum_i u_i [u_i^2 - 2u_i u_c + u_c^2 + v_i^2 - 2v_i v_c + v_c^2 - \alpha] = 0. \quad (\text{B.7})$$

By defining $S_u = \sum_i u_i$, $S_{uu} = \sum_i u_i^2$, etc., we can rewrite the previous equation (B.7) as

$$S_{uuu} - 2u_c S_{uu} + u_c^2 S_u + S_{uvv} - 2v_c S_{uv} + v_c^2 S_u - \alpha S_u = 0, \quad (\text{B.8})$$

but $S_u = 0$, and thus

$$u_c S_{uu} + v_c S_{uv} = \frac{1}{2}(S_{uuu} + S_{uvv}), \quad (\text{B.9})$$

and similarly from equation B.6, since $S_v = 0$, we can obtain

$$u_c S_{uv} + v_c S_{vv} = \frac{1}{2}(S_{vvv} + S_{vuu}). \quad (\text{B.10})$$

By simultaneously solving (B.9) and (B.10) we can obtain (u_c, v_c) and then the circle center coordinate back in the (x, y) coordinate system: $(x_c, y_c) = (u_c, v_c) + (\bar{x}, \bar{y})$. To obtain the radius R , the equation B.3 has to be expanded and using $S_u = S_v = 0$ we obtain

$$N(u_c^2 + v_c^2 - \alpha) + S_{uu} + S_{vv} = 0, \quad (\text{B.11})$$

and thus

$$\alpha = u_c^2 + v_c^2 + \frac{S_{uu} + S_{vv}}{N}. \quad (\text{B.12})$$

The radius R is $R = \sqrt{\alpha}$.

Appendix C

ECQA Mapping Scheme

In this appendix the detailed mapping between the CLAROs channel on the Front-End Boards (FEBs) and the Multi-Anode Photo Multiplier Tubes (MaPMTs) anode in the Elementary Cells (ECs) is reported. In figure C.1 the mapping scheme for an R-type EC is reported. The same scheme is valid for each R-type EC. The UART information is missing because every R-type EC of the load has different UART connectors associated: 0 and 3 for the EC3 (bottom-left), 1 and 2 for the EC0 (top-left), 4 and 7 for the EC2 (bottom-right) and 5 and 6 for the EC1 (top-right).

In figure C.2 the mapping scheme for an H-type EC is reported. The same scheme is valid for each H-type EC. The UART information is missing because every H-type EC of the load has different UART connectors associated: 0 for the EC3 (bottom-left), 1 for the EC0 (top-left), 4 for the EC2 (bottom-right) and 5 for the EC1 (top-right).

FEB0 CHIP7 CH7	FEB0 CHIP7 CH5	FEB0 CHIP6 CH2	FEB0 CHIP6 CH0	FEB1 CHIP7 CH7	FEB1 CHIP7 CH5	FEB1 CHIP6 CH2	FEB1 CHIP6 CH0
FEB0 CHIP7 CH1	FEB0 CHIP7 CH0	FEB0 CHIP6 CH7	FEB0 CHIP6 CH6	FEB1 CHIP7 CH1	FEB1 CHIP7 CH0	FEB1 CHIP6 CH7	FEB1 CHIP6 CH6
FEB0 CHIP5 CH6	FEB0 CHIP5 CH4	FEB0 CHIP4 CH3	FEB0 CHIP4 CH1	FEB1 CHIP5 CH6	FEB1 CHIP5 CH4	FEB1 CHIP4 CH3	FEB1 CHIP4 CH1
FEB0 CHIP5 CH2	FEB0 CHIP5 CH0	FEB0 CHIP4 CH7	FEB0 CHIP4 CH5	FEB1 CHIP5 CH2	FEB1 CHIP5 CH0	FEB1 CHIP4 CH7	FEB1 CHIP4 CH5
FEB0 CHIP3 CH5	FEB0 CHIP3 CH7	FEB0 CHIP2 CH0	FEB0 CHIP2 CH2	FEB1 CHIP3 CH5	FEB1 CHIP3 CH7	FEB1 CHIP2 CH0	FEB1 CHIP2 CH2
FEB0 CHIP3 CH1	FEB0 CHIP3 CH3	FEB0 CHIP2 CH4	FEB0 CHIP2 CH6	FEB1 CHIP3 CH1	FEB1 CHIP3 CH3	FEB1 CHIP2 CH4	FEB1 CHIP2 CH6
FEB0 CHIP1 CH6	FEB0 CHIP1 CH7	FEB0 CHIPO CH0	FEB0 CHIPO CH1	FEB1 CHIP1 CH6	FEB1 CHIP1 CH7	FEB1 CHIPO CH0	FEB1 CHIPO CH1
FEB0 CHIP1 CH0	FEB0 CHIP1 CH2	FEB0 CHIPO CH5	FEB0 CHIPO CH7	FEB1 CHIP1 CH0	FEB1 CHIP1 CH2	FEB1 CHIPO CH5	FEB1 CHIPO CH7
64	63	62	61	60	59	58	57
56	55	54	53	52	51	50	49
48	47	46	45	44	43	42	41
40	39	38	37	36	35	34	33
32	31	30	29	28	27	26	25
24	23	22	21	20	19	18	17
16	15	14	13	12	11	10	9
8	7	6	5	4	3	2	1

Figure C.2: Scheme representing the association between the single MaPMT anodes and CLARO channels on the FEBs for an H-type EC. On the top side the CLARO channels at which the anodes are connected are reported, with the channel ID parameters at which the channel is associated (FEB and CHIP). On the bottom side the MaPMT anode numbering convention is reported.

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