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CICLO XXX

COORDINATORE Prof. Stefano Trillo

LOW-FREQUENCY LOAD-PULL FOR TRANSISTOR CHARACTERIZATION AND MICROWAVE POWER AMPLIFIER DESIGN

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Preface

The design of RF systems with high energy-efficiency is very important for mobile communications. These systems are based on integrated and hybrid RF circuits, with high production costs, which lead to stringent constraints on the exact prediction of the final prototype performance. The design of RF circuits is typically carried out by means of CAD tools that allow estimating the final performance with an accuracy depending on the accuracy of the available component models. In order to improve their prediction capability, transistor models used in the design of microwave amplifiers can be identified by measurements performed with load-pull systems, that are able to put the transistor under actual operating conditions. These measurement systems are also used to directly estimate the performance of the final amplifier to be designed in different operating classes, from the most common ones as A, AB, B or C to the harmonic-manipulated ones, where the load terminations must be suitably controlled also at harmonics.

In high-frequency load-pull systems, it is complex to apply the theoretical terminations required by the *waveform engineering* theory at the transistor current-generator plane, due to the linear and nonlinear dynamic effects of the transistor that tend to hide the intrinsic device behavior. On the contrary, the required electrical regime can be easily imposed at the transistor current source by using low-frequency load-pull systems; furthermore, by means of a procedure called "*nonlinear embedding*", it is possible to obtain the source/load terminations at the design frequency that guarantee the desired performance. Low-frequency load-pull systems can be implemented by using conventional instrumentation present in each microwave laboratory, i.e., arbitrary function generator, oscilloscope, dc voltage supplies and vector network analyzer. These instruments are definitely cheaper than the expensive setups required for microwave load-pull measurements.

In the load-pull systems, the load terminations can be synthesized in an active or passive way. In the active technique, the load is synthesized by applying appropriate incident signals at the output port of the transistor, but this procedure is often complex and time-consuming. The alternative is the passive technique that uses passive components, such as tuners and multiplexers, to apply the load at the fundamental frequency and at the harmonics. In the high-frequency version, these components are usually implemented in

microstrip or coaxial technology, while, in their low-frequency version, lumped components, i.e., inductors, resistors, and capacitors, can be adopted.

This thesis is mainly focused on the design and implementation of circuit and component solutions to implement a low-frequency passive load-pull system. In particular, a power bias tee able to handle up to 500 Vdc, 3.4 Adc and RF power of 300 W (at 725 MHz) was designed. Moreover, a low-frequency multiplexer capable of handling load terminations up to the fourth harmonic and a low-frequency resistive tuner capable of handling a minimum power of 15 W, were designed.

The thesis is organized as follows. In the first chapter, the main measurement systems and techniques used to implement the so-called "*waveform engineering"* design technique will be dealt with. The second chapter will describe the design of different components required for the efficient implementation of a passive low-frequency load-pull system. Finally, in the third chapter the designs of two RF power amplifiers will be presented as application examples of the developed measurement setup and the waveform engineering approach.

Prefazione

La progettazione dei sistemi RF ad alta efficienza energetica è molto importante per le comunicazioni mobili. Questi sistemi utilizzano circuiti RF in forma integrata e ibrida con alti costi di produzione che impongono vincoli stringenti sulla corretta predizione delle prestazioni del prototipo finale. Il progetto di circuiti RF è realizzato mediante strumenti CAD che consentono di stimare le prestazioni finali con una accuratezza dipendente dall'accuratezza dei modelli utilizzati. In particolare, i modelli di transistor utilizzati nella progettazione di amplificatori a microonde sono spesso ottenuti da misure eseguite mediante sistemi di load-pull. Questi sistemi possono anche essere utilizzati per caratterizzare le prestazioni dell'amplificatore finale in diverse classi operative, da quelle più comuni come A, AB, B o C a quelle denominate a "*manipolazione armonica*", dove le terminazioni del carico devono essere gestite in modo adeguato alla frequenza fondamentale e alle armoniche.

Nei sistemi load-pull ad alta frequenza, è complesso applicare le terminazioni teoriche al piano del generatore di corrente del transistor, a causa della rete parassita del transistor e degli effetti non lineari dinamici. Al contrario, sfruttando i sistemi di load-pull a bassa frequenza, risulta piuttosto semplice imporre le terminazioni al piano del generatore di corrente del transistor; inoltre, mediante una procedura chiamata "*nonlinear embedding*", è possibile ottenere le prestazioni e le relative terminazioni di carico alla frequenza di progetto dell'amplificatore. I sistemi di load-pull a bassa frequenza possono essere implementati utilizzando strumentazione convenzionale presente in ogni laboratorio a microonde, cioè generatore di funzioni arbitrarie, oscilloscopio, alimentatori a tensione continua e analizzatore vettoriale di reti. Questi strumenti sono decisamente più economici rispetto a quanto richiesto per eseguire misure di load-pull a microonde.

Nei sistemi di load-pull, le terminazioni di carico e sorgente possono essere sintetizzate in modo attivo o passivo. Nella tecnica attiva, il carico viene sintetizzato applicando opportune forme d'onda all'ingresso e all'uscita del transistor, ma questa procedura è spesso complessa e richiede molto tempo. L'alternativa è la tecnica passiva che utilizza componenti passivi come tuner e multiplexer per applicare il carico alla frequenza fondamentale e alle armoniche. Nella versione ad alta frequenza, questi componenti sono solitamente implementati in tecnologia a microstriscia o coassiale, mentre, nella loro

versione a bassa frequenza, possono essere adottati componenti concentrati, come induttori, resistori e condensatori.

Questa tesi si concentra principalmente sulla progettazione e l'implementazione di soluzioni circuitali e componenti per realizzare un sistema di load-pull passivo a bassa frequenza. In particolare, è stata progettata una bias tee di potenza in grado di gestire fino a 500 Vdc, 3.4 Adc e una potenza RF di 300 W (a 725 MHz). Inoltre, sono stati progettati un multiplexer a bassa frequenza in grado di gestire i carichi di terminazione fino alla quarta armonica e un tuner resistivo a bassa frequenza in grado di gestire una potenza minima di 15 W.

La tesi è organizzata come segue. Nel primo capitolo verranno trattati i principali sistemi di misura e le tecniche utilizzate per implementare la metodologia di progetto nota come "*waveform engineering*". Il secondo capitolo descriverà la progettazione di diversi componenti necessari all'implementazione di un sistema di load-pull a bassa frequenza. Infine, nel terzo capitolo, verrà presentato il progetto di due amplificatori di potenza RF come esempi applicativi del setup di misura sviluppato e del *waveform engineering*.

Chapter 1

Large-Signal Characterization of Microwave Transistors and Power Amplifier Design

1.1. Introduction

In modern RF equipment for mobile applications or broadcasting stations, the concept of energy saving has become increasingly important. The electronic amplifier represents an analog component present in each of these systems and it allows increasing the power level of the received or transmitted signals. Many efforts made since 1920 have allowed improving the efficiency of transmission equipment by means of new amplifier topologies [1].

The classes of power amplifiers (PA) are conventionally indicated by letters that identify the characteristics and performance of the amplifier. There are two fundamental classes of amplification: the conduction angle classes (which uses the letters A, B, C, or AB) and the waveform-engineered classes (which uses the letters D, E, F, G, H, S) [2].

The main figures of merit of a power amplifier are: bandwidth, gain, efficiency and linearity. The bandwidth is the range of frequency in which the amplifier has a given performance, the gain is the ratio of output to input power or voltage amplitude, and is usually measured in decibel (dB). Finally, the efficiency represents the rate of supplied power that is converted into a useful signal at the output, and the linearity measures the ability of an amplifier, which is a strongly nonlinear circuit, to behave like a linear component.

The conduction-angle classes are related to the time period that the amplifier is conducting current, expressed as a fraction of the period of a sinusoidal signal waveform applied to the input. A class-A amplifier is conducting during all the entire signal period; class B only for one-half of the signal period, class C for less than half the period. If one reduces the conduction angle, the efficiency increases and the linearity of the amplifier is reduced as well as the output power. Waveform-engineered classes use suitable harmonic terminations at the output of the device in order to optimize the tradeoff between output power and efficiency, and they are more often used to build narrow-band amplifiers [2].

The choice of the device output termination is particularly important for the efficiency, and must be determined considering actual transistor operation, i.e., a large-signal regime as described in [3]. The load-pull systems allow one to plot on the Smith chart suitable "contours", namely closed lines that identify, for a fixed parameter (e.g, input power or gain compression level), the reflection coefficients (and therefore the impedances) which lead to the same power, efficiency or gain. The traditional microwave load-pull systems are very expensive, but since from the historical Cripps's contribution [4], efforts have been made to draw load-pull contours or get useful information for power amplifier design, by using simulations or less expensive measurement setups. After briefly describing the main load-pull systems, a method to get suitable information for power amplifier design, based on simulations and low-frequency load-pull measurements, will be described in the following paragraphs.

1.2. High-Frequency Load-Pull Systems

The optimal power matching under small signals does not represent the optimum condition under a large-signal excitation for a power amplifier, as described in [3]. For such a reason, the load-pull measurement systems can be used to investigate the performance under large-signal excitations by varying the load terminations. The load-pull systems are of an *active* or *passive* type, and allow controlling the impedances at the fundamental and harmonic frequencies to implement different operating classes for the amplifiers (e.g., F, inverse F, J, tuned load) [2].

In the passive technique, the impedances applied to the transistor are modified by a mechanical component called *tuner*, built with microstrips and stubs. However, the range of impedances that can be synthesized through passive load-pull systems is limited by the tuner losses and network connections. These losses, introduced by cables, connectors, transistor package, bias tees, and other elements inserted into the measurement system, prevent the achievement of impedances near the Smith chart edge. This is particularly critical when high-power devices, requiring very low termination impedances, must be characterized.

The block diagram of a passive load-pull measurement system is shown in figure 1.1 where an oscillator imposes the signal to the DUT (Device Under Test), while the tuner at the input, by sweeping the source impedance, allows one to optimize the input matching to ensure the maximum power transfer to the device. Finally, the tuner at the output port, by

sweeping the load impedance, gets the impedance that ensures the best performance for the device [2], while the "acquisition section" acquires the incident and reflected waves at the input and output port of the DUT that are necessary to determine the performance. The "acquisition section" is generally constituted by a Vector Network Analyzer (VNA).

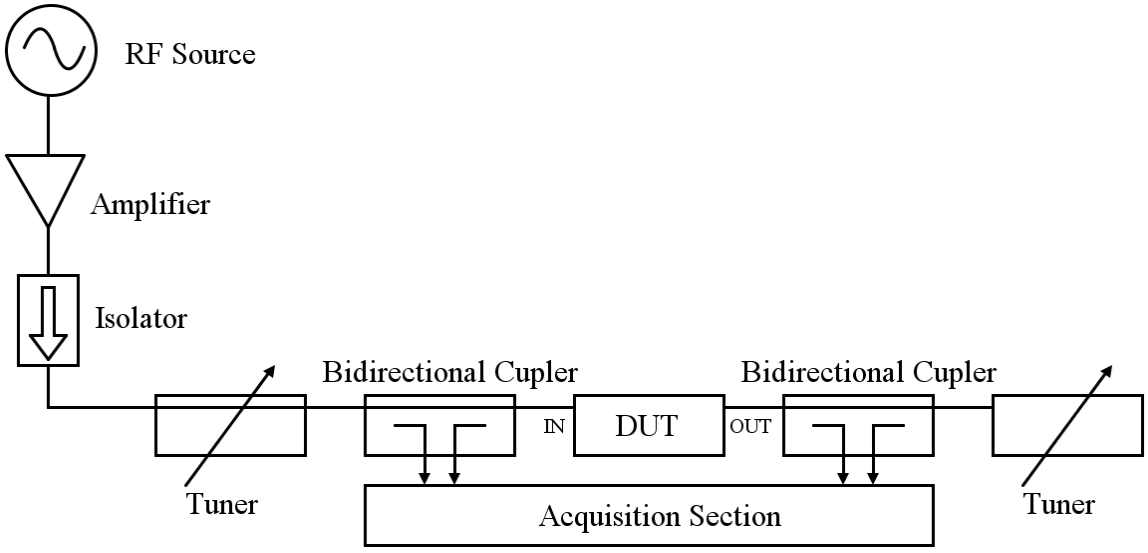


Figure 1.1 – Block diagram of a passive load-pull system.

Multi-harmonic passive tuners are very expensive and the challenge for the manufacturers is to create large bandwidth tuners and ensure a good isolation between the different harmonic frequencies that are usually three: the fundamental (f_0), the second ($2f_0$) and the third ($3f_0$) harmonic. Figure 1.2 shows the block diagram of a multi-harmonic tuner realized with a microwave multiplexer [3].

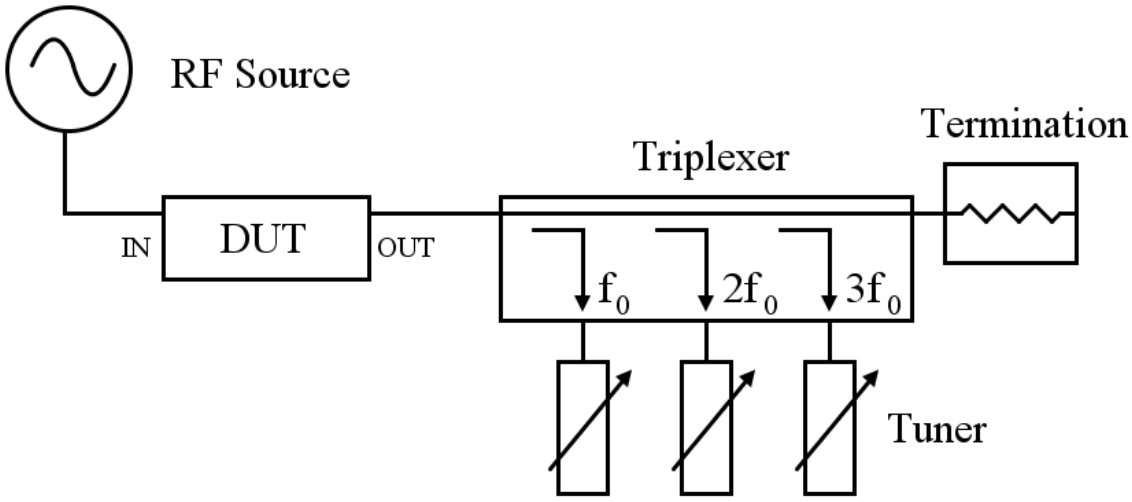
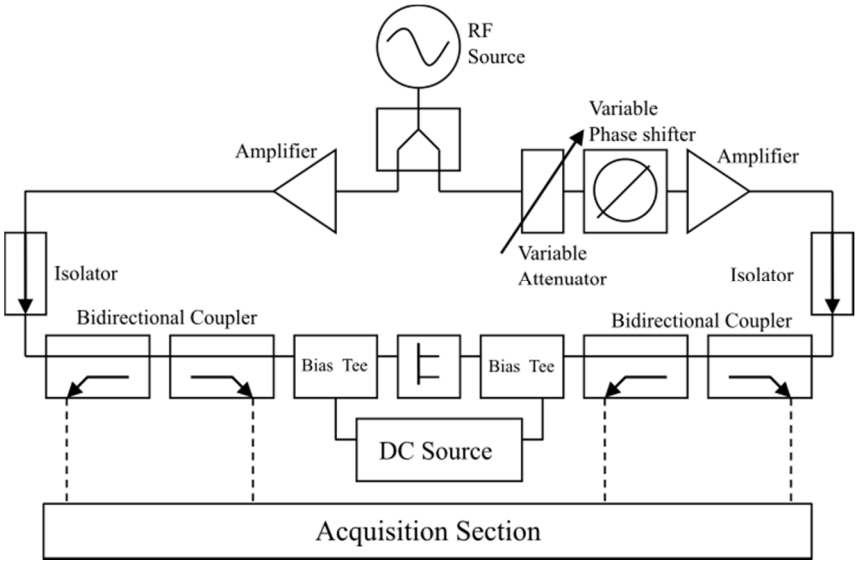


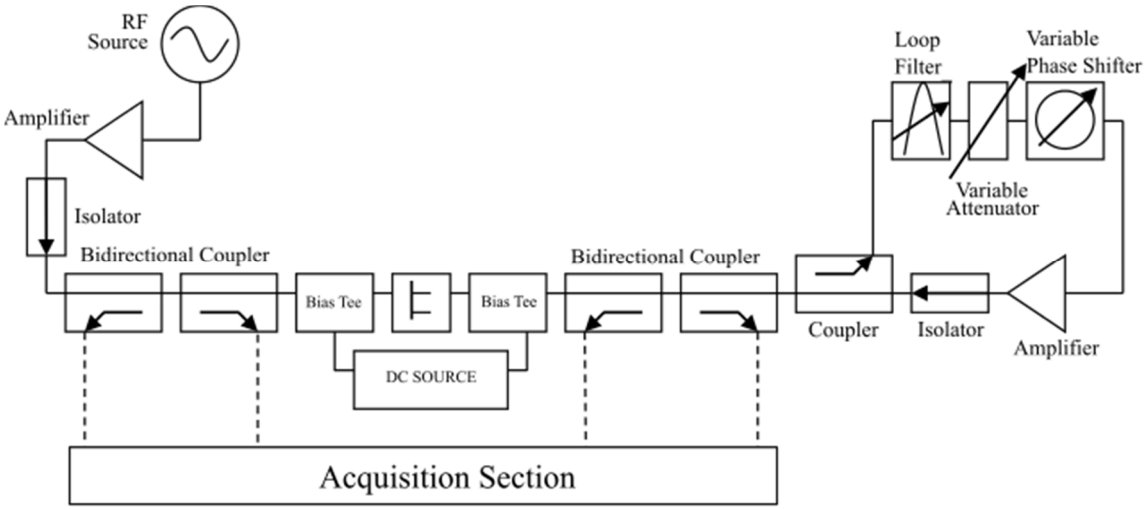
Figure 1.2 – Block diagram of a load-pull system based on a multiplexer.

The active load-pull measurement technique is based on injecting the signal directly in the input/output port of the DUT for synthesizing a specific load impedance. In fact, the

required load impedance must be generated by changing the relative phase and amplitude of the incident waves to the device [2]. The block diagram of an active load-pull measurement system is shown in figure 1.3a.



a)



b)

Figure 1.3 – Block diagram of an active load-pull system (a) and block diagram of an active-loop load-pull system (b).

The main drawback of this measurement technique is related to the difficulty of controlling the synthesized load, i.e., the reflection coefficient when varying the amplitudes and phases of the voltage waves applied to the device ports, due to the nonlinear behavior of the DUT. To this end, suitable controlling algorithms are required.

The active-loop load-pull measurement technique shown in Figure 1.3b, which has the advantage of synthesizing and controlling reflection coefficients independently. The difference with respect to the system in Figure 1.3a is that at the output port of the DUT a

portion of the reflected wave is used to generate the incident wave (Figure 1.3b). This feature mitigates the problems associated to the variation of the output load while the input signal varies. The main disadvantage of this technique is the possibility of oscillations within the ring-loop [2].

To conclude, the active load-pull systems allow covering all the impedances on the Smith chart, compared to passive systems, where the mechanical resolution of the tuner and the losses of the tuner and multiplexer limit the Smith chart coverage. However, in the passive systems, the impedance does not depend on the power at the DUT output and the tuner control is relatively easy.

1.3. Nonlinear FET Modelling and Waveform Engineering

Figure 1.4 shows the nonlinear model of a generic field-effect transistor which is composed of three blocks: the *resistive core*, *capacitive core* and *linear extrinsic parasitic network*. The resistive core describes the low-frequency I/V characteristics, but also it encloses several phenomena such as device breakdown and the Schottky diode current [5,6]. The description of the resistive core can be derived from dynamic I/V measurements or, more effectively, by means of low-frequency load-pull measurement systems which will be described later.

The capacitive core describes the dynamic nonlinear high-frequency effects (i.e., nonlinear capacitances and related non-quasi-static effects) [5,6], and it can be identified by means of small-signal and/or large-signal measurements.

Finally, the linear extrinsic parasitic network describes the transistor access structures as well as the metallization resistances or leakage towards the substrate that can be identified by means of suitable small-signal measurements and/or electromagnetic simulations [5,6].

Through the knowledge of these blocks, it is possible to determine the optimum impedances at the Current Generator Plane (CGP) and then to obtain those at the Extrinsic Plane (EP) of the device (Figure 1.4) at each frequency, by means of CAD systems. This method is known as "*waveform engineering*" and can be used both for quasi-linear and high-efficiency classes of amplification [6]. We want to emphasize that, in the absence of reactive elements at the CGP, the load that maximizes output power and/or efficiency is resistive.

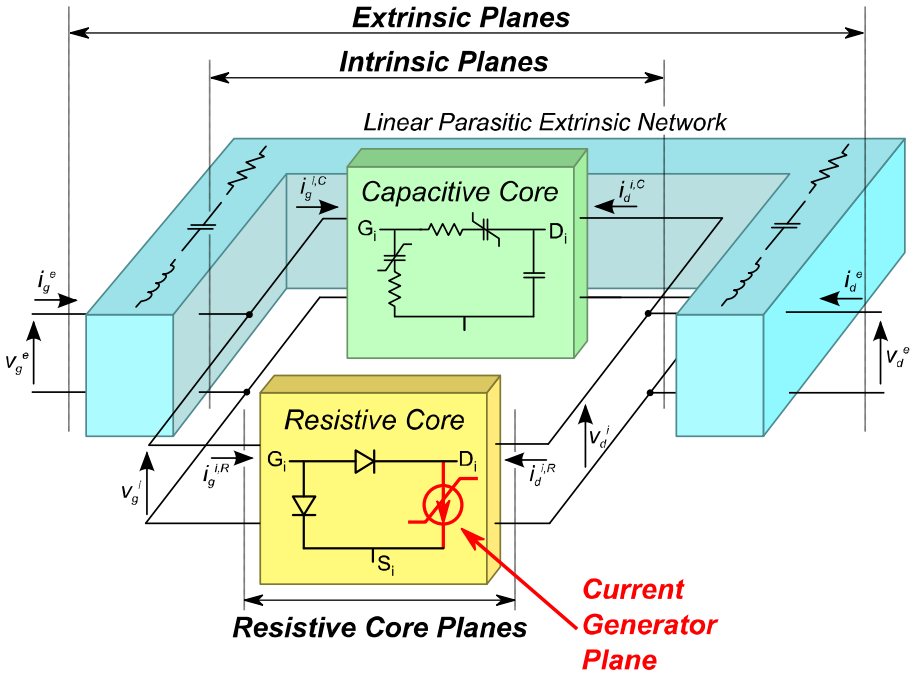


Figure 1.4 – Nonlinear model of a field-effect transistor (FET).

To design circuits by using these models, the designer must have access to every part of the model for monitoring the load line, and therefore the waveforms, at the CGP following, for instance, the guidelines defined in [8-14] to properly synthesize the operating class of interest. We will refer to this kind of approach with the term *model-based* waveform engineering.

On the other side, the proliferation in the last twenty years of vector measurement systems [15-21] enabling the measurement of transistor waveforms at microwave frequencies, has given a sudden boost to the idea of properly shaping the transistor waveforms. It should be clearly pointed out that, although waveforms are gathered at microwave frequencies, it is always necessary to de-embed these waveforms in order to apply the waveform engineering concept at the CGP. In other words, the waveforms to be correctly shaped are those at the CGP. We will indicate this kind of approach as *measurement-based* waveform engineering.

Whichever the adopted solution is for applying the waveform engineering, modelling and measurement issues are always both involved. When a measurement-based approach is adopted, it is always necessary to translate the waveforms at different reference planes and this operation at least requires a model of the parasitic elements [22-26]. On the other side, when a model-based approach is used, linear and nonlinear measurements must be necessarily used for extracting and validating the model. Therefore, it appears clear that

the division between measurement- and model-based approaches is not so strict: it is only a useful schematization for describing the different approaches proposed during these years.

Finally, it must be recalled that the term *waveform engineering* was introduced in [15] by Tasker. It defines a demarcation that correctly identifies the waveform engineering approaches. In fact, many nonlinear measurement techniques that allow one to accurately characterize the transistor behavior under realistic operation do exist (e.g., [27-29]), but they do not belong to waveform engineering approaches.

1.4. Model-Based Waveform Engineering

The model-based approaches are inspired by the Cripps' load line theory [31,32] and have their epistemological roots in the large amount of excellent contributions [4,32-37] describing the correct current and voltage waveforms at the CGP for achieving a selected class of amplification (e.g., A, F, J) to which a well-defined transistor performance (in terms of output power, efficiency, linearity, etc.) is inherently associated.

The most widely used amplifier design technique is based on performing source- and load-pull simulations in the CAD environment, at the fundamental and harmonic frequencies. The swept source and load impedances are chosen at the EP, so the nonlinear model has to provide access to the CGP in order to analyze the corresponding waveforms. Foundry models typically provide access to the CGP, although the achievable information can be limited due to confidentiality issues. As an example, in some cases the current waveform at the CGP can be provided as an output of the Harmonic Balance (HB) analysis, whereas the access at the Intrinsic Plane (IP) in Figure 1.4 is prevented for hiding the parasitic-network description, which may represent a very sensitive information. Foundries implement these users' limitations by supplying compiled models. An adequate modelling service, providing access to the CGP, is a key feature for commercial foundries.

Once source- and load-pull simulations have been performed and the CGP waveforms shaped according to the desired class of operation, the impedances to be synthesized at the EP are immediately available over the required frequency range and the next step consists in the input and output matching-network design. Nevertheless, this is strictly true only in the particular situation that a single-transistor amplifier must be designed. In a general case, the PA consists of different stages (e.g., driver and

power stages), each one paralleling more than one transistor. In this case, the described procedure has to be repeated for each stage and during the matching-network design, special care should be taken in assuring that all the devices in the same stage experience the same load line (i.e., the same current and voltage waveforms at the CGP). A significant case is represented by the transistor power bars that are typically used in the design of high-power microwave amplifiers. Figure 1.5 shows an internally matched C-band single-stage high-power amplifier (47 dBm) for pulsed radar applications. The design was carried out by exploiting a GaN 16-mm power bar, consisting of eight identical transistors with 0.5-µm gate length. The drain voltage and current waveforms at the CGP for the unit cell along with the corresponding load line are reported in Figure 1.6.

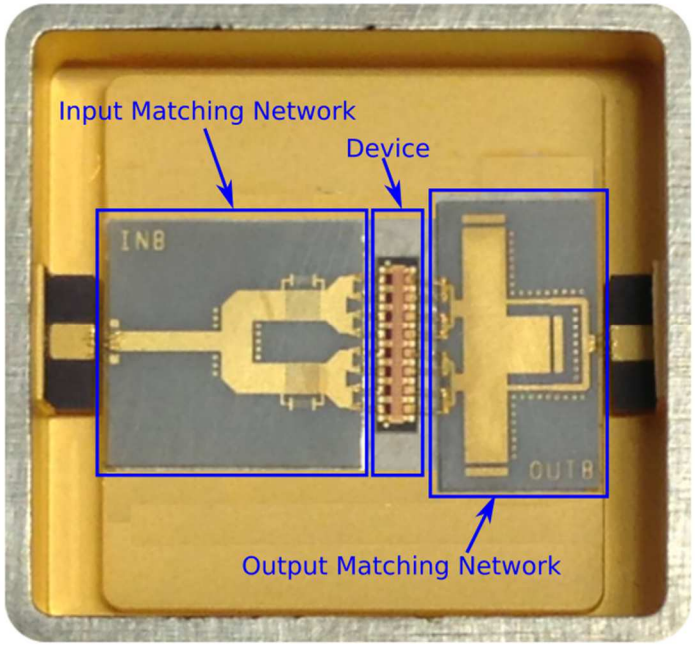


Figure 1.5 – Broadband C-band internally matched high-power amplifier (47 dBm) for pulsed radar applications. (Courtesy of MEC srl)

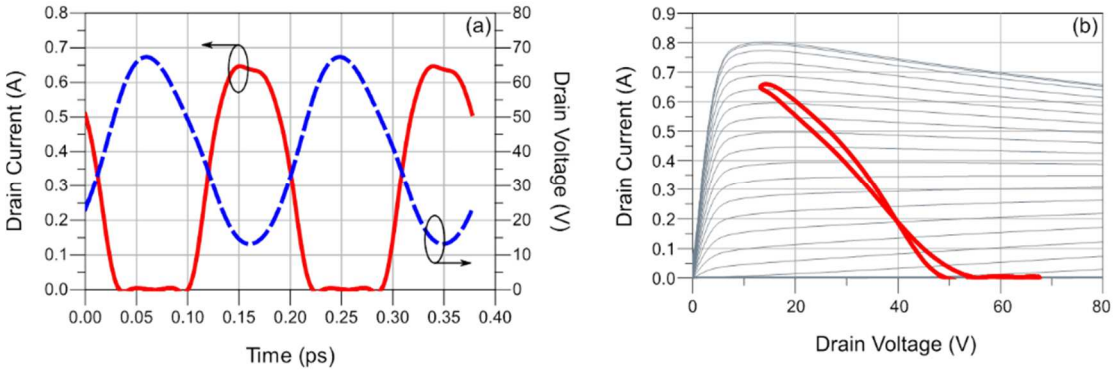


Figure 1.6 – Simulated voltage and current waveforms (a) at the current-generator plane and relative load line (b) of the elementary cell (periphery 2 mm). Bias condition: V_{DQ} = 40 V, I_{DQ} = 50 mA.

Once the load line for the single transistor has been selected according to the desired transistor operation at the CGP, the matching-network design requires an additional *symmetrization* step. Since the optimum waveform shapes are defined at the CGP, it makes no surprise that the symmetric transistor operation must be guaranteed at that plane. Figure 1.7 shows the load lines at the CGP corresponding to the different transistors in the power bar from the outermost to the innermost (for symmetry reasons, the other four load lines are superimposed to the showed ones). Finally, in Figure 1.8 the measured PA performance in terms of output power, Power Added Efficiency (PAE), and power gain are reported.

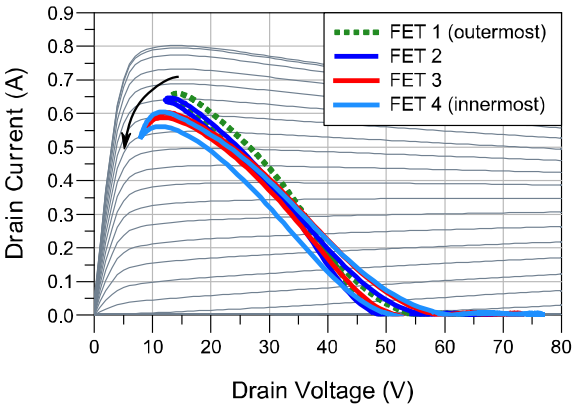


Figure 1.7 – Load lines at the current-generator plane corresponding to the different elementary cells that constitute the power bar. The dotted line represents the outermost transistor. Bias condition: V_{DQ} = 40 V, I_{DQ} = 400 mA.

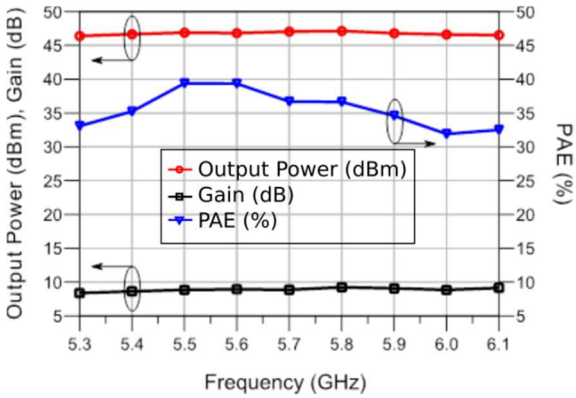


Figure 1.8 – Measured power amplifier performance. Pulse width 50 µs, duty cycle 10%. Bias condition: V_{DQ} = 40 V, I_{DQ} = 400 mA.

When designing a power amplifier, the model-based approaches are undoubtedly the most used ones in the framework of waveform engineering and the reason is simple: a transistor model is necessary not only for defining the optimum source and load conditions, but also for investigating the device behavior under more complex excitations (e.g., modulated signals), for checking stability, for performing yield analysis, and so on. On the other hand, the weak point of these approaches is their accuracy, which is inherently linked to the accuracy of the adopted model. Foundry models are typically tailored on specific transistor operations and selected bias conditions, and, therefore, are less accurate when used for the design of amplifiers in different classes of operation (e.g., harmonic-manipulated amplifiers) or under bias conditions different from the one considered by the foundry in the model extraction phase. This is one of the reasons why also measurement-based approaches in the last years have become more and more appealing.

1.5. Measurement-Based Waveform Engineering

The microwave setups described in 1.2 can be conveniently used to characterize devices at large signal and high frequency. These nonlinear high-frequency measurement systems allow managing high powers and the synthesis of the terminations at fundamental frequency and harmonics, that are necessary to determine the load condition for the synthesis of matching networks at the work frequency. As previously described, high-frequency setups are commonly divided into "passive" and "active" systems, depending on whether they use passive tuners or signal sources to synthesize terminations at the input and output ports of the DUT [15-19]. As regarding the acquisition section, different architectures have been proposed in the last decades and they are commonly divided into "mixer-based" [54, 55] and "oscilloscope-based" systems [56, 57]. Mixer-based setups share the architecture of the acquisition section of a VNA and, therefore, provide a very high-dynamic range. In a mixer-based setup, the harmonic frequencies of a signal generated by a nonlinear DUT are acquired one-by-one and this forces the signal that must be acquired to be repetitive. The same requirement applies to those systems based on equivalent-time sampling techniques, like equivalent-time oscilloscopes or harmonic-sampler based large-signal network analyzers. Nevertheless, differently from a mixer-based architecture, the whole spectral content is acquired at once resulting in a shorter measurement time but in a poorer dynamic range. Whereas for the systems described above the signals to be measured must be repetitive, this is not the case for setups based on real-time oscilloscopes. The latter have been developing very quickly in the last years and are becoming a valid alternative to perform waveform measurements at microwave frequencies, although they provide a dynamic range lower than a mixer-based setup. Clearly all these architectures have their own pros and cons and the selection of one solution rather than the others depends on the targeted application, on the targeted accuracy, and, eventually, on the cost.

Electrical variables measured by means of the systems mentioned above are actually at the EP of the DUT (see Figure 1.4). This means that the contribution of all linear parasitic effects and nonlinear capacitances is included in these measurements. Depending on the operating frequency, these effects can hide the actual waveforms at CGP, thus a suitable de-embedding procedure becomes crucial to take a look at what is really happening at such plane. The problem of retrieving electrical variables at the CGP is clearly nonlinear thus exploiting a nonlinear device model to de-embed data is the obvious choice [58]. In spite

of that, it is possible to treat the problem using linear approximations [38] with the caution that the accuracy level achieved at the CGP must be carefully checked [58].

When designing a power amplifier, the conventional DC I/V measurements may provide a starting point for estimating the best device load line according to the requirements [38]. However, it is well demonstrated that such data are not an accurate description of the I/V characteristics of the device current generator at microwaves, especially for new technologies (e.g., GaN). This is due to the influence of the so-called low-frequency dispersion, which includes a whole set of phenomena related to the thermal and trap states of an electron device [39-43]. The low-frequency attribute is related to the theoretical and experimental evidence [44-46] that the involved time constants are typically higher than 1 μs, providing a cut-off frequency below the megahertz range. Above that, thermal and trapping phenomena cannot follow the instantaneous values of the signals, and remain related to the average values of the dissipated power and of the electric field; this justifies the assumption that the current generator is a frequency independent element above the low-frequency dispersion cut-off.

Measuring the current-generator behavior under actual operating conditions at microwave frequencies is not practical since the effects of the device parasitic elements and the intrinsic capacitances hide the CGP as the frequency increases. However, it is possible to identify a bandwidth above the low-frequency dispersion cut-off where the influence of the reactive phenomena is negligible, giving direct access to the current-generator waveforms consistent with microwave operation. Measuring a microwave device within this bandwidth, allows one to directly monitor the current-generator intrinsic variables. To this aim, the setup shown in Figure 1.9 [44] can be adopted. It implements a low-frequency Large-Signal Network Analyzer (LSNA) with load-pull capabilities, dedicated to the characterization of microwave devices in the megahertz bandwidth (e.g., fundamental frequency of 2 MHz). The bias point of the DUT is set by a DC source, whereas its input port is excited with an RF source at the fundamental and harmonic frequencies. The synthesis of the load condition cannot be performed by conventional mechanical passive tuners for such a low frequency, but other possibilities can be exploited. These include the use of an active synthesis by injecting a second signal at the output port of the device. Such a signal can contain not only the fundamental component but also the harmonics. By tuning their amplitudes and relative phases, one can obtain any load condition and shape the current-generator waveforms according to the desired theoretical class of operation [8-14].

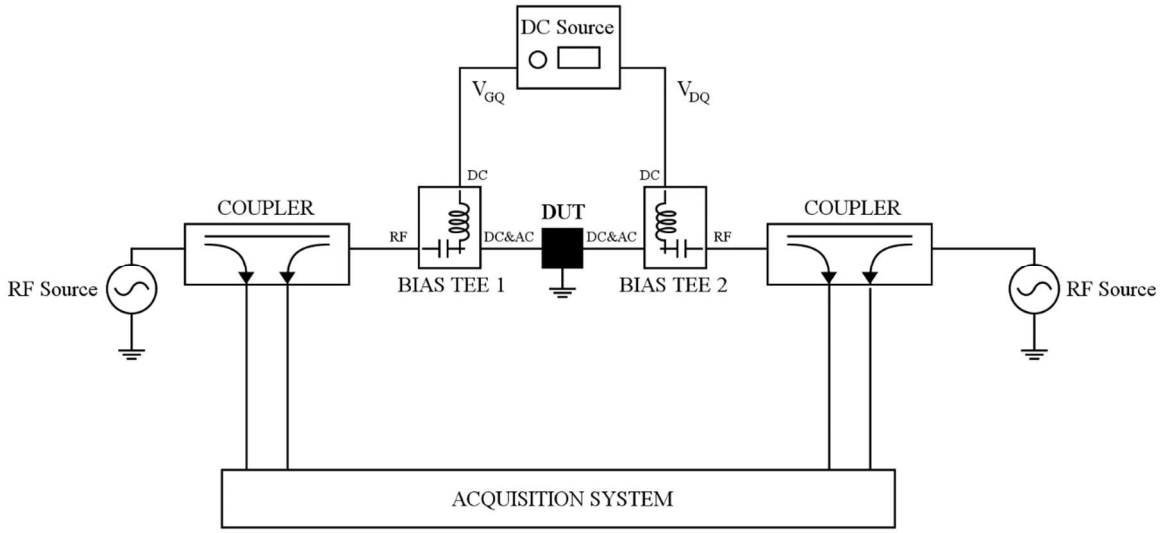


Figure 1.9 – Low-frequency LSNA setup.

In the low-frequency setup shown in Figure 1.9, incident and reflected waves are separated by means of two dual-directional couplers, connected to an acquisition system. Because of the low-frequency signals involved, the acquisition system can be a conventional 4-channel 50-Ω oscilloscope with a bandwidth sufficiently wide to get enough harmonics. As an example, considering a fundamental frequency of 2 MHz, many commercial oscilloscopes allow for the acquisition of several tens of harmonics, which are definitely enough for a typical characterization involving conventional CW signals. An alternative is the use of mixer-based instruments [44], capable of handling signals in the megahertz range.

The signal paths of the setup are characterized by means of their Scattering (S)-parameters within the bandwidth of the system. Such data are then used to post-process the acquired waveforms and shift them at the DUT reference planes. To get the current-generator voltage and current waveforms one needs to eliminate the effects of the resistive parasitic elements of the device, since at low frequency the reactive ones are negligible.

Referring to Figure 1.4, the selected low-frequency condition in the frequency domain can be written as follows:

$$I^{i,R}(k\omega_{LF}) = \begin{bmatrix} I_g^{i,R}(k\omega_{LF}) \\ I_d^{i,R}(k\omega_{LF}) \end{bmatrix}, V^{i}(k\omega_{LF}) = \begin{bmatrix} V_g^{i}(k\omega_{LF}) \\ V_d^{i}(k\omega_{LF}) \end{bmatrix}, k = -M,...,M \qquad (1)$$

where M is the number of harmonics considered and ω_{LF} is the fundamental frequency adopted for the measurements. According to the assumption of frequency independence of the current generator above the low-frequency dispersion cut-off, one can assume that for

each microwave frequency ω_{HF} a condition must exist for which the current-generator waveforms correspond to the ones measured at ω_{LF}. This statement is indeed the foundation of the nonlinear-embedding approach [47], which defines the way to transpose the low-frequency data to the microwave range, once the quantities in Equation 1 are known (i.e., measured).

The requirement for applying the nonlinear embedding is a model of both the capacitive core (i.e., intrinsic capacitances) and of the parasitic network of the device. These models are typically easier to be identified, especially if compared with the complexity of the resistive-core model, where the description of the effects of the low-frequency phenomena is not trivial [39-43]. The nonlinear-embedding approach bypasses such a problem, since the current-generator I/V behavior is directly measured.

Since the capacitive core is in parallel with the current generator, its contribution can be evaluated by applying the measured voltage phasors in Equation 1 properly shifted at the desired ω_{HF}, i.e.,

$$\begin{bmatrix} i_g^{i,C}(t) \\ i_d^{i,C}(t) \end{bmatrix} = \begin{bmatrix} \sum_{k=-M}^{M} I_g^{i,C}(k\omega_{RF}) e^{jk\omega_{RF}t} \\ \sum_{k=-M}^{M} I_d^{i,C}(k\omega_{RF}) e^{jk\omega_{RF}t} \end{bmatrix} = \sum_{k=-M}^{M} jk\omega_{RF} \mathbf{C}\left(v_{gs}^{i}(t), v_{ds}^{i}(t)\right) \begin{bmatrix} V_{gs}^{i}(k\omega_{LF}) e^{jk\omega_{RF}t} \\ V_{ds}^{i}(k\omega_{LF}) e^{jk\omega_{RF}t} \end{bmatrix} \quad (2)$$

where the capacitance matrix **C** can be identified by means of multi-bias S-parameters [47], although other modeling approaches may be implemented without any loss of generality (e.g., [48, 49]). Clearly, if non-quasi-static effects are present, they must be correctly accounted for (e.g., [49-51]).

By using Equations 1 and 2, all the intrinsic electrical variables are now known and the total intrinsic currents can be calculated as

$$\begin{bmatrix} I_g^{i}(k\omega_{RF}) \\ I_d^{i}(k\omega_{RF}) \end{bmatrix} = \begin{bmatrix} I_g^{i,R}(k\omega_{RF}) + I_g^{i,C}(k\omega_{RF}) \\ I_d^{i,R}(k\omega_{RF}) + I_d^{i,C}(k\omega_{RF}) \end{bmatrix}, k = -M,...,M \quad (3)$$

where the resistive currents have been properly shifted at ω_{HF} as well. As a final step, one can include the effect of the parasitic network. In particular, by using its hybrid matrix description H, it is a straightforward operation to shift the intrinsic data at the EP:

$$\begin{bmatrix} V_{gs}^{e}(k\omega_{RF}) \\ V_{ds}^{e}(k\omega_{RF}) \\ I_{g}^{e}(k\omega_{RF}) \\ I_{d}^{e}(k\omega_{RF}) \end{bmatrix} = \mathbf{H}^{-1}(k\omega_{RF}) \begin{bmatrix} V_{gs}^{i}(k\omega_{RF}) \\ V_{ds}^{i}(k\omega_{RF}) \\ I_{g}^{i}(k\omega_{RF}) \\ I_{d}^{i}(k\omega_{RF}) \end{bmatrix}, k = -M,..., M \qquad (4)$$

Once all the extrinsic variables are derived, the high-frequency conditions which guarantee, at the CGP, the same load line measured at ω_{LF} are known. As an example, one can easily calculate the high-frequency load terminations and the device input impedance:

$$Z_L(k\omega_{RF}) = -\frac{V_{ds}^{e}(k\omega_{RF})}{I_{d}^{e}(k\omega_{RF})}, \quad Z_{IN}(k\omega_{RF}) = \frac{V_{gs}^{e}(k\omega_{RF})}{I_{g}^{e}(k\omega_{RF})} \qquad (5)$$

From Equations 1-5 the key feature of this techniques emerges, namely the possibility to transpose the low-frequency data to any microwave frequency and theoretically beyond the frequency limitations of nonlinear microwave instruments (i.e., 67 GHz), starting from the same set of measured low-frequency load lines.

The only requirement is that the models of the capacitive core and parasitic network are sufficiently accurate in the bandwidth of interest. It must be emphasized that since the current and voltage waveforms at the CGP are measured, it is not required to model the complex dispersive phenomena affecting the resistive core [39-43].

In Figure 1.10, an application of the nonlinear-embedding approach for the design of a class AB tuned-load PA in C-band [52] is shown. A 0.5-µm GaN HEMT with a total periphery of 1 mm biased in V_{DQ} = 25 V, I_{DQ} = 100 mA was characterized at 2 MHz to find the optimum load line which was obtained by synthesizing approximately a short circuit at the 2nd and 3rd harmonics (see Table 1.1) at the CGP. Then, the selected load line was transposed at a fundamental frequency of 5.5 GHz, by exploiting the foundry model for the capacitive core and the parasitic network. Figure 1.10 shows the results provided by the nonlinear-embedding procedure in terms of load lines and waveforms, whereas the corresponding source and load impedances are reported in Table 1.1. It is noteworthy that not only the output harmonics were properly tuned, but also the source impedance was harmonically controlled. In fact, the sinusoidal input signal used to search for the low-frequency load line, becomes quite distorted when shifted at the EP at microwaves due to the nonlinearities of the intrinsic capacitances. Therefore, a suitable input harmonic tuning is needed to guarantee a sinusoidal input signal at the input intrinsic plane.

Frequency	Load Impedance @ CGP	Source Impedance	Load Impedance
5.5 GHz	55.6 + j0.0 Ω	2.0 + j8.3 Ω	35.9 + j22.0 Ω
11 GHz	3.8 + j0.3 Ω	0 – j7.7 Ω	2.5 – j7.0
16.5 GHz	3.7 + j0.4 Ω	5.5 – j6.4 Ω	1.7 – j13.1 Ω

Table 1.1 – Predictions of the optimum source and load impedances for the class-AB tuned-load power amplifier.

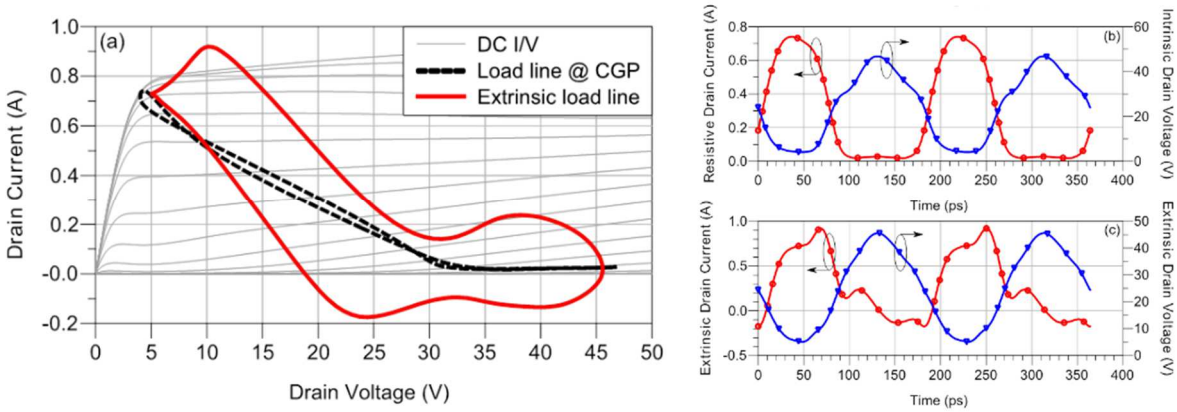


Figure 1.10 – Application of the nonlinear embedding approach for a tuned-load class-AB load line at 5.5 GHz: (a) load lines at the current-generator plane and at the extrinsic plane; waveforms at the current-generator plane (b) and output extrinsic plane (c).

The PA was fabricated by implementing the input and output matching networks to get the predicted impedances at the transistor extrinsic planes. The final circuit is reported in Figure 1.11, whereas a comparison of the predicted and measured performance of the power amplifier is reported in Table 1.2, where the good agreement is evident.

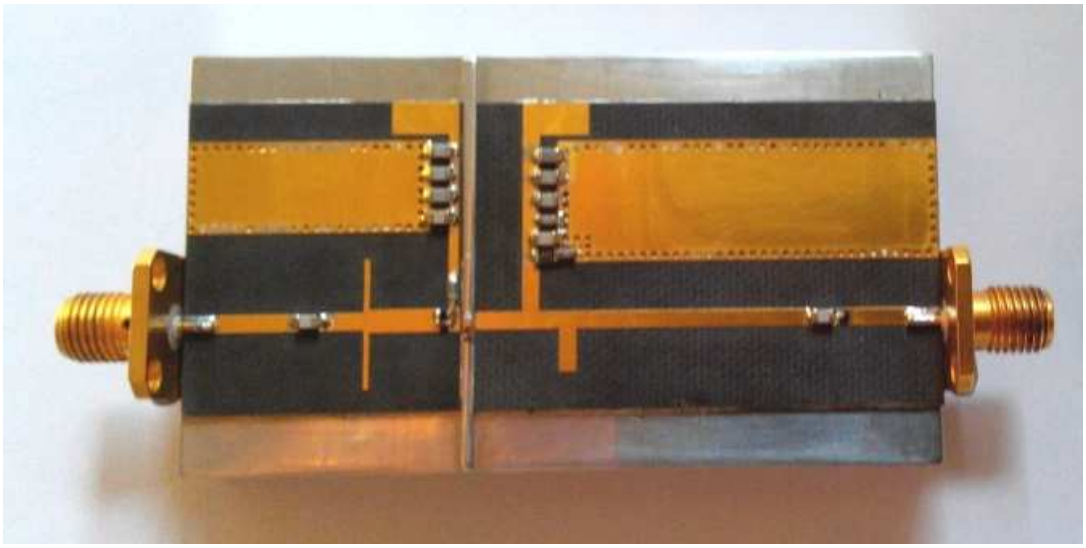


Figure 1.11 – The fabricate C-band class-AB tuned-load PA [52].

Predicted	Quantity	Measured
36.1 dBm	Output Power	36.4 dBm
57.6%	Drain Efficiency	57.6%

Table 1.2 – Comparison between predicted and measured performance of the class-AB tuned-load PA.

The previous example is limited to a single large-signal operating condition, but one can iterate the nonlinear-embedding procedure for different low-frequency load lines. For example, one could keep constant the load terminations at harmonics according to the desired class of operation, and measure the current-generator waveforms by sweeping the power level and the fundamental load impedance. Once the design frequency is selected, the application of the nonlinear embedding to the whole set of measurements, allows one to estimate the equivalent of microwave load-pull contour data, with the great advantage of having imposed the load condition directly at the proper reference plane. In Figure 1.12 [58], an example of class-F load-pull contours is shown, where the harmonic terminations at the CGP were kept constant during the low-frequency measurements, and then the data were transposed at a frequency of 2.4 GHz. In this particular case, the contours are represented for a constant value of the intrinsic voltage V_{GD}, which is an important parameter related to the device reliability. Such a representation is not straightforward at microwave frequencies, also when vector measurements are available, because the intrinsic electrical variables are not directly accessible.

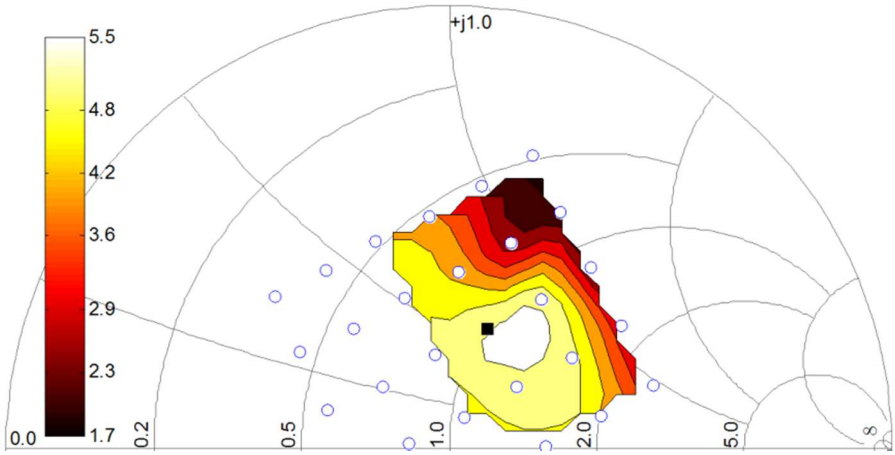


Figure 1.12 – Constant output power class-F load-pull contours at 2.4 GHz for a 0.25-µm GaN HEMT. The contours are represented for a constant level of the intrinsic voltage V_{GD} = -69 V [53].

To conclude, the low-frequency load-pull system allows applying directly the theoretical terminations required for the *waveform engineering* at the transistor current-generator plane and, through the nonlinear embedding, determining the performance of the final amplifier. Active load-pull systems have a complex management of the load at the fundamental frequency and the harmonics. Such a drawback can be solved by using passive load-pull system. The next chapter will describe some circuit solutions to implement a passive load-pull measurement setup equipped with power bias-tee, multiplexer and tuner.

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Chapter 2

Low-Frequency Load-Pull Characterization

2.1. Introduction

The performance evaluation of RF devices varying the termination load can be carried out at the design frequency by means of traditional load-pull systems or the *nonlinear-embedding* procedure described in the previous chapter. The nonlinear-embedding procedure combines information from measurements at high and low frequency to determine the load terminations at the project frequency. This design methodology uses less expensive equipment (available in every microwave laboratory) with respect to microwave load-pull systems. The low-frequency measurements are carried out by means of a low-frequency and large-signal measurement setup, based on the structure of the LSNA and capable to handle higher powers with respect to microwave LSNAs [1]. The measurement setup in Figure 2.1 implements a low-frequency active and passive load-pull system.

The choice of the excitation frequency for the experimental characterization must be low enough to neglect the reactive effects. However, the frequency must be sufficiently high to consider frozen the thermal and trapping phenomena. From practical experience, the excitation frequency of 2 MHz is usually adequate [1].

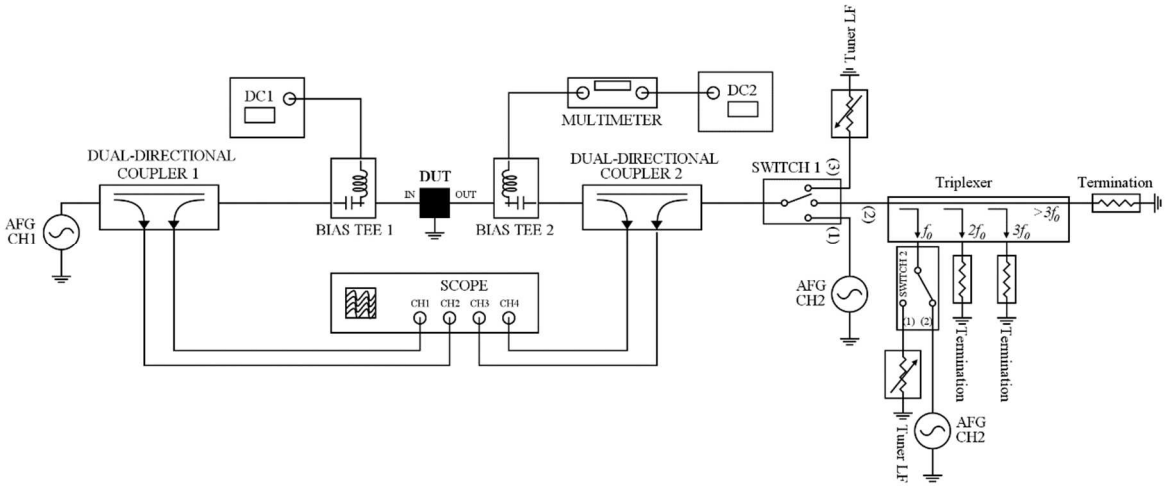


Figure 2.1 – Low-frequency large-signal measurement setup.

By operating at low frequency, it is possible to neglect the device linear and nonlinear dynamic effects and to vary the impedances at the current-generator plane of the DUT. To realize the *waveform engineering* it is necessary to vary the impedances at the fundamental frequency and, usually, at the second and third harmonics through a Low-Frequency (LF) tuner and multiplexer. The optimum real impedance is the one that satisfies the constraint of power, gain or efficiency or a trade-off among these quantities. The resistive and reactive contributions of the bias tees, cables, and couplers are de-embedded from the measures that must refer to the DUT plane. The extrapolation of impedances to the project frequency is described in [1] and has been recalled in Chapter 1.

In this chapter, a passive solution will be introduced to implement a multi-harmonic and LF load-pull system operating at 2 MHz. In particular, a power bias tee and a LF tuner will be dealt with as well as a multiplexer capable of handling the load terminations at the fundamental frequency (f_0), at the second ($2f_0$) and third ($3f_0$) harmonic, that are necessary to implement the amplifier classes as F, J or tuned load configuration. The tuner and the multiplexer are designed to operate at the fundamental frequency of 2 MHz. By appropriately replacing the capacitors and the inductors it is possible to extend the tuner frequency range[1].

Finally, we want to highlight that the LF passive system allows greater speed of synthesis of the impedance compared to the LF active version, whose research algorithm depends on the characteristics of the DUT to be characterized (e.g. saturation power or bias). However, the active solution has the advantage of being able to synthesize any impedance of the Smith chart. In fact, the synthesized impedance is not related to the resistances/reactances of the path between the DUT drain and RF source (see Fig. 1.9), that determine, in the passive version, the reduction of the area of impedances which can be synthesized.

2.2. Low-frequency Load-Pull Measurement Setup

The block diagram of the Large-Signal and Low-Frequency (LSLF) measurement setup is shown in Figure 2.1 and implements a LF load-pull system that allows the active and

[1] The impedance associated with the resistors has negligible reactance compared to the resistive part up to 30 MHz, then the value of 30 MHz represents the maximum frequency of our tuner. Currently, the introduced reactances allow one to compensate only the cables, coupler and bias tee, but nothing forbids to compensate the resistor reactances and exceed the frequency of 30 MHz.

passive synthesis of termination loads. The measurement system consists of an arbitrary two-channel generator, where the first channel allows exciting the input of the DUT, while the second one applies the incident waveform at the output of the DUT to handle the active synthesis of the load [2]. If the switch 1 is set on position "1" the termination load is actively synthesized. The load impedance can be seen as the combination of the incident and reflected power waves at the transistor output port. In the absence of a physical load (tuner), a function generator can be used to generate the reflected wave with arbitrary amplitude and phase with respect to the excitation wave at the input of the DUT.

If the switch 1 in Figure 2.1 is set to position "2" and switch 2 is set to position "1", the loads at the fundamental frequency (f_0) and the harmonics ($2f_0$, $3f_0$) are handled through the low-frequency multiplexer and tuner. In this way, it is possible to implement the *waveform engineering*, e.g., to apply a short circuit to the second and third harmonics to generate a tuned-load configuration or a short circuit to the second harmonic and an open circuit to the third harmonic for class-F operation. Another possibility allowed by the measurement setup in Figure 2.1 is to set the impedance value at the fundamental frequency in the active manner by means of the switch 2 set to position "2", that guarantees a greater flexibility for the synthesis of the load termination.

Finally, if the switch 1 is set to position "3", the load condition is imposed through the tuner at the fundamental frequency only, useful for managing the load termination for the conduction-angle amplifiers (i.e., A, AB, B or C). In this case, the tuner applies the same termination at the fundamental frequency and at the harmonics.

In Figure 2.1, two bias tees separate the DC and RF paths, while two dual-directional couplers with bandwidth [100 kHz – 400 MHz] and the oscilloscope with analog bandwidth of 4 GHz, acquire incident and reflected waveforms at the DUT. The bias tee at the input is a wide-band commercial bias tee with bandwidth [100 kHz – 12 GHz], while at the output there is an in-house fabricated bias tee, able to handle high currents and voltages, with bandwidth [45 kHz, 725 MHz].

The input bias system (DC1 in Figure 2.1, HP4155 – semiconductor analyzer) ensures the high resolution (4 μV; 20 fA), with adequate accuracy (V: 0.05%, I: 0.2%) required for the measurement of the dc electrical quantities at the input port of the DUT. The output-bias system (DC2 in Fig. 2.1) consists of a power supply with high current and voltage capabilities (TTi – QPX600DP, with voltage range 0 - 160 V and maximum power equal to 1200 W) and of a programmable 6.5 digit multimeter (Keithley 2000) for accurate current

measurements. The measuring instruments are controlled through a NI LabView interface that manages the de-embedding of the acquired waveforms, transposing the gathered waveforms from the oscilloscope plane to the DUT plane, i.e., eliminating the contributions of the bias tees, cables and couplers.

Figure 2.2 shows the screenshot of the controlling software. The front panel presents 4 tabs: *Instrument Settings*, *File Settings*, *Measurement Settings* and *Run-Time Indicators & Plots*. In the tab "Instrument Settings" the characteristics of the DC source, arbitrary function generator (AFG), multimeter and LF tuner are defined, while "File Settings" defines the paths of the de-embedded files and configuration file of the LF tuner. In the tab "Measurement Settings" are defined the voltage amplitudes to apply at the input and output of the DUT (active system) or the voltage amplitudes and the impedances (LF tuner) to apply at the input and output of the DUT (passive system). In the tab "Run-Time Indicators & Plot" the run-time performance of the device at its reference plane are shown.

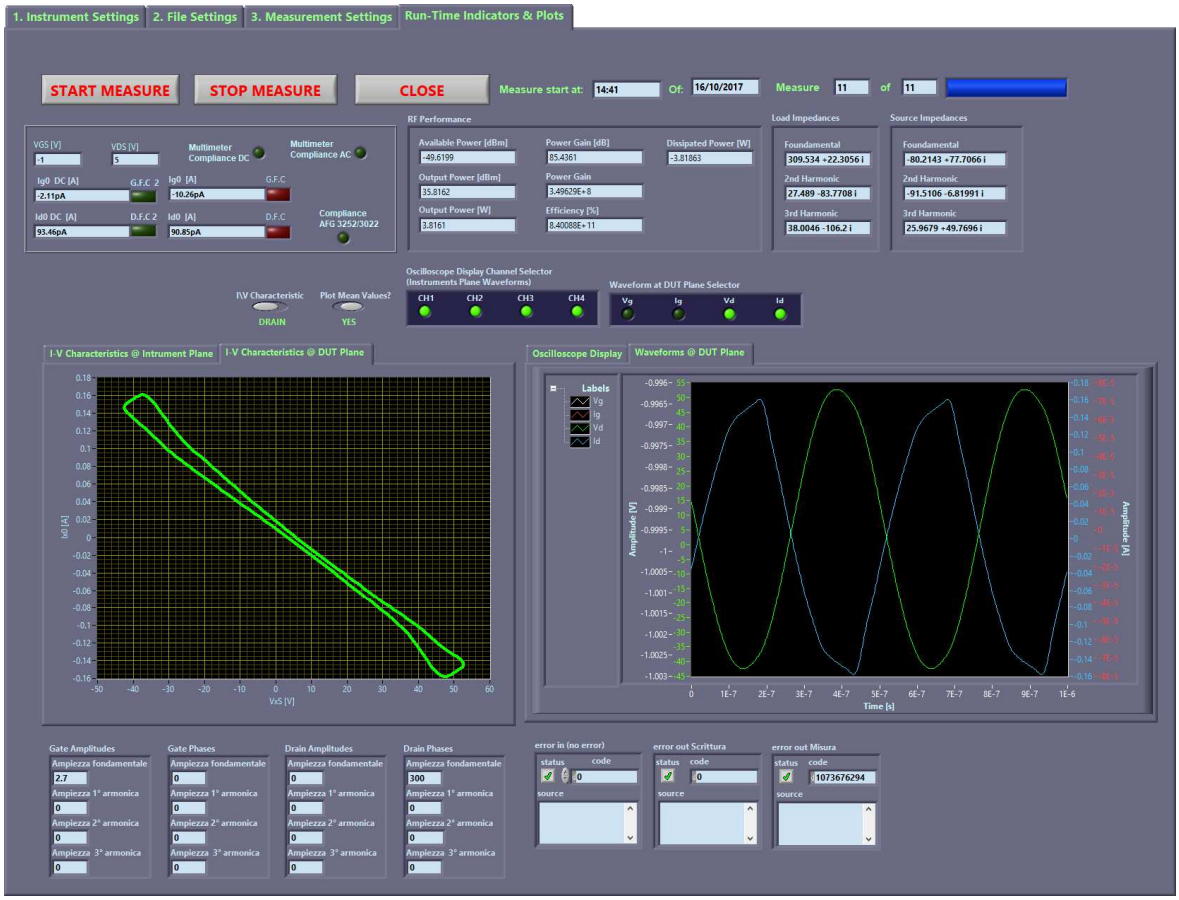


Figure 2.2 – Front panel of the controlling software for the load-pull measurement setup.

2.3. Power Bias Tee

The bias tee is a three-port circuit used to set the bias point of the transistor. It is a passive component with three ports normally called DC, RF and RF+DC. This component is capable of combining signals from DC and RF ports and ensures a good isolation between them. The typical characteristic parameters of a bias tee are insertion loss, isolation and Voltage Standing Wave Ratio (VSWR). The insertion loss represents the attenuation introduced by the bias tee between the RF and RF+DC branches. The isolation is the ability of the bias tee to prevent the interaction between the RF and DC branches, while the VSWR is a scalar measure of the proximity between the impedance seen from the RF branch and the system characteristic impedance (for a microwave system it is 50 Ω).

Maximum DC Voltage	> 100 V
Maximum DC Current	> 3 A
Bandwidth @ -1 dB	100 kHz to 500 MHz
Insertion Loss	< 1 dB
Characteristic Impedance	50 Ω

Table 2.1 – Goal to achieve for the bias tee.

Operating at LF, it is not required to handle large bandwidths, while high voltages and currents are important. Some examples are shown in papers [2, 11]. To avoid oscillations of the DUT it is necessary to use a broadband bias tee at the input of the DUT. In this context, the characteristics of the bias tee to be designed have been identified in Table 2.1.

The PCB (Printed Circuit Board) support is FR-4, that is a composite material made of woven fiberglass cloth with an epoxy resin. The characteristics of the support used to make the PCB are shown in Table 2.2.

Thickness of Copper	18 µm
Substrate Height	1.5 mm
Relative Dielectric Constant	4.35 – 4.8 [12]

Table 2.2 – Characteristics of the PCB support.

To ensure the characteristic impedance of 50 Ω, the traces must have a width of about 3 mm [13], this width allows a maximum current of 5 A (for over-temperature of the trace of 10 °C) [14,15].

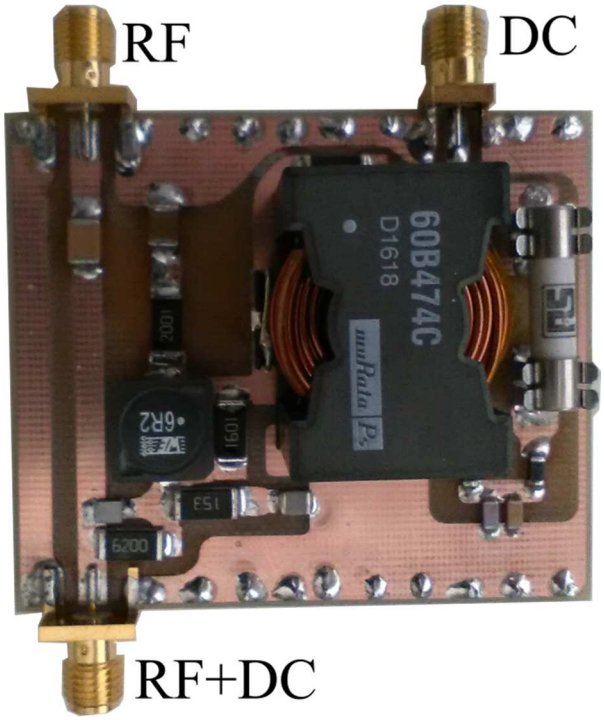


Figure 2.3 – Photo of the realized bias tee (size 5 x 6 cm).

Figure 2.3 shows the photo of the realized bias tee, which is capable of handling a maximum voltage V_{MAX}^{DC} of 500 V and a maximum current I_{MAX}^{DC} of 3.4 A. The electrical schematic is shown in Figure 2.4.

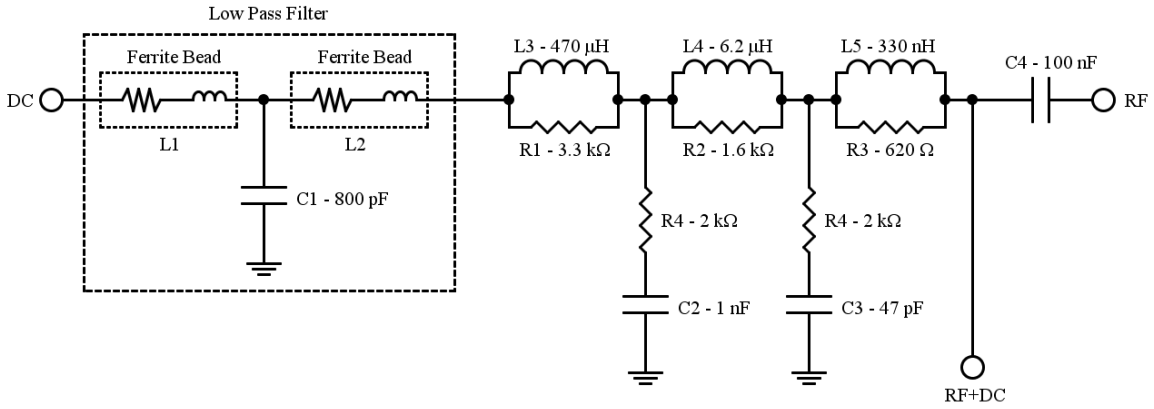


Figure 2.4 – Schematic of the realized bias tee.

The three inductors in the DC branch allow a good insolation greater than 20 dB above 200 kHz as shown in Figure 2.5b and measured with the VNA Agilent E5061E. The bandwidth or Insertion Loss parameter is shown in Figure 2.5a. The bandwidth defined at -1 dB is [45 kHz, 725 MHz], while the typical insertion loss is -0.3 dB. Figure 2.5c shows the VSWR, that is typically < 1.8. The self-resonance frequencies of the inductors in the DC branch reduce the bandwidth of the bias tee. Indeed, the capacitor self-resonance

frequency of the decoupling capacitor in the RF branch is higher than the inductors self-resonance and does not reduce the performance of the bias tee. Figure 2.6 shows the impedance magnitude of the capacitor C4 in Figure 2.4, measured with the Agilent E5061E VNA in the band [50 MHz, 2500 MHz]. Table 2.3 shows some salient characteristics of the used components.

Component	Value		Self-Resonance	I_{MAX}^{DC}	V_{MAX}^{DC}
L1,L2	Ferrite-Bead Model: BLM31PG330SN1L Murata		1 GHz[2]	7 A[2]	-
L3	470 µH		2.1 MHz[2]	3.5 A[2]	-
L4	6.2 µH		43 MHz[2]	5.5 A[2]	-
L5	330 nH		180 MHz[2]	3.4 A[2]	-
C1	800 pF	470 pF	Not critical	-	1 kV[2]
		330 pF			500 V[2]
C2	1 nF		Not critical	-	3 kV[2]
C3	47 pF		Not critical	-	1 kV[2]
C4	100 nF		2.2 GHz[3]	-	630 V[2]

Table 2.3 – Characteristics of the bias tee components.

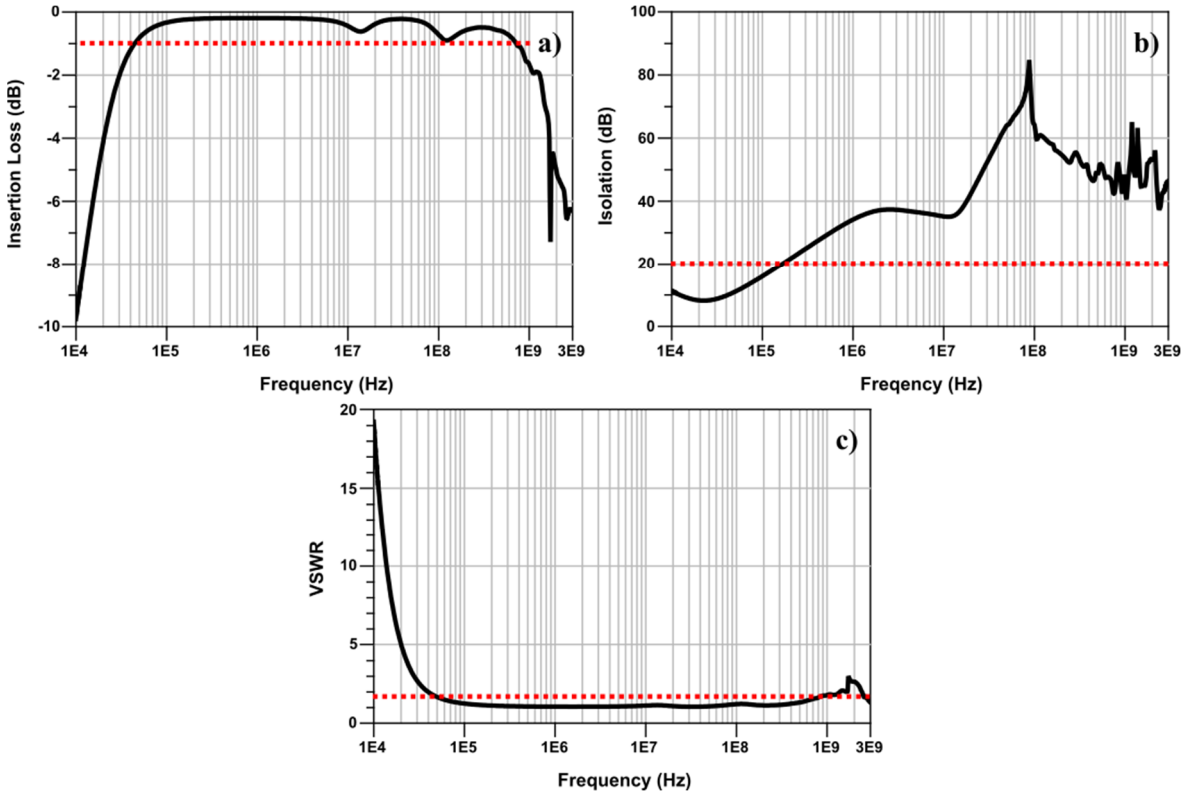


Figure 2.5 – Insertion loss (a), isolation (b) and VSWR parameters measured between 10 kHz to 3 GHz with the Agilent E5061E VNA.

[2] From datasheet.
[3] Measured with the Agilent E5061E VNA.

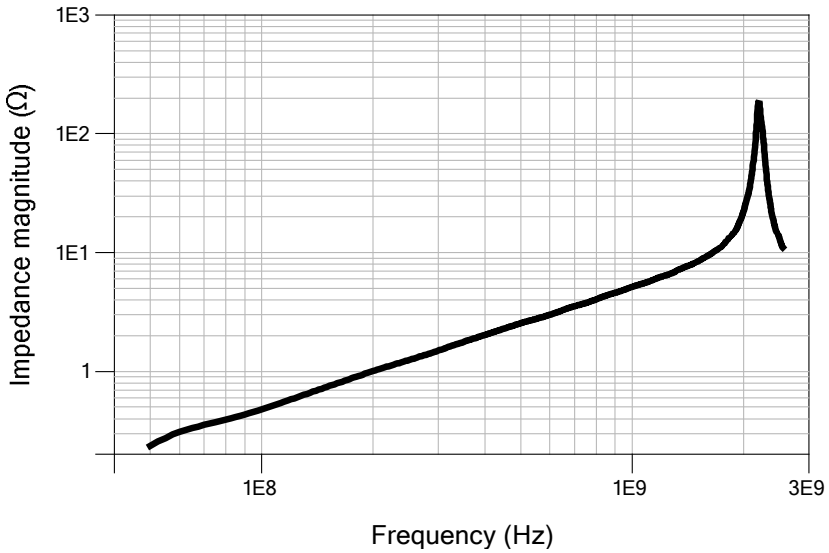


Figure 2.6 – Impedance magnitude of the capacitor C4 (100 nF) measured from 50 MHz to 2.5 GHz with the Agilent E5061E VNA.

The low pass filter highlighted in Figure 2.4 uses ferrite-beads to improve the insulation at high-frequency, while the resistors R1, R2, R3 and the elements R4-C2 and R5-C3 equalize the insertion loss parameter.

Finally, it is possible to estimate the maximum RF power based on the capacitor characteristics and the physical size of the microstrips. The maximum voltage V_{MAX}^{rms} at the RF+DC port in Figure 2.4 can be derived from the maximum DC voltage V_{MAX}^{DC} of the capacitor C4, i.e., in sinusoidal regime:

$$V_{MAX}^{rms} = \frac{V_{MAX}^{DC}}{\sqrt{2}} = 440\ V_{rms} \qquad (1)$$

The datasheet of C4 (C4532 Series – TDK) does not report the estimated maximum power dissipated for the package 1812, but it can be estimated from the datasheet of a 1812 resistor and it is about 3 W[4]. In the bandwidth between 50 MHz and 725 MHz the Equivalent Series Resistance (ESR) is <0.1 Ω as shown in Figure 2.7, then the estimated maximum AC current through the capacitor is about 5.5 A_{rms}.

[4] This value is also similar for multi-layers ceramic capacitors of American Technical Ceramics, but with different maximum voltage values and similar physical size.

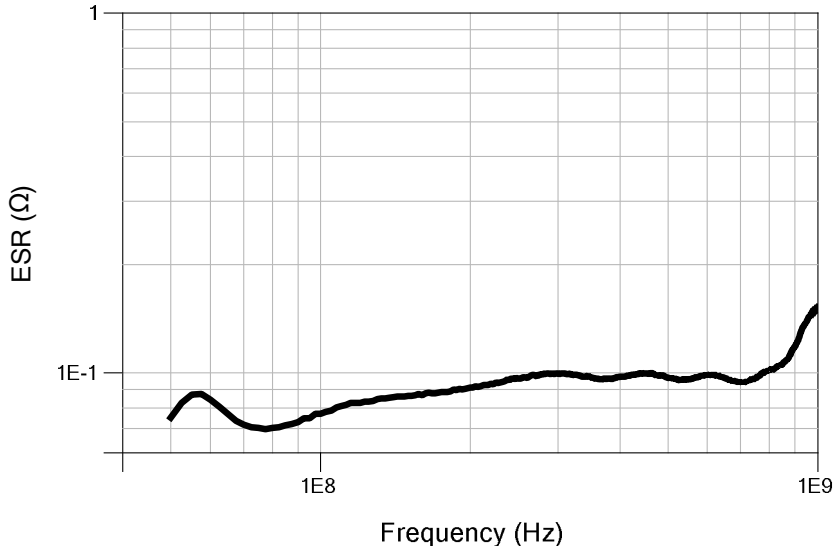


Figure 2.7 – ESR of the capacitor C4 (100 nF) measured from 50 MHz to 1 GHz with the Agilent E5061E VNA.

The maximum AC current I_{MAX}^{AC} on the microstrip from the connector RF to the connector RF+DC is a function of the skin effect. In the worst case, the thickness of the trace for skin effect at the frequency of 725 MHz (upper frequency of bias tee) is:

$$\delta = \sqrt{\frac{2\rho}{\omega\mu_0\mu_r}} \approx 2.4\ \mu m\ at\ 725\ MHz \qquad (2)$$

where ρ is the resistivity of the conductor (copper 1.678 10^{-8} Ωm), ω is the angular frequency, μ_r is the relative magnetic permeability (≈1) and μ_0 the free space permeability [3].

Considering the skin effect, the trace from the connector RF to the connector RF+DC can carry up to 0.7 A_{rms} at 725 MHz, for these reasons and taking into account Equation (1), the power bias tee can handle about 55 dBm (308 W) of RF power at 725 MHz.

To summarize, Table 2.4 shows a synthesis of the characteristics of the designed bias tee.

Maximum RF Power	55 dBm (308 W)
Maximum Voltage at DC Port	500 V
Maximum DC Current	3.4 A
DC resistance from DC to RF+DC Port	0.2 Ω
Bandwidth a -1 dB	45 KHz – 725 MHz
Typical insertion Loss	-0.3 dB
Typical VSWR at RF Port	< 1.8
Size (without connectors)	(50 x 60 x 22) mm

Table 2.4 – Characteristics of realized bias tee.

2.4. Low-Frequency Tuner at 2 MHz

2.4.1. Introduction

The LF tuner described in this section was specifically designed for the measurement setup at LF. It is built using concentrated components, i.e., inductors, resistors and capacitors. The use of miscrostrips and stubs (typical of the microwave version) is discarded due to the excessive wavelength involved under LF operation, i.e., about 150 m (in vacuum) at 2 MHz. The tuner proposed was designed to operate at the frequency of 2 MHz with a minimum dissipated power greater than 15 W.

In LF characterization, the optimal load at the current-generator plane must be resistive and, for suitable device peripheries, the resistance that maximizes the output power lies in the range [30, 300] Ω. From these considerations, the LF tuner specifications are defined in Table 2.5.

Working frequency	2 MHz
Minimum dissipated power	> 15 W
Minimum range of load resistance values	30 Ω to 300 Ω

Table 2.5 – LF tuner characteristics.

Operating at LF, the reactive contributions of the DUT are negligible, but they are not the only ones. Reactive contributions introduced by cables and bias tees (see Figure 2.1) need to be properly compensated through the insertion of series capacitance or inductances, in order to provide a resistive load at the DUT output port. These parasitic quantities have been estimated through the simulation of cables and bias tee, where the cables are represented by transmission lines, while the bias tee is represented through a LC network [3]. The whole network is depicted in Figure 2.8, where C' and L' represent the capacitance and inductance for unit length and Δz is the length of the network segment [3]. From a preliminary analysis of commercial cables (i.e., LMR-195, LMR-200, LMR-400, LMR-500, RG58) and bias tee (i.e., PSPL5544, PSPL5547, PSPL5575A), we have obtained the following mean values: C' = 81.9 pF/m, L'=0.21 μH/m, L between 0.1 mH to 1.5 mH and C between 20 nF to 440 nF. To a first approximation, the reactive contribution of the dual-directional coupler has been neglected.

Figure 2.9 represents the conjugate reflection parameter simulated at the "DUT" port of the connection path in Figure 2.8 at the frequency of 2 MHz by varying the length of the cable (Δz) between 0.3 m to 0.8 m (values of actual lengths of cables available in our laboratory) and varying the resistive impedance at the "tuner" port between 1 Ω to 799 Ω

(maximum resistor value in DC regime). The shaded area on the Smith chart is the area that the tuner must cover, and highlights the reactances that the tuner must be able to synthesize for "compensating" the connection path contributions. In order to have a rough estimation of the reactances to be compensated by the tuner, we approximated the circuit formed by the connection path and the tuner as series impedances. In particular, a set of five capacitors "C_T" (14 nF,1 nF, 1 nF, 2 nF, 9 nF) and nine inductors "L_T" (200 nH, 200 nH, 300 nH, 500 nH, 1 µH, 1.8 µH, 5 µH, 8 µH, 12 µH) have been determined to cover the highlighted area.

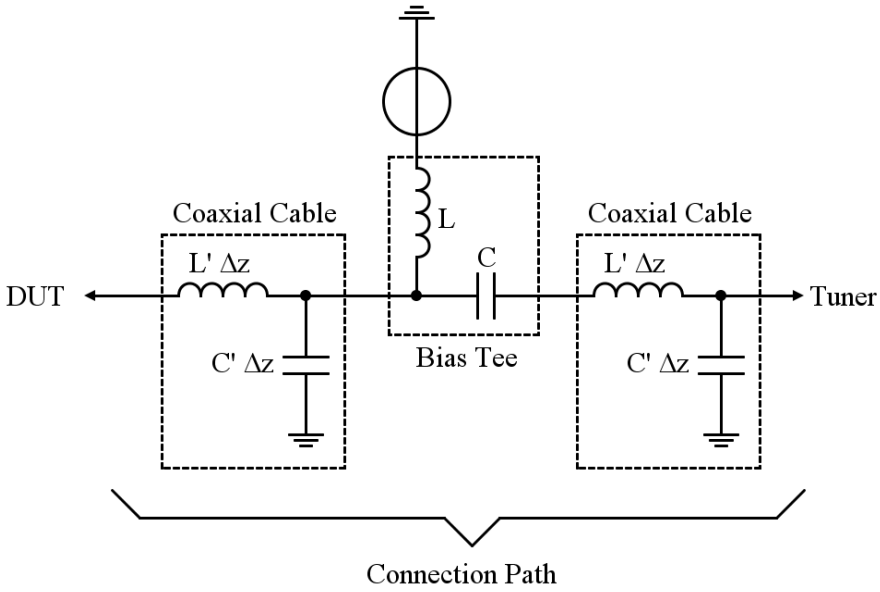


Figure 2.8 – Network adopted to describe the reactance introduced by the path between the DUT and the tuner.

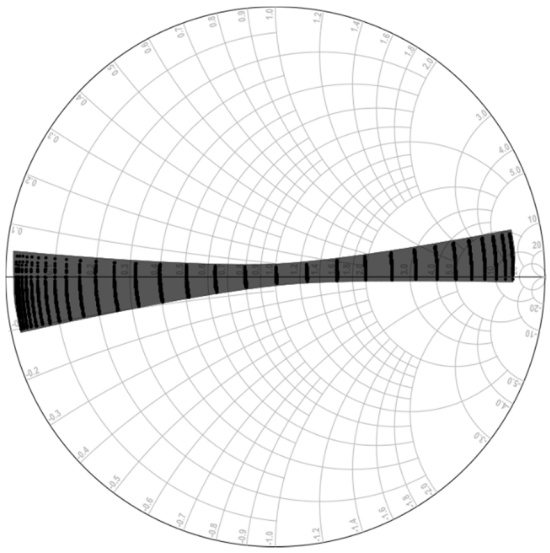


Figure 2.9 – Simulation of the conjugate reflection parameter of the connection path in Figure 2.8 at 2 MHz by varying the length of the coaxial cable (Δz) and the tuner resistance.

The tuner coverage area, obtained by using this set of inductors and capacitors (C_T, L_T), is depicted in Figure 2.10 at 2 MHz (highlighted in red).

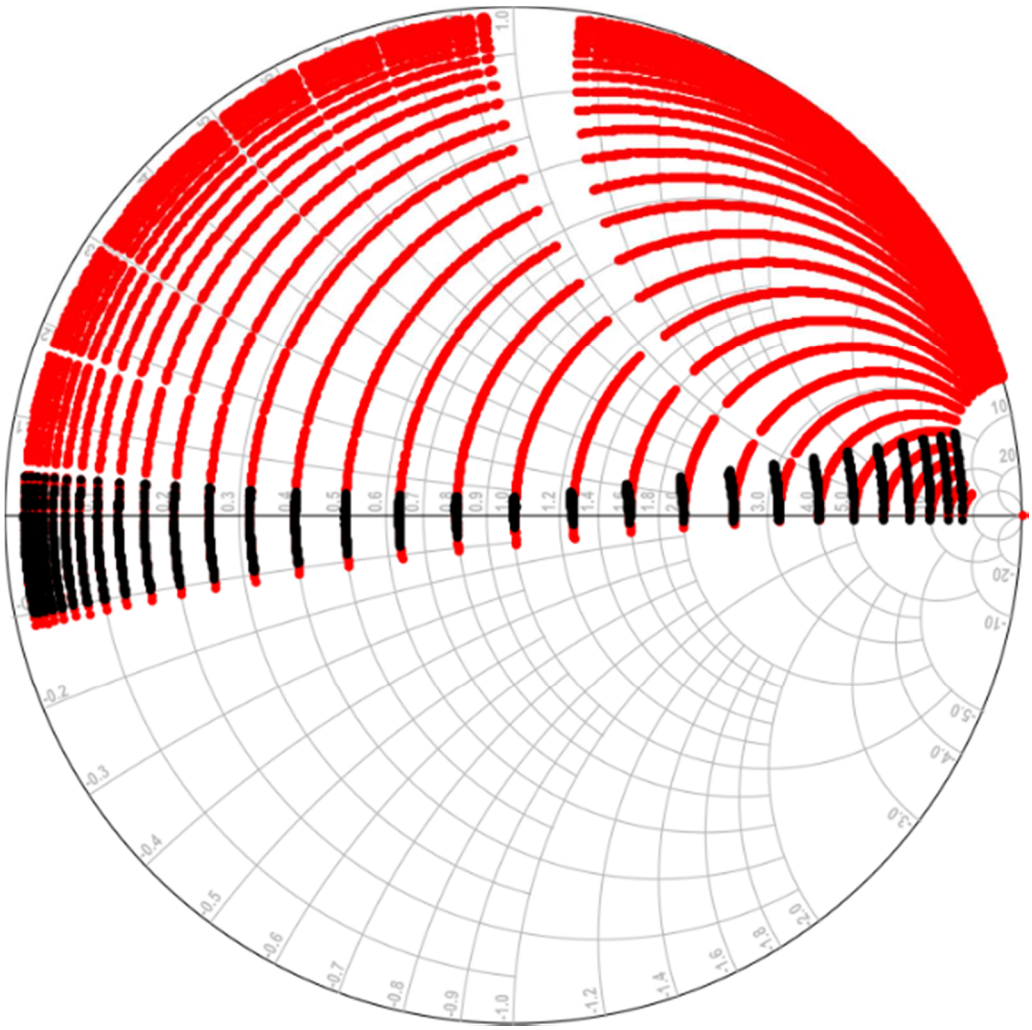


Figure 2.10 – Representation of the tuner ideal coverage area at the frequency of 2 MHz (red) superimposed on figure 2.9.

Finally, Figure 2.10b shows the simulation of the reflection coefficient at the DUT plane varying the connection path characteristics (L, C, Δz), the resistance values R_T and the discrete reactive elements (C_T, L_T) of the tuner (see inset in Fig. 2.10b). For this simulation we chose to compute only a subset of the impedances that can be generated by the tuner. From Figure 2.10b we note that the tuner is capable of synthesizing real impedances at the DUT plane in the range [1 Ω - 799 Ω] (intersection of the loci with the real axis), even when varying the characteristics of the connection path.

In Figure 2.10b, for a given value of the resistance R_T, each different connection path (obtained by varying L, C, Δz) is represented by a point Z_{path} which, by modifying L_T and C_T, is moved clockwise or counterclockwise to intersect the real axis, i.e., the real impedance to apply to the DUT (see Figure 2.10c).

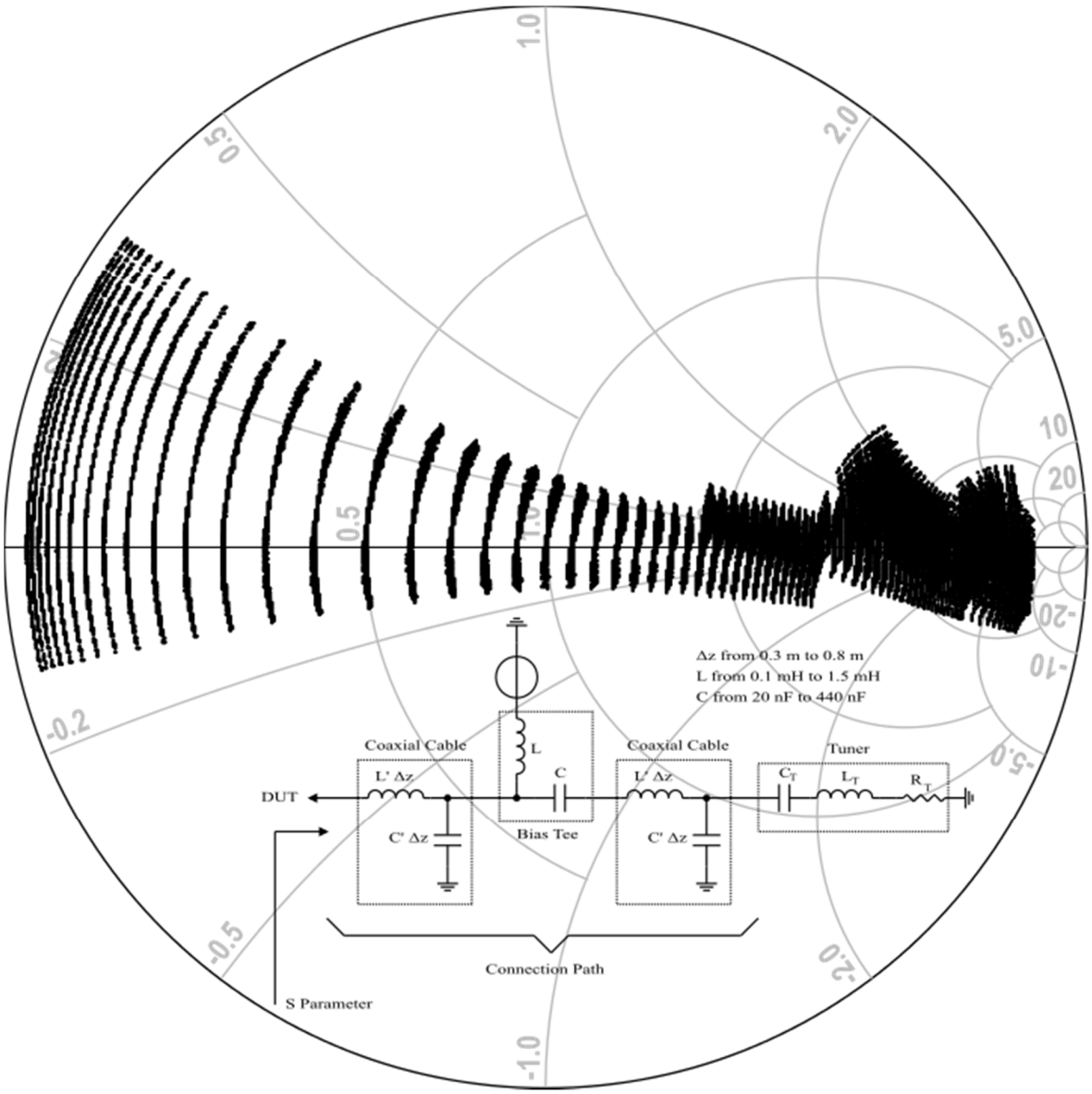


Figure 2.10b – Reflection coefficient at the DUT plane varying the connection path characteristics (L, C, Δz) and some discrete elements (R_T, C_T, L_T) of the tuner. The schematic represents the simulated circuit.

To give a clearer view of the tuner capability, results related to a given connection path will be analyzed in the following. In particular, one of the connection paths of the setup in our laboratory has the following characteristics: $\Delta z = 0.5$ m, $C = 100$ nF and $L = 470$ μH (see Paragraph 2.3). In Figure 2.10d we show the simulation of the reflection coefficient at the DUT plane by varying the tuner parameters (R_T, C_T, L_T) with the characteristics of the connection path just described. From this figure, we observe that for each resistance R_T does exist a value of C_T and L_T that allows seeing at the DUT plane a real impedance (intersection of the loci with the real axis). In Figure 2.10d a wider range of impedances generated by the tuner has been used with respect to the case in Figure 2.10b.

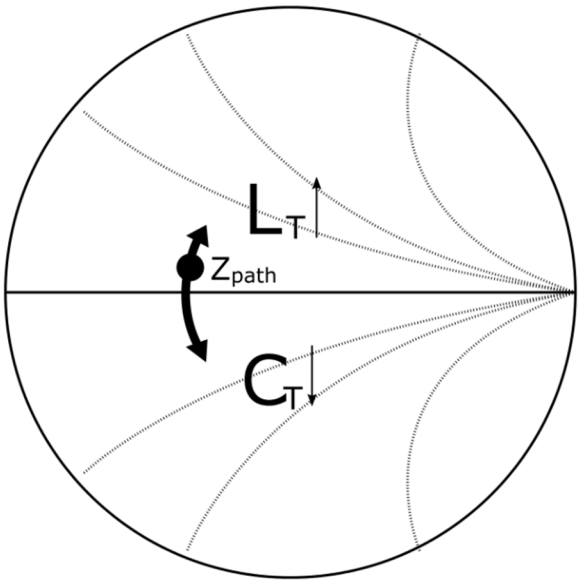


Figure 2.10c – Shifting of the impedance by reducing the tuner's capacitance (C_T) or increasing the tuner's inductance (L_T).

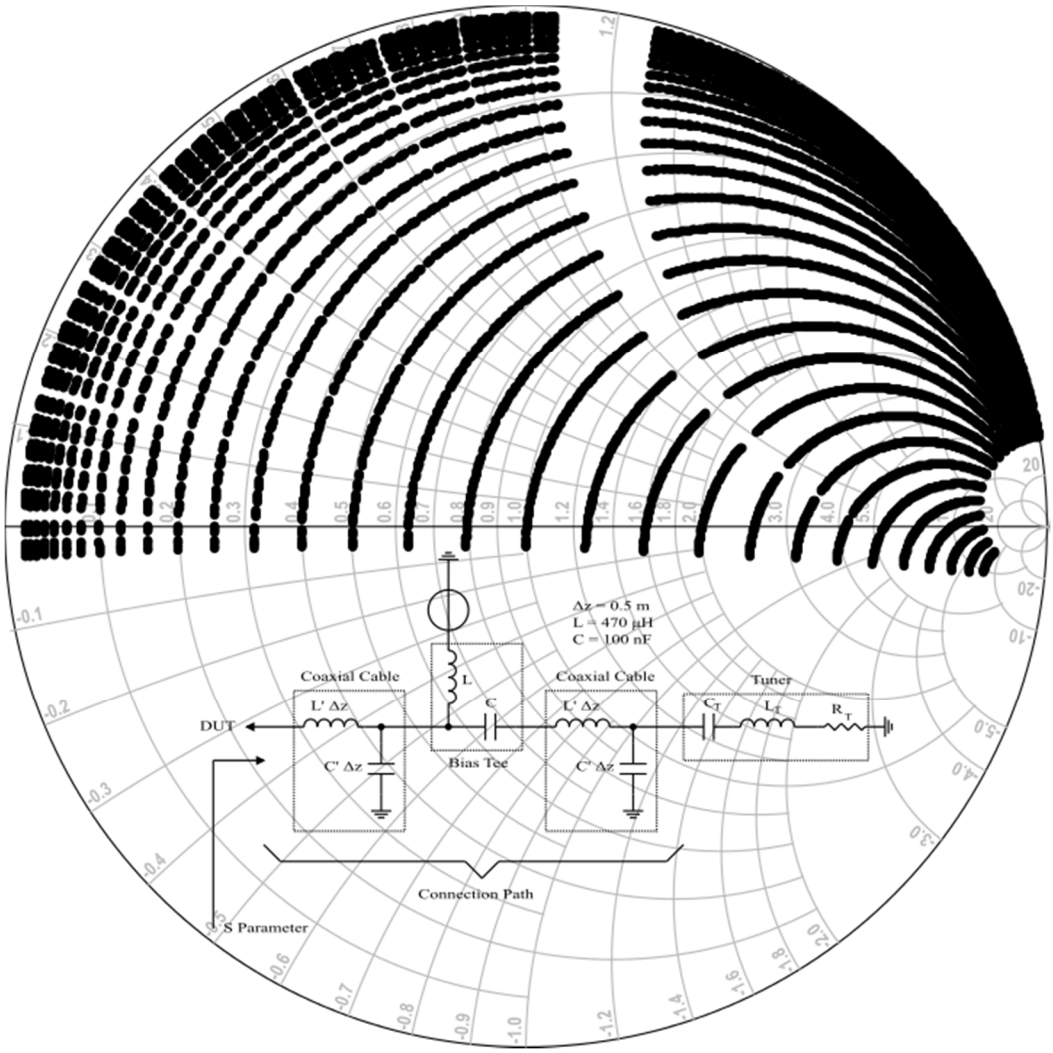


Figure 2.10d – Reflection coefficient at the DUT plane with constant Δz=0.5 m, L=470 µH, C = 100 nF and varying the elements of the tuner, i.e., R_T range [1 Ω – 799 Ω], C_T range [14 nF – 27 nF] and L_T range [200 nH - 29 µH]. The schematic represents the simulated circuit.

The circuit diagram of the tuner is depicted in Figure 2.11. The system is formed of 11 power resistors on thick film technology, with low Equivalent Series Inductance (ESL - ≤ 0.1 μH) and case TO-220, which allows good heat dissipation. The polyester capacitors withstand a maximum voltage of at least 250 Vac, while the inductors are built on air or on ferromagnetic support. The air inductors L1, L2, L3, L4, L5, L6 are realized with enameled wire with diameter of 1 mm and with number of turns calculated by the Nagaoka's formula (see next Section), while L7, L8, L9 are made on a ferrite toroidal core (Fair Rite, material 61) with enameled wire of diameter 1 mm.

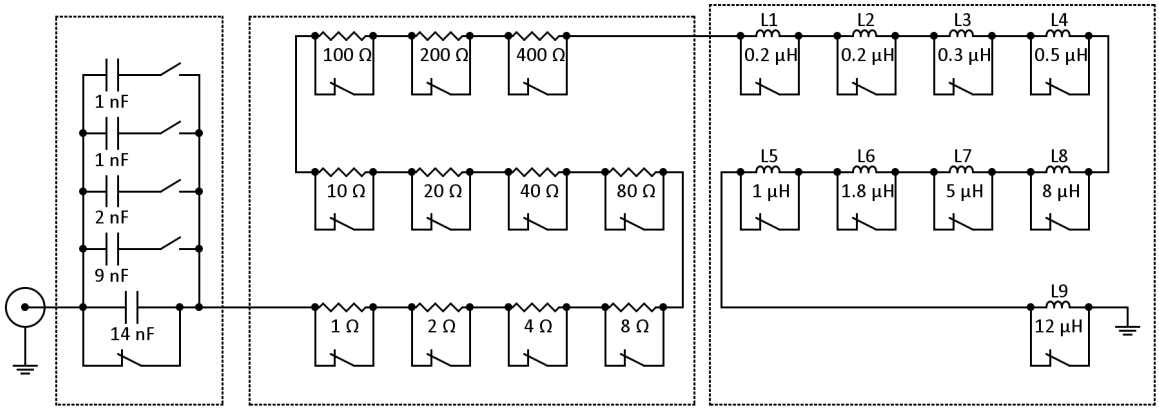


Figure 2.11 – Electrical schematic of low-frequency tuner.

The switches in Figure 2.11 insert the reactive and resistive elements of the tuner. The resistor structure allows for varying the resistance from 1 Ω to 799 Ω, with resolution of 1 Ω. To increase the power specification of the tuner, the resistors could be mounted on a heat sink. For example, a maximum dissipated power of 50 W can be achieved by using a heat sink with a thermal resistance of 1.1 K/W.

In the realized tuner, the switches are implemented through relays controlled by a microprocessor system. The ohmic-reactive load is configurable through three text commands that are sent to the tuner via a USB interface. Control drivers have been developed and implemented in NI LabVIEW to enhance the interfacing with the automatic measurement setup. For searching the impedances, a LabView program has been implemented, whose front panel is shown in Figure 2.12. The research of the impedance is done using the measurement setup shown in Figure 2.1, with the switch on position "3" and in absence of the DUT, with a direct connection of the gate and drain paths. The software generates a file that contains the configurations of resistors, inductors and capacitors needed to synthesize the impedances to be applied at the DUT. The automated software imposes the resistance of the impedance by means of the physical resistors and inserts suitable capacitors and/or inductors to compensate for the parasitic imaginary part.

The choice of the inductors to insert is managed by an algorithm based on the *bisection method* while, for the capacitors, all the permutations are tested (4 capacitors, $2^4 = 16$ permutations). The number of the permutations for the inductors is too high ($2^9 = 512$ permutations) and the bisection method allows a faster search, i.e., the software, once the resistors have been set, measures the impedances without inductors, in the presence of all the inductors (29 µH) and in an intermediate case (12 µH). Based on these measurements, the algorithm determines the range of values needed to compensate the residual imaginary part of the path, obtaining at each iteration a better estimate of the inductance to be applied. The search ends if the synthesized impedance falls within the range of *allowed values* defined as the area of a square with side twice the "deviation" (input control highlighted in Figure 2.12) or when the maximum number of iterations is reached. The "deviation" is the tolerance on the searched impedance, represented as an S parameter. In this last case, the program saves the impedance configuration nearest to the target impedance. Figure 2.13 shows the flowchart of the search algorithm.

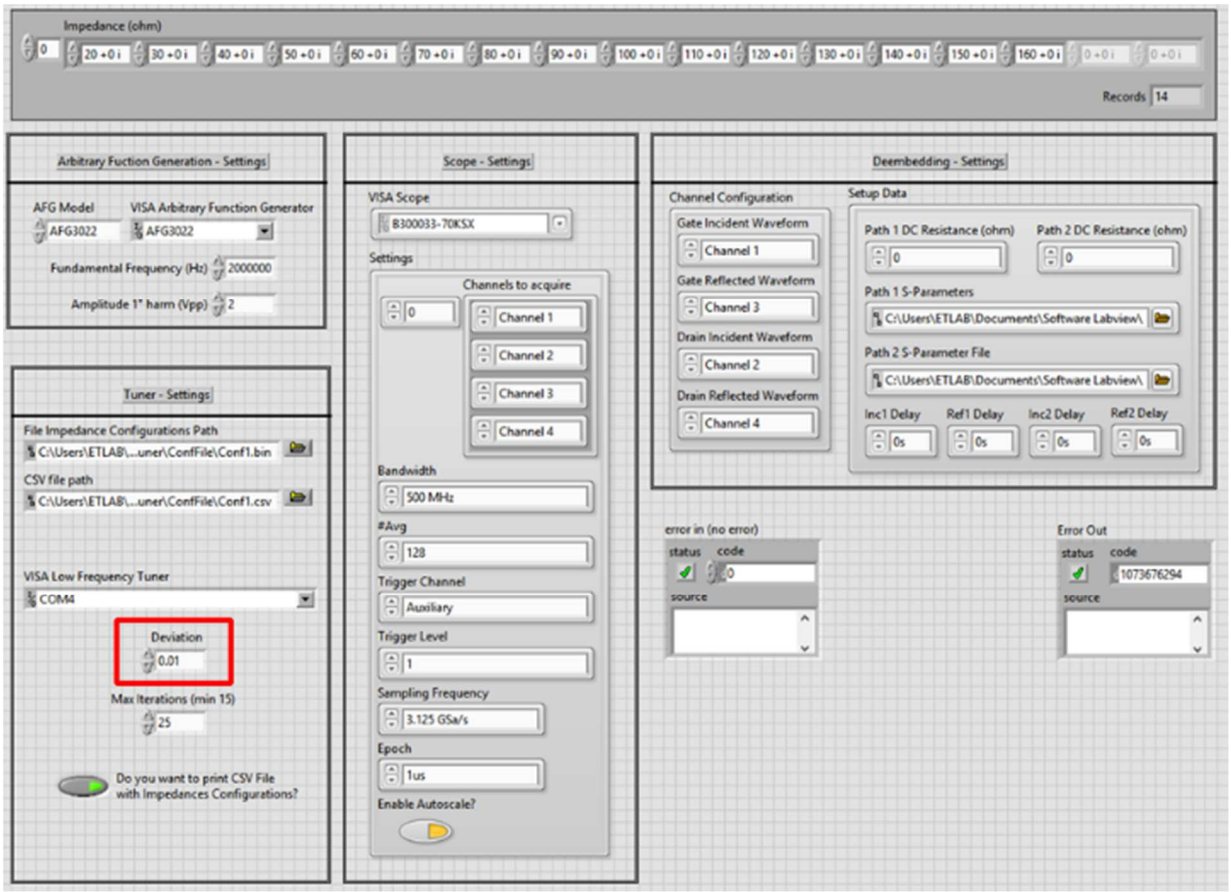


Figure 2.12 – Front panel of the software for automatic search of impedances.

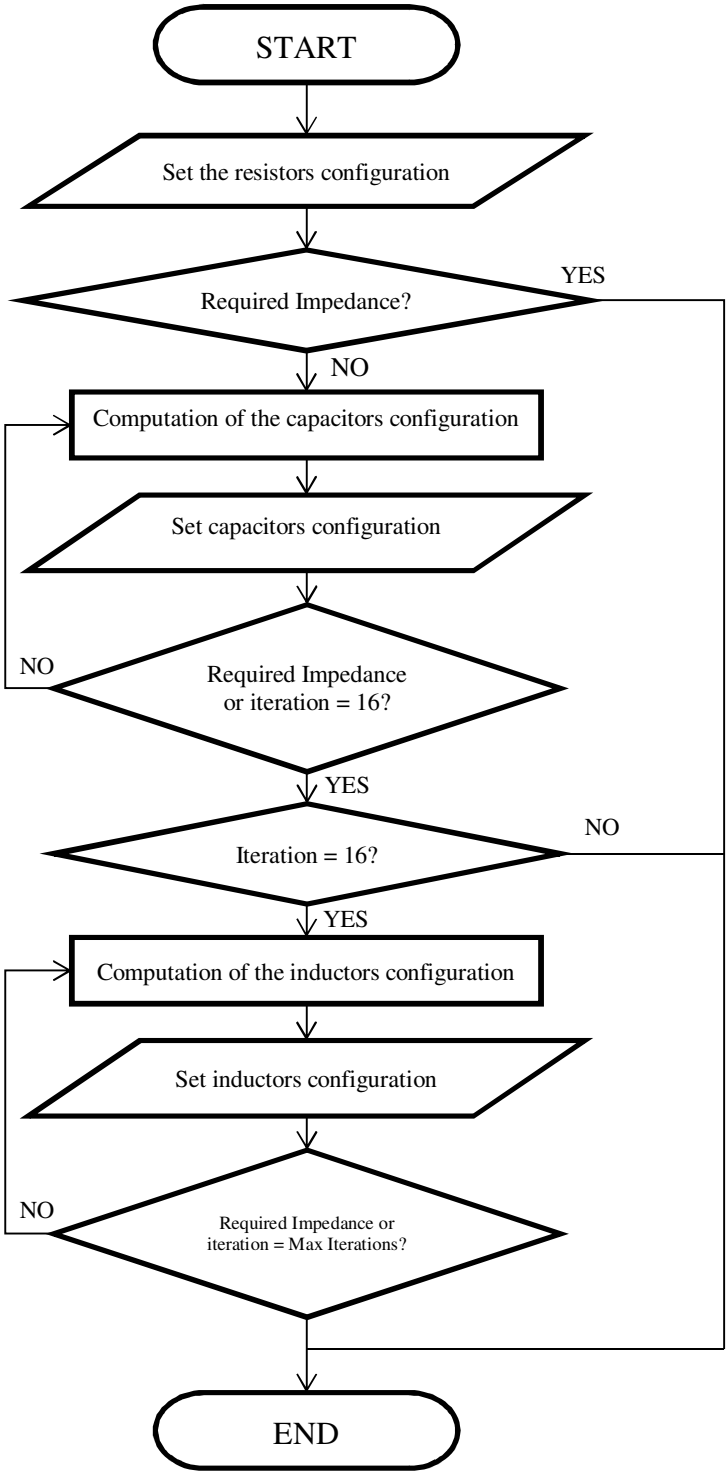


Figure 2.13 – Flowchart of the algorithm for the automatic search of a required impedance.

2.4.2. Air Inductors

The exact formula for calculating the turns of a single-layer solenoid on air was written by Lorentz and then Wheeler, but the Wheeler's formula is too complicated for practical use. The formula used to calculate the coil turn number *N* is:

$$N = \sqrt{\frac{Lb}{\mu_0 \pi a^2 f\left(\frac{2a}{b}\right)}} \qquad (3)$$

where a is the radius of the coil, b the axial length, μ_0 the permeability of vacuum, L the coil inductance and $f\left(\frac{2a}{b}\right)$ is a suitable value tabulated by Nagaoka [4] that is a function of the shape ratio $\left(\frac{2a}{b}\right)$ [5]. Table 2.6 reports the number of turns and the inner diameter of the inductors.

	Inductance	Inner diameter (mm)	Length (mm)	Turns
L1	200 nH	6	8	7
L3	300 nH	6	11	10
L4	500 nH	6	16	15
L5	1 µH	16	9	8
L6	1.8 µH	16	13	12

Table 2.6 – Table of characteristics of air coils.

2.4.3. Inductor on Ferromagnetic Core

The ferromagnetic core inductor is an inductor that uses a magnetic core on ferrite or iron.

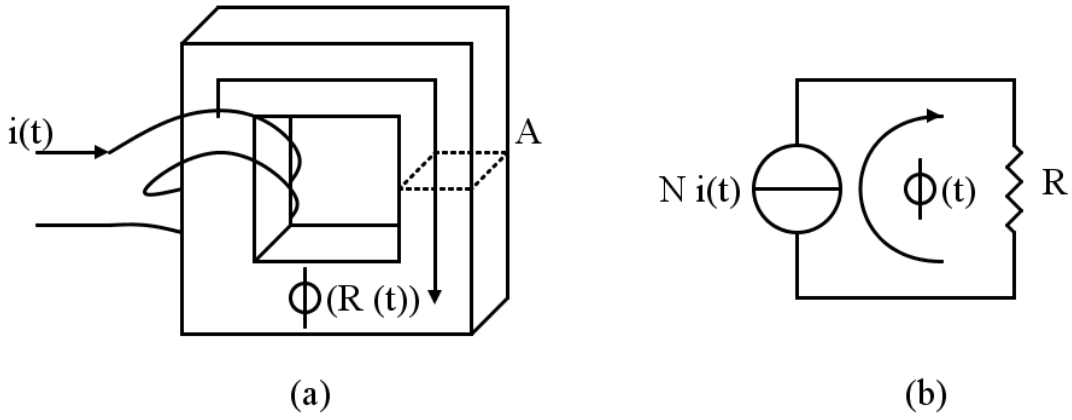


Figure 2.14 – Ferromagnetic core inductor a) and equivalent circuit b).

From the ferromagnetic core inductor topology depicted in Figure 2.14a and from its equivalent circuit in figure 2.14b, it is possible to derive the inductor saturation current (I_{sat}). From the equivalent circuit in Figure 2.14b, equation (4) is derived by using the Kirchhoff's laws:

$$N\, i(t) = \Phi(\mathrm{t}) \cdot R \qquad (4)$$

Substituting:

- $i(t) = I_{sat}$ [A],

- $\Phi(t) = B_{sat}\, A$, with B_{sat} [Tesla] the saturated flux density and A [m^2] the cross-sectional area,

- $R = \frac{H_{sat}\, l}{B_{sat}\, A}$, with H_{sat} [A/m] the saturation magnetic field at B_{sat} and l [m] the effective path length,

the saturation current (I_{sat}) is [6]:

$$I_{sat}[A] = \frac{H_{sat}\, l}{N} \qquad (5)$$

The number of turns needed to realize the inductors L6, L7 and L8 is obtained by the formula:

$$N = \sqrt{\frac{L}{A_L}} \qquad (6)$$

where L is the inductance to be realized and A_L the inductance factor of the toroidal core [7].

The toroidal core selected is the number 5961000601 by Fair Rite, that is made with NiZn ferrite which allows one to realize inductors operating at frequencies up to 25 MHz. Table 2.7 shows some characteristics of the toroidal core 5961000601.

B_{sat}	H_{sat}	Effective length path (l)	A_L
0.235 Tesla	1194 A/m	5.2 10^{-2} m	75 nH

Table 2.7 – Characteristics of the toroidal core 5961000601 (Fair Rite).

Table 2.8 shows the characteristics of the L7, L8 and L9 inductors realized on the toroidal core 59561000601 with turns in enameled wire with diameter of 1 mm.

	Inductance	I_{sat}	Turns
L7	5 µH	7.8 A	8
L8	8 µH	5.6 A	11
L9	12 µH	4.8 A	13

Table 2.8 – Characteristics of inductors on ferrite core.

2.4.4. Low-Frequency Tuner

The tuner was made on FR-4 support with 3 mm traces and a distance between them of at least 1 mm.

Figure 2.15 shows the layout of the tuner realized by using the KICAD program, which is a free software suite for Electronic Design Automation (EDA). Figure 2.16 shows the photograph of the realized prototype.

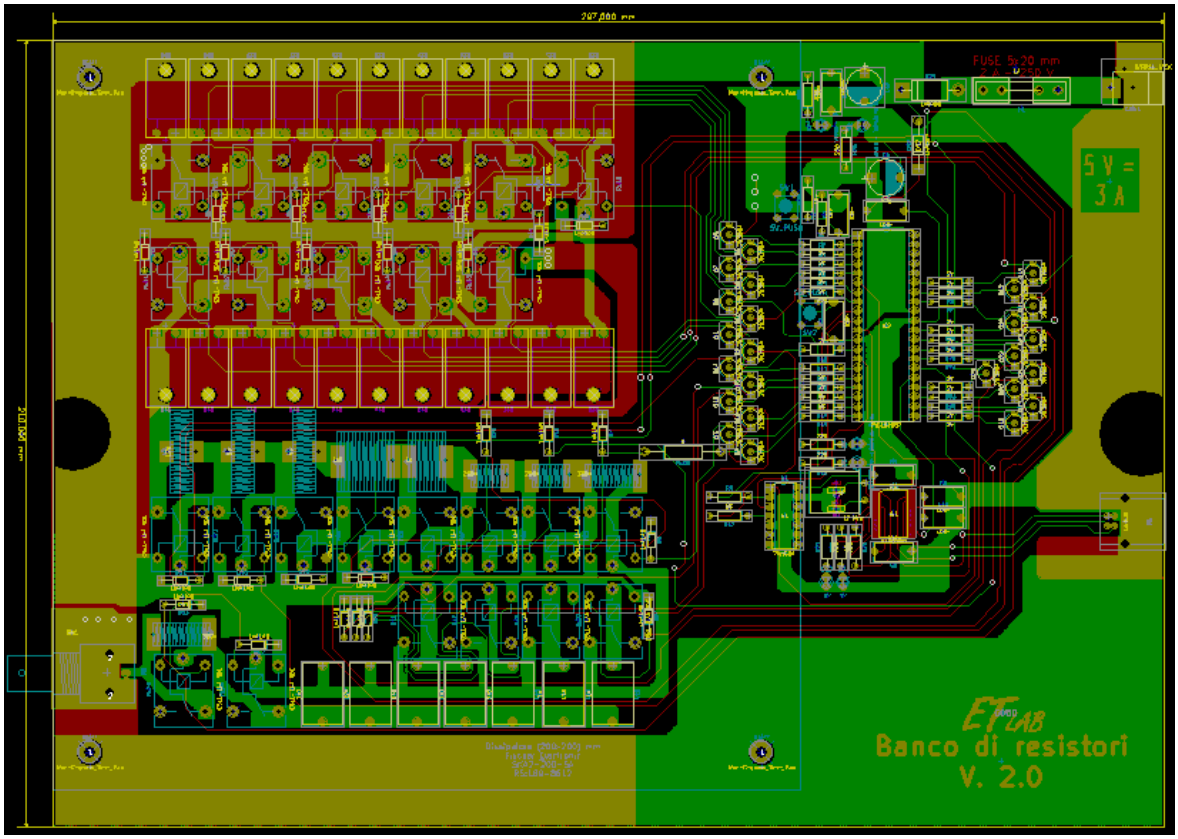


Figure 2.15 – Layout of the realized LF tuner.

Table 2.9 reports the maximum voltages and currents that can be handled by the tuner under continuous regime (DC) and alternate regime (AC).

	Maximum Voltage	Maximum Currents
AC regime	250 V_{rms}[5]	3.5 A_{rms}[6]
DC regime	250 V[5]	5 A[7]

Table 2.9 – Absolute maximum ratings of the designed LF tuner.

[5] Maximum voltage of resistors (Vishay - LTO 50 Series).
[6] Maximum current of enameled copper wire (BLOCK Transformatoren.de – CUL100/1.12).
[7] Maximum current on traces (for over-temperature of the trace of 10 °C).

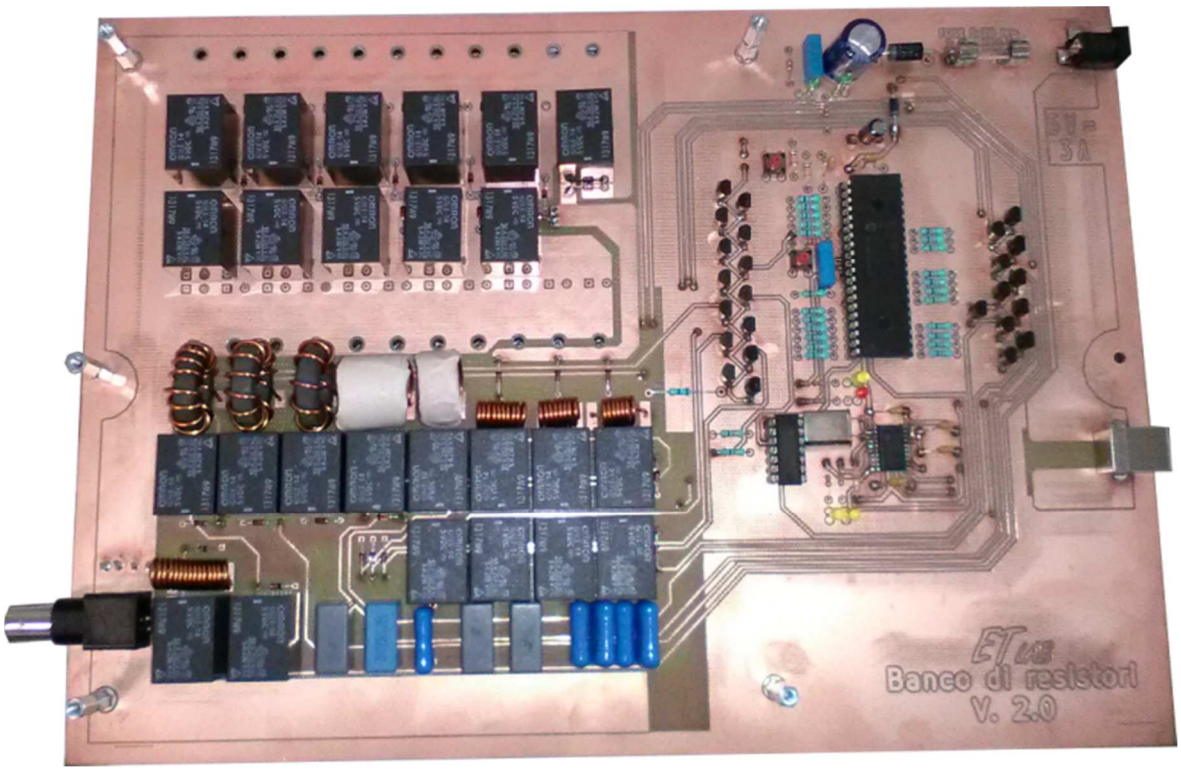


Figure 2.16 – LF tuner.

The LF tuner has been tested with the LSLF measurement setup described in section 2.1. The path from the DUT to the tuner consists of the in-house designed bias tee, a dual-directional coupler (RFC001400-40-100, 0.01-400 MHz produced by RFPA) and two 30 cm cables. In order to test the power capability of the tuner, the DUT in Figure 2.1 is replaced with a power amplifier Vectawave VBA100-30 with maximum output power of 30 W and gain of 46 dB on a 50-Ω load. The nominal loads and the load (R_T, L_T, C_T) configurations are reported in Table 2.10 for the minimum input power level at the amplifier of -36 dBm.

Nominal resistance (Ω)	Load Configuration			Synthesized Impedance for Pav=-36 dBm (Ω)
	Resistance (Ω)	Inductor (μH)	Capacitance (nF)	
25	25	-	14	24.9+j3.3
30	30	-	14	28.5+j1.9
40	45	0.5	-	39.1+j1.6
50	65	0.5	-	49.9+j0.4
75	110	1.9	-	74.8+j0.3
100	280	15.8	-	99.6-j5
150	190	4	-	152.8+j0.9
200	250	20.6	-	191.3+j13.1
300	10	28.6	-	315.1+j8.2

Table 2.10 – Examples of load (R_T, L_T, C_T) configurations.

Figure 2.17 shows the trend of a set of nine impedances in the range between 25 Ω to 300 Ω, varying the input available power (Pav) between -36 dBm and -5 dBm. The reactance variation for impedance values greater than 50 Ω is due to the ferrite losses (eddy currents and hysteresis power losses) and it is about 4% of the nominal resistance value. For impedance values equal or lower than 50 Ω, the reactance variation with respect to the nominal resistance value is about 2%.

Figure 2.18a gives an indication of the power dissipated on the considered loads as a function of the Pav.

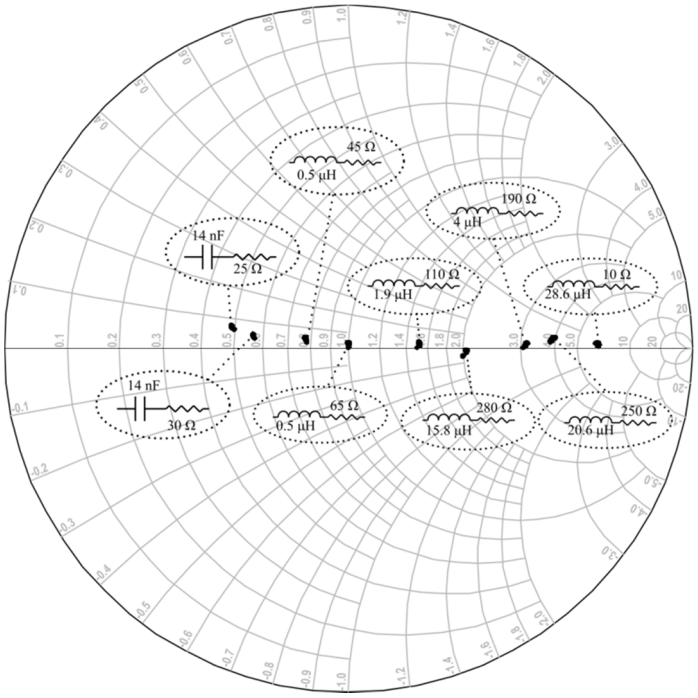


Figure 2.17 – Trend of impedances set in the range between 25 Ω to 300 Ω to vary the power. In the dotted ellipses the tuner configurations are shown.

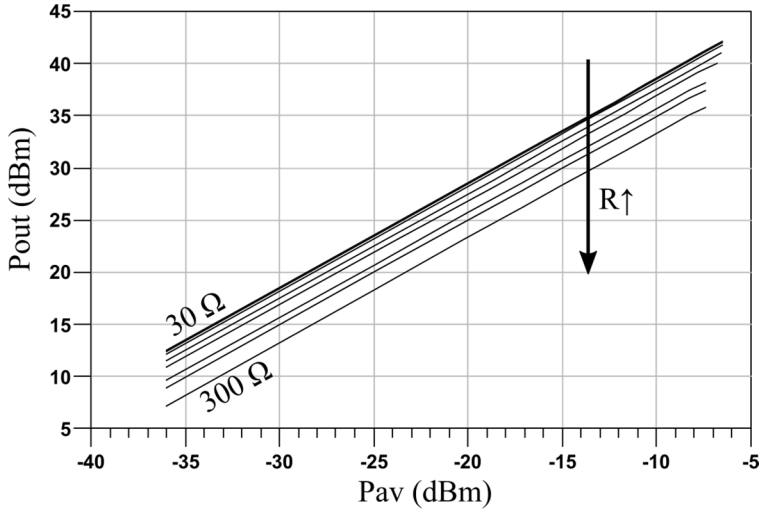


Figure 2.18a – Power dissipated on the loads related to the *nominal resistances* in Table 2.10.

Figure 2.18b shows the path between the DUT and the tuner, where we observe that the bias-tee inductor is in parallel with the tuner output path, being the bias-tee capacitance contribution negligible. The magnitude of the bias-tee parallel-branch impedance measured at the RF+DC port, with the DC port shortened and the RF port terminated with an open circuit, is shown in Figure 2.19a where different self-resonances associated with the different inductors which practically implement the bias tee are evident. In particular, the parallel-branch impedance is about 1000 Ω at the frequency of 2 MHz. Consequently, when resistances greater than 150 Ω are required at the DUT port, the impedance of the bias-tee parallel-branch is not negligible. Higher resistance values can still be obtained, but require the exploitation of resonance effects involving the bias-tee parallel-branch itself. To obtain the nominal resistance of 300 Ω in Table 2.10, resonance effects have been exploited using the series of a 10 Ω (R_T) resistor and a 28.6 μH (C_T) inductor. However, the frequency variation of the bias-tee impedance and the use of resonant circuits do not ensure constant impedance at the harmonic frequencies compared to the fundamental frequency impedance. This is observed in Figure 2.19b for the greatest values of resistive impedance (i.e., 300 Ω and 600 Ω at 2 MHz), while for resistance values up to 150 Ω the impedance at the harmonics is similar to the one at the fundamental (up to the 5th harmonic). To improve the impedance values at the harmonics, it is necessary to implement a suitable low-frequency multiplexer which will be described in the next paragraph.

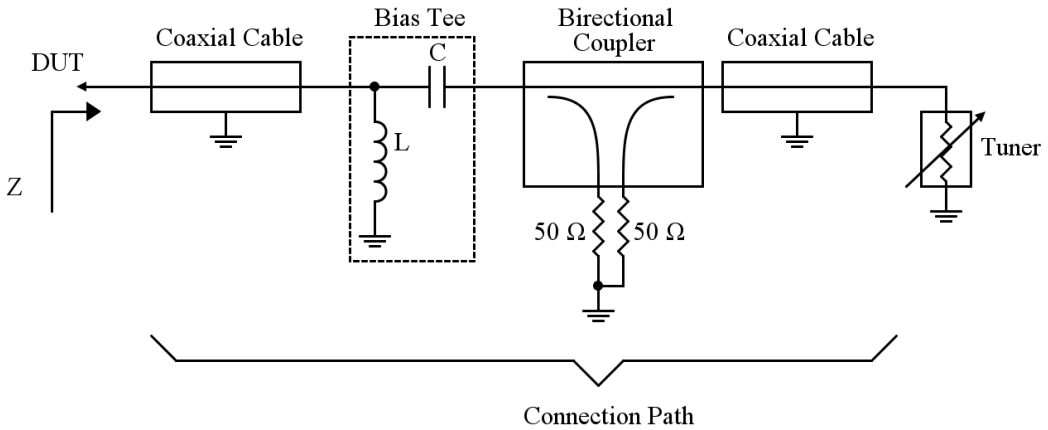


Figure 2.18b – Block diagram of the structure between the DUT and the tuner.

To summarize, the tuner allows the synthesis of real impedances at 2 MHz between 30 Ω and 300 Ω, managing powers higher than 15 W. The system has a good power stability with reactance variations ≤ 4% with respect to the synthetized resistance. The set

of inductors and capacitors allow the synthesis of real/imaginary impedances too; this aspect could be useful for generating load-pull maps.

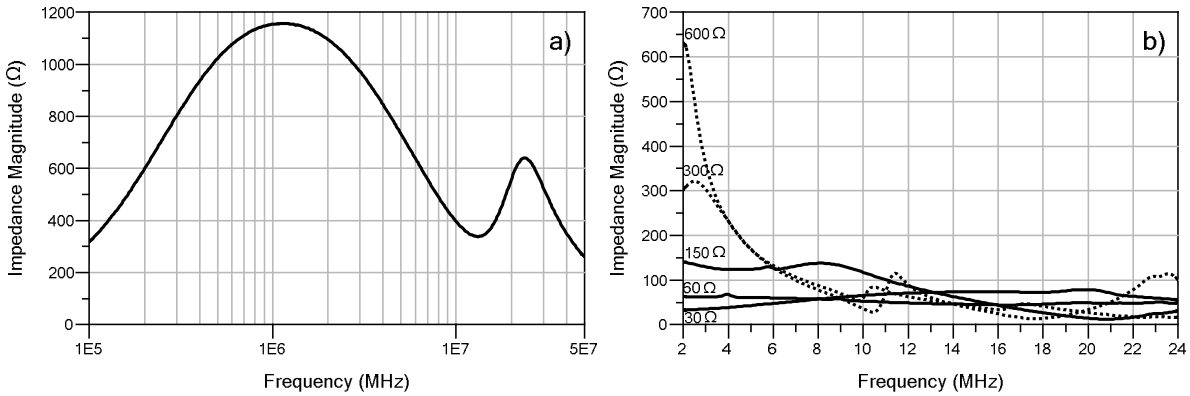


Figure 2.19 –Magnitude impedance of the bias tee inductor (a) and impedance at the fundamental frequency and the harmonics (b) measured with the Agilent E5061E VNA.

2.5. Low-frequency multiplexer

2.5.1. Introduction

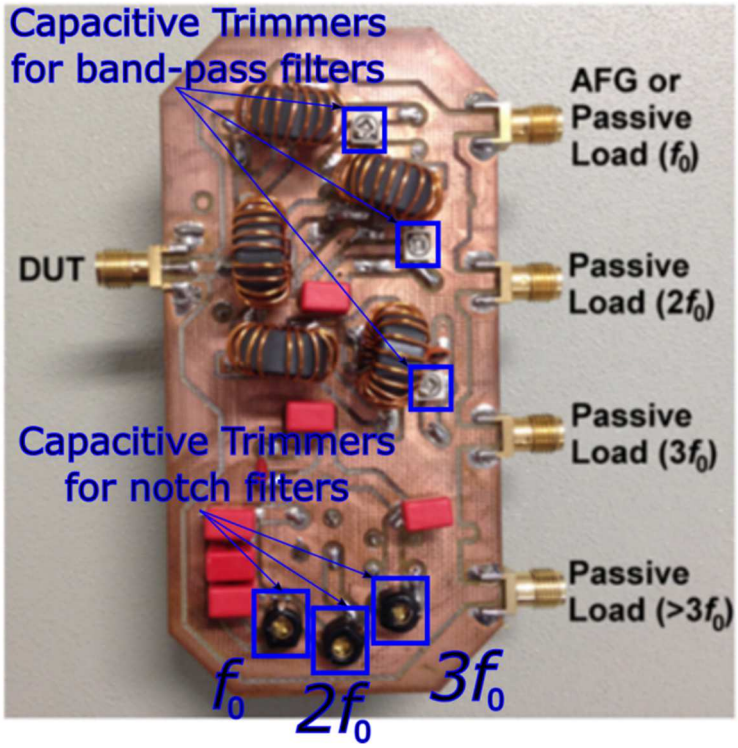


Figure 2.20 – Low-frequency multiplexer.

The LF tuner is designed to handle the load terminations at the frequency of 2 MHz (fundamental frequency - f_0) and it does not allow handling the terminations at the harmonic frequencies, which are necessary for the *waveform-engineering* design technique. The multiplexer usually adopted for this purpose at microwave frequencies [16]

can be realized at LF by using a solution based on lumped components. Figure 2.20 shows the realized LF multiplexer, while Figure 2.21 illustrates its electrical schematic.

The multiplexer is composed of three (series-resonant) band-pass and three (parallel-resonant) notch filters. Band-pass filters allow setting the load terminations at the fundamental frequency (f_0), second harmonic ($2f_0$), and third harmonic ($3f_0$). In the preliminary design, the harmonic frequencies above the third harmonic ($>3f_0$) were terminated on a suitable load by means of a high-pass filter. However, from accurate simulations it was found that this high-pass filter did not guarantee an adequate attenuation in the stopband even by increasing the filter order. For such a reason, it has been implemented a solution based on three notch filters (parallel resonant at f_0, $2f_0$ and $3f_0$) to apply a suitable load termination above $3f_0$. In addition, it is noted that the resistance applied to the output of a band-pass filter represents a loss of the LC series resonant circuit which, when a high value is needed, can dramatically reduce its quality factor to the point of making the filter useless. The notch filters are also used to impose open-circuit terminations at the frequencies $2f_0$ and $3f_0$ to handle, for example, the class F (open at $3f_0$) or class F^{-1} (open at $2f_0$) operations. Indeed, by generating open circuits with the notch filters, we can accurately manage the impedance shown to the DUT as will be seen later. On the other side, the band-pass filters are mainly used to impose load terminations up to 250 Ω at the fundamental frequency and to impose low resistance values at the frequencies $2f_0$ and $3f_0$ to handle, for example, the tuned-load configuration.

When we operate at LF, as previously observed, it is possible to set the load terminations directly at the transistor output port (nearly coincident with the current-generator plane). Moreover, it is often sufficient to apply only real impedances. The capacitive trimmers, visible in Figure 2.20, allow one to tune the filters and impose any real impedance at the DUT output port, at the fundamental frequency and harmonics. In fact, by varying the resonance frequency of the filters, the reactances at the fundamental frequency and harmonics can be properly modified. These reactances allow compensating the ones introduced by the cables, bias tee and coupler (see the connection path in Figure 2.21a), which modifiy the impedance value applied to the branch f_0. Figure 2.21b shows the reflection coefficient (at 2 MHz) of the connection path when varying the resistance (R) connected at the f_0 branch, the coaxial cable length (Δz) and the inductance (L) of the bias tee: to obtain a resistive impedance at the DUT port, the multiplexer must compensate the reactances of the impedances shown in Figure 2.21b.

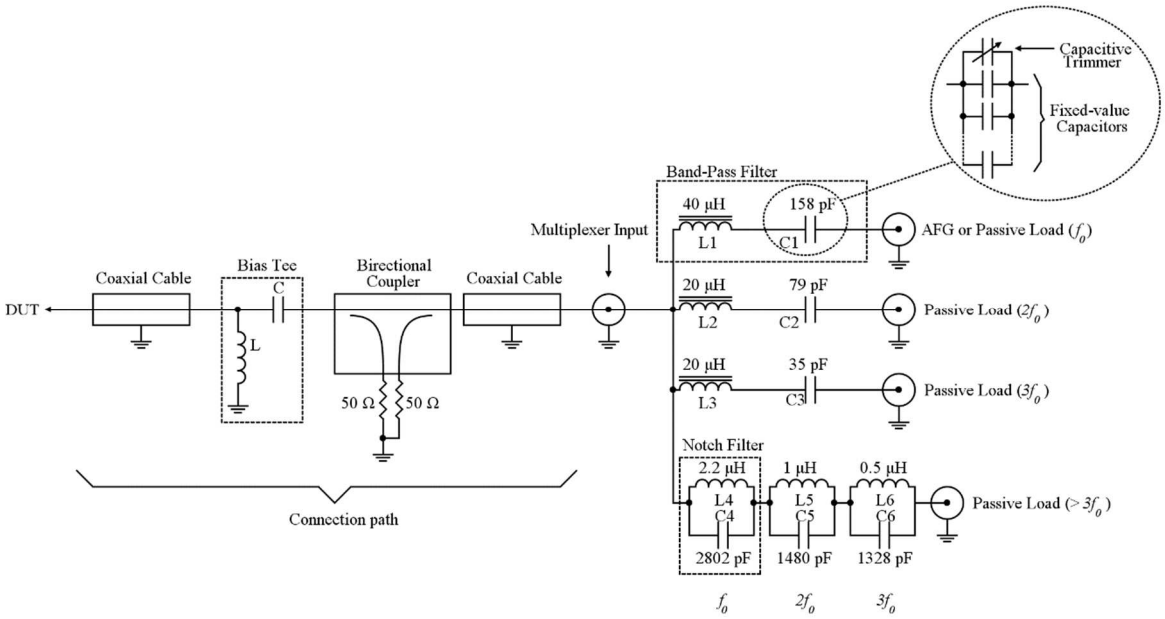


Figure 2.21a – Schematic of the multiplexer and the connection path with the DUT.

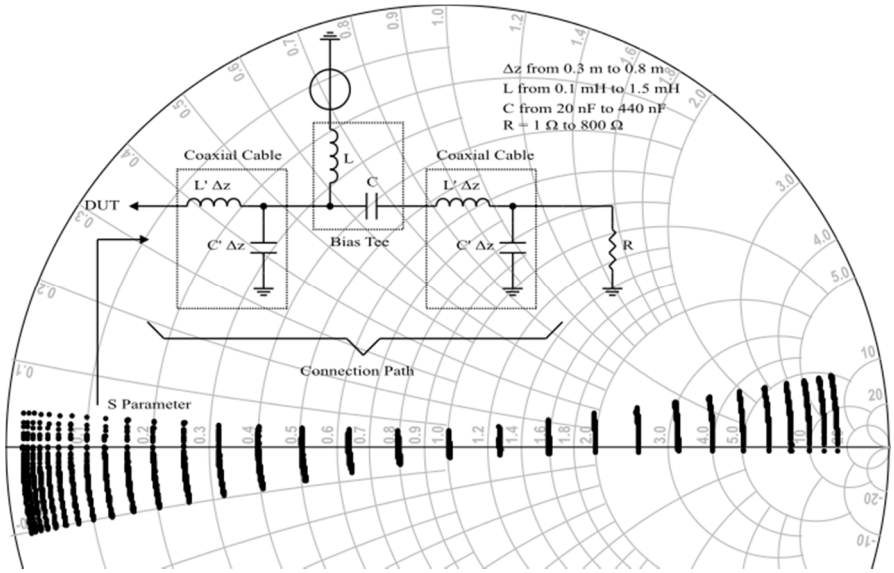


Figure 2.21b – Simulated reflection coefficient (2 MHz) of the connection path when varying the length of the coaxial cable (Δz), the load resistance (R) and the inductance (L) of the bias tee. The schematic represents the simulated connection path.

Figure 2.21c shows the impedances (area highlighted in red) that the band-pass filter is able to synthesize at the frequency of 2 MHz (f_0) at its "Input" port (see Figure 2.21a), when varying the resistance applied to the branch f_0 between 1 Ω to 800 Ω and the trimmer capacitance C1 between 153 and 163 pF.

Figure 2.21d shows the impedances that the multiplexer can synthetize (highlighted in red) superimposed on the conjugate of the reflection parameter associated with the connection path (highlighted in black) at the frequency of 2 MHz. Since the connection path and the multiplexer are series connected, the area highlighted in red in Figure 2.21d represents the compensable area of the branch at 2 MHz. As previously discussed for the

tuner, we approximated the circuit formed by the connection path and the multiplexer as a series of impedances to get a first estimate of the multiplexer coverage area.

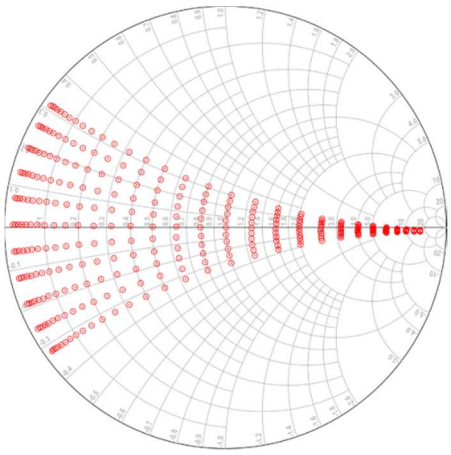


Figure 2.21c – Reflection coefficient area that the multiplexer can compensate at the frequency of 2 MHz.

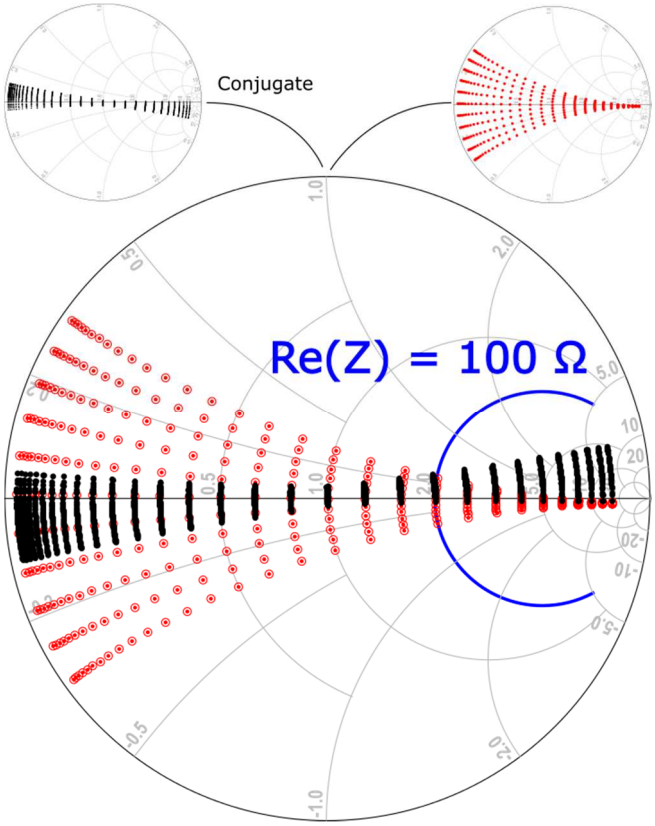


Figure 2.21d – Reflection coefficient area that the multiplexer can compensate (highlighted in red) superimposed on the conjugate reflection coefficient associated with the connection path between the DUT and the multiplexer (highlighted in black) at the frequency of 2 MHz.

The same considerations apply for the band-pass filters at 4 MHz ($2f_0$) and 6 MHz ($3f_0$). Figure 2.22 shows the reflection coefficient area that the multiplexer can compensate (highlighted in red) superimposed on the conjugate reflection coefficient associated with

the path between the DUT and the multiplexer (highlighted in black) at the frequency of 4 MHz and 6 MHz respectively.

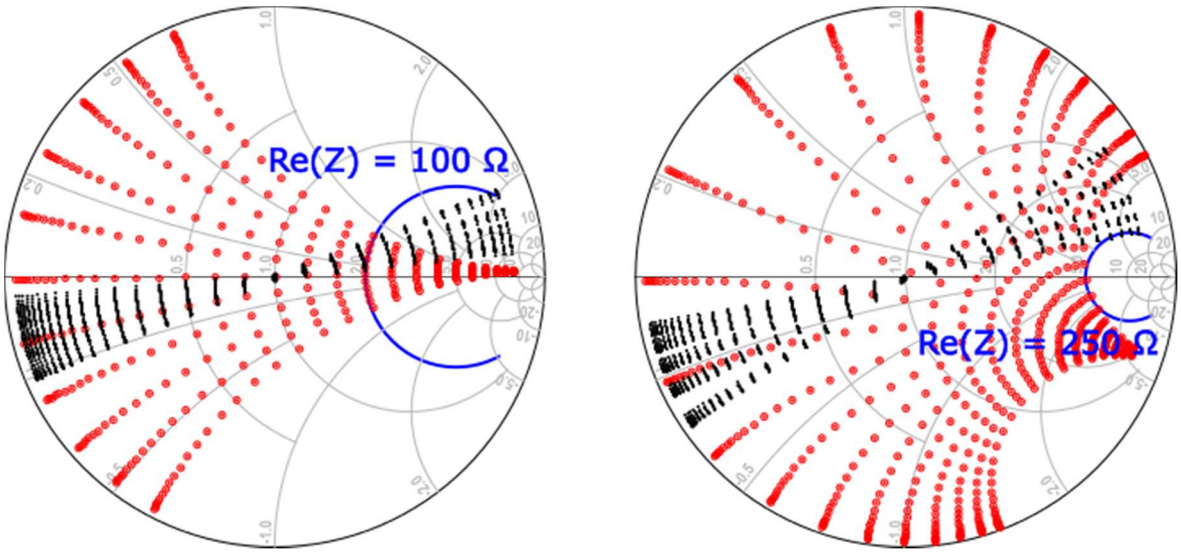


Figure 2.22 – Reflection coefficient area that the multiplexer can compensate (highlighted in red) superimposed on the conjugate reflection coefficient associated with the path between the DUT and the multiplexer (highlighted in black).

Figure 2.21d and Figure 2.22 show that for the highest impedance values (i.e., over 100 Ω in magnitude for 2, 4 MHz and over 250 Ω in magnitude for 6 MHz), the multiplexer, in this rough approximation, cannot compensate the reactive effects. However, for the fundamental frequency it is possible to exploit the compensation capabilities of the LF tuner described in section 2.4. Indeed, the LF tuner is able to compensate all the reactances of the upper half of the Smith chart as shown in Figure 2.10. Moreover, at the frequencies of 4 and 6 MHz the load terminations are typically short circuits or open circuits that are correctly managed by the band-pass (series resonant) and notch (parallel resonant) filters in Figure 2.21a. This is consistent with the application for which the multiplexer is thought, since the most common waveform engineering classes impose at the current-generator plane only short circuits or open circuits at the harmonic frequencies.

The considerations made for the band-pass filters are similar for the notch filters. Figure 2.23a depicts the reflection coefficients (areas highlighted in red) that the notch filters are able to compensate at the frequencies of 2 MHz, 4 MHz and 6 MHz, while the areas highlighted in black represent the conjugate reflection parameters generated by the paths when R is infinite (i.e., open circuit). Indeed, as explained above, the notch filters are mainly used to generate and control the impedance value in the open-circuit conditions at $2f_0$ and $3f_0$. Notch filters are in parallel to the band-pass ones and must show real impedances not to change the behavior of the latter.

As seen from Figure 2.23a, the notch filters cannot compensate the reactive effects in every condition, although it is still possible to insert selectable capacitors by means of jumpers included in the multiplexer PCB. The additional capacitors shift the reflection coefficient (highlighted in red in Figure 2.23a) clockwise, covering new areas of the Smith chart. The choice of adopting additional capacitors with insertion jumpers is motivated by the lack of ceramic capacitive trimmers with values greater than 120 pF.

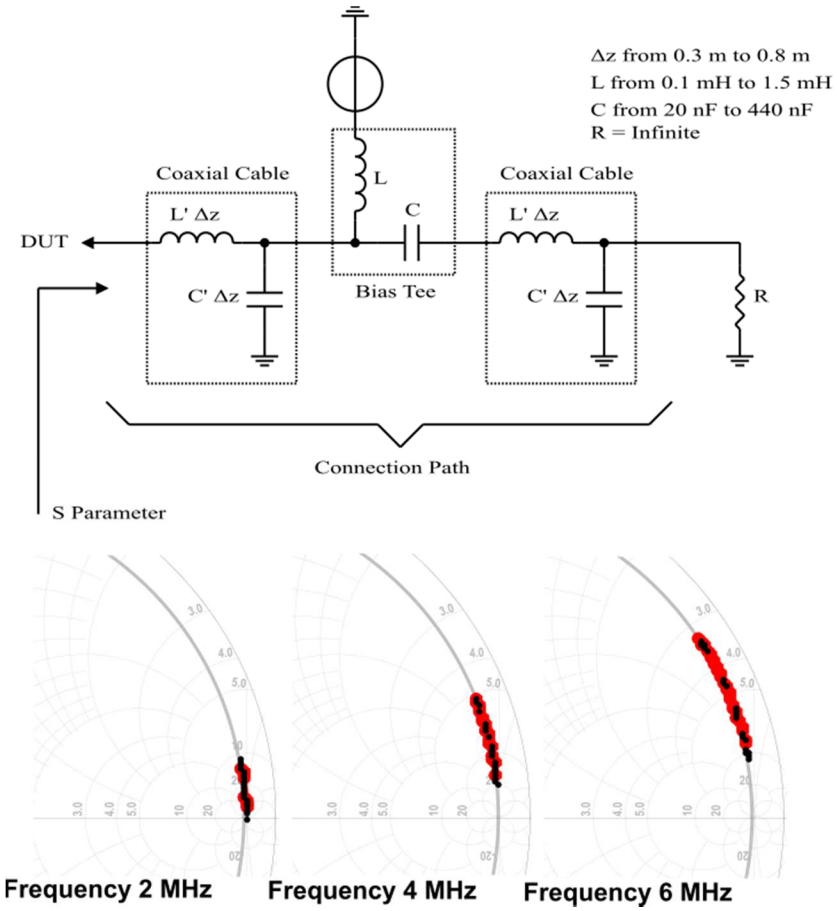


Figure 2.23a – Reflection coefficient areas that the multiplexer can compensate (highlighted in red) superimposed on the conjugate reflection parameter associated to the path between the DUT and the multiplexer (highlighted in black) when R is an open circuit. The schematic represents the simulated connection path.

Figure 2.23b shows the simulated reflection parameter at the DUT plane obtained from the cascade between the connection path and the multiplexer when varying the path characteristics (L, C, Δz as shown in Figure 2.23c), the capacitive trimmers and the resistance at the output of each band-pass filter. Each theoretical capacitor in Figure 2.21 is implemented in the circuit of Figure 2.20 through the parallel of fixed-value capacitors and one capacitive trimmer with maximum capacitance of 10 pF for the band-pass filters and 120 pF for the notch filters (see Table 2.14). The band-pass filter capacitance at frequency f_0 (C1) may vary between 153 pF to 163 pF (the theoretical value of 158 pF in Figure 2.21a $\in [153 \div 163]$ pF), while the band-pass filter capacitance at frequency $2f_0$ (C2) may vary

between 74 pF and 82 pF. Finally, the band-pass filter capacitance at frequency $3f_0$ (C3) may vary between 30 pF and 40 pF. To improve the figure readability, only real impedances were considered at the output of each band-pass filter.

Figure 2.23d shows the reflection coefficient at the DUT plane obtained from the cascade between the connection path and the multiplexer when varying the path characteristics (L, C, Δz as show in Figure 2.23c) and the capacitive trimmer (120 pF) of each notch filter. In this case, the band-pass filters are terminated on an open circuit. The schematic in Figure 2.21a shows that the notch filters are connected in parallel to the band-pass filters; if the capacitive trimmers of the notch filters were not tuned to obtain a purely real impedance, the corresponding band-pass filter would have to be tuned to compensate the connection path and the notch filter reactances. The notch filter capacitance at frequency f_0 (C4) may vary between 2742 pF and 2862 pF, while the notch filter capacitance at frequency $2f_0$ (C5) may vary between 1420 pF and 1540 pF. Finally, the band-pass filter capacitance at frequency $3f_0$ (C6) may vary between 1268 pF and 1388 pF

From Figure 2.23b and Figure 2.23d we note that the multiplexer is capable of showing real impedances at the DUT plane in the range [1 Ω - 100 Ω] for the fundamental frequency and second harmonic and [1 Ω – 250 Ω] for the third harmonic (intersection of the loci with the real axis), even varying the characteristics of the connection path. In particular, Figure 2.23d shows that the notch filters can be tuned to obtain purely real impedances for each path; the tuning of the notch filters at the harmonics allows the synthesis of the load terminations for the inverse F (second harmonic) or F (third harmonic) class at the DUT plane.

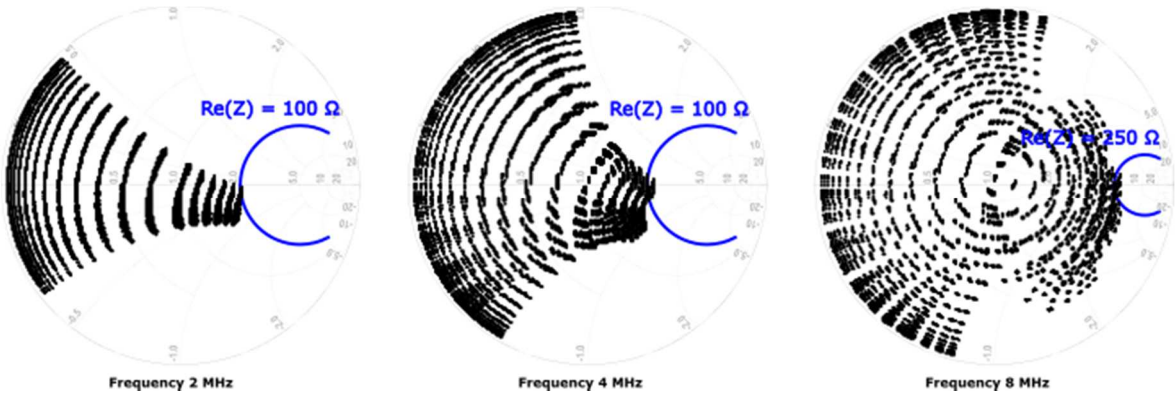


Figure 2.23b – Reflection coefficient at the DUT plane varying the path characteristics (L, C, Δz as shown in Figure 2.21b), the resistance at the output port of the band-pass filter and the capacitive trimmers of each band-pass filter. Above 100 Ω (for 2 MHz and 4 MHz) and 250 Ω (for 6 MHz), the multiplexer is not capable of synthesizing resistive impedances. For this reason, the curves above these values have not been plotted.

In our laboratory setup, the existing connection path has the following characteristics: Δz = 0.5 m, C = 100 nF and L = 470 μH (see Paragraph 2.3). Figure 2.23e shows the simulation of the reflection coefficient at the DUT plane when varying the capacitance trimmer of each band-pass filters (10 pF) and the resistance at the output of the band-pass filter with the characteristics of the path just described. From Figure 2.23e we observe that for each resistance applied to the output of the band-pass filters (i.e., up to 100 Ω for the fundamental frequency and second harmonic and up to 250 Ω for the third harmonic) does exist a capacitance value of the corresponding trimmers that allows seeing at the DUT plane a real impedance (intersection of the loci with the real axis).

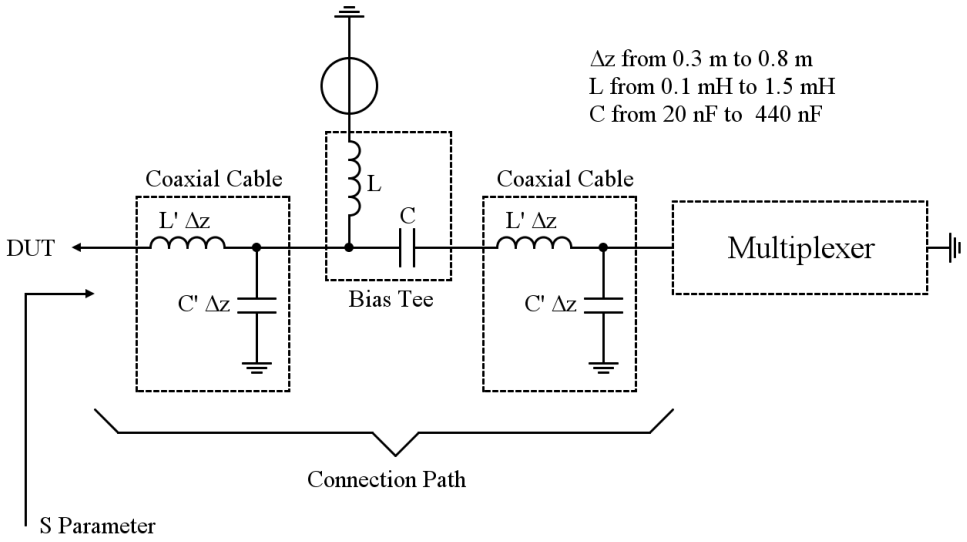


Figure 2.23c - Circuit simulated for the connection path and multiplexer.

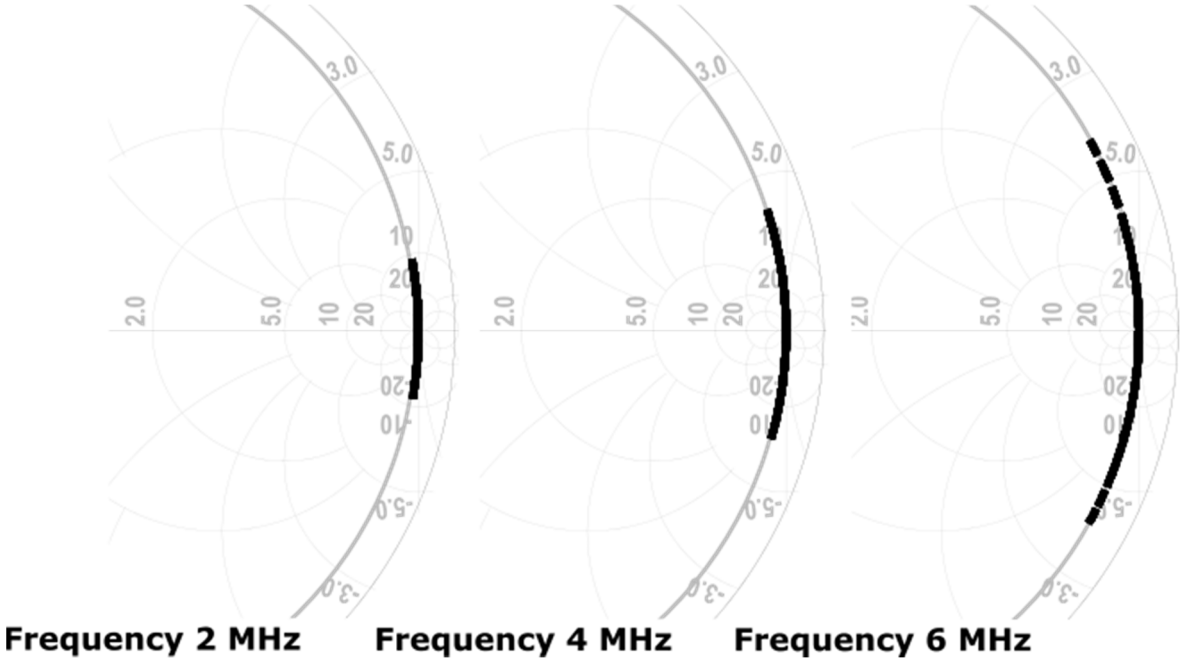


Figure 2.23d – Reflection coefficient at the DUT plane varying the path characteristics (L, C, Δz as shown in Figure 2.21b) and each capacitive trimmer of the notch filters.

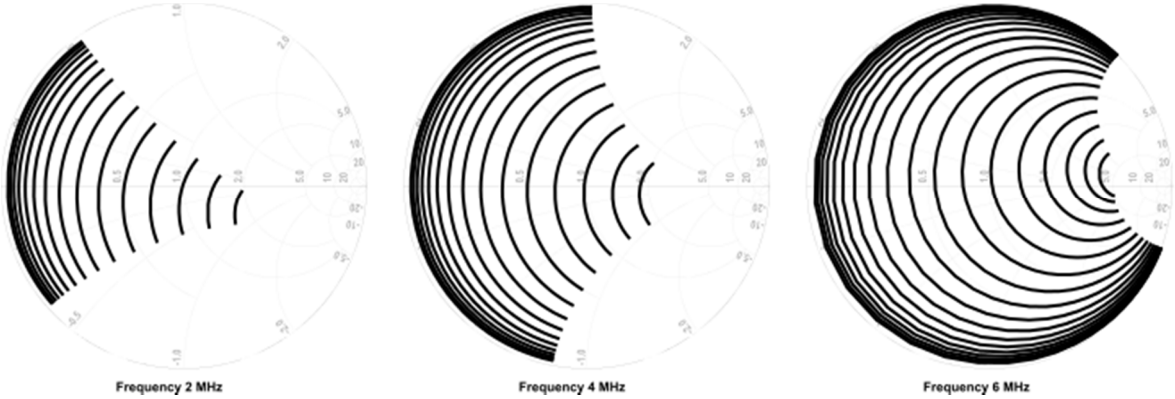


Figure 2.23e – Reflection coefficient at the DUT plane with constant Δz=0.5 m, L=470 μH, C = 100 nF and varying the resistance at the output of the band-pass filter (up to 250 Ω) and the trimmer capacitance (10 pF). Above 100 Ω (for 2 MHz and 4 MHz) and 250 Ω (for 6 MHz), the multiplexer is not capable of synthesizing resistive impedances. For this reason, the curves above these values have not been plotted.

In Figure 2.23f we show the reflection coefficient simulation varying the capacitance trimmer of the notch filters (120 pF) with the following characteristics of the connection path: Δz = 0.5 m, C = 100 nF and L = 470 μH (see Paragraph 2.3) and with the output of the band-pass filters on open circuits. From Figure 2.23f we observe that a capacitance value of the corresponding trimmers does exist that allows seeing at the DUT plane a real impedance (intersection of the loci with the real axis). The importance of the notch filters tuning at the fundamental frequency and harmonics has been previously outlined.

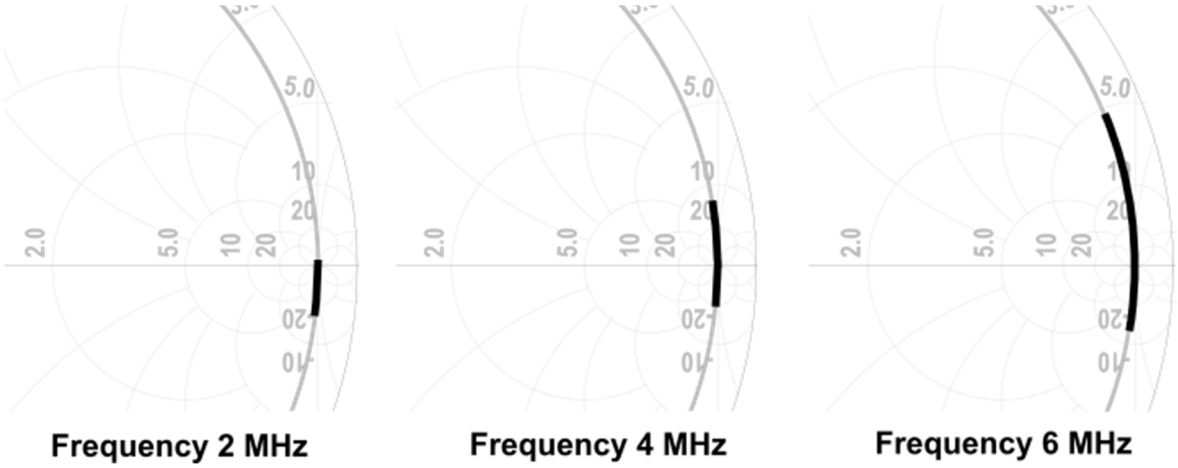


Figure 2.23f – Reflection coefficient at the DUT plane with constant Δz=0.5 m, L=470 μH, C = 100 nF and varying the capacitance trimmer of the notch filters (120 pF) with the band-pass filter terminated with an open circuit.

The inductors used for L1, L2 and L3 in Figure 2.21a are made on ferrite core using material 67 by Fair Rite. This core is a NiZn ferrite and allows realizing inductors operating at frequencies up to 50 MHz.

Table 2.11 shows the characteristics of material 67, while Table 2.12 reports the characteristics of inductors on ferrite core and Table 2.13 shows the characteristics of air inductors.

Part Number	B_{sat}	H_{sat}	Effective length path (l)
5967000601	0.235 Tesla	1194 A/m	$5.2\ 10^{-2}$ m
5967001101			$3.12\ 10^{-2}$ m

Table 2.11 – Characteristics of toroidal cores in material 67 (Fair Rite).

	Inductance	I_{sat}	Turns
L1	3 x 13.4 µH ≈ 40 µH	3.8 A	22 on 5967000601
L2	2 x 10 µH = 20 µH	2.5 A	20 on 5967001101
L3	3 x 6.7 ≈ 20 µH	3 A	17 on 5967001101

Table 2.12 – Characteristics of inductors on ferrite core.

	Inductance	Inner diameter (mm)	Length (mm)	Turns
L4	2.2 µH	16	15	11
L5	1 µH	16	9	7
L6	500 nH	16	6	5

Table 2.13 – Table of characteristics of the coils on air.

2.5.2. Realization and Tuning of the Multiplexer

The multiplexer in Figure 2.20 is realized on FR-4 substrate with 3 mm traces (implementing a 50-Ω transmission line) and a distance between the traces of at least 1 mm. The selected capacitors are made with polypropylene with maximum DC voltage of 100 V and Equivalent Series Resistance ESR < 1 Ω as shown in Figure 2.24, while the capacitive trimmers are of a ceramic type. Table 2.14 shows the characteristics of the capacitive trimmers and the capacitors in Figure 2.21a: the total capacitance values (obtained by the parallel of the values reported in Table 2.14) are lower with respect to the theoretical values in Figure 2.21a, to take into account the parasitic capacitances of the traces. Traces capacitances can be calculated as the capacitances associated at the parallel plate capacitor, i.e. $C_{trace} = \varepsilon \frac{A}{d}$, where A is the area of the plate, d the thickness of the dielectric and permittivity ε = 4.35 (for FR-4).

The tuning is carried out by adjusting the capacitive trimmers on the electronic board. More precisely, it is performed by connecting the multiplexer as shown in Figure 2.25. The path is formed by the bias-tee described in Paragraph 2.3, a dual-directional coupler (RFC001400-40-100, 0.01-400 MHz produced by RFPA) and two cables with characteristic impedance of 50 Ω and length 30 cm. This tuning procedure allows setting real impedances at the DUT plane, i.e., it allows one to compensate the reactive effects of the path.

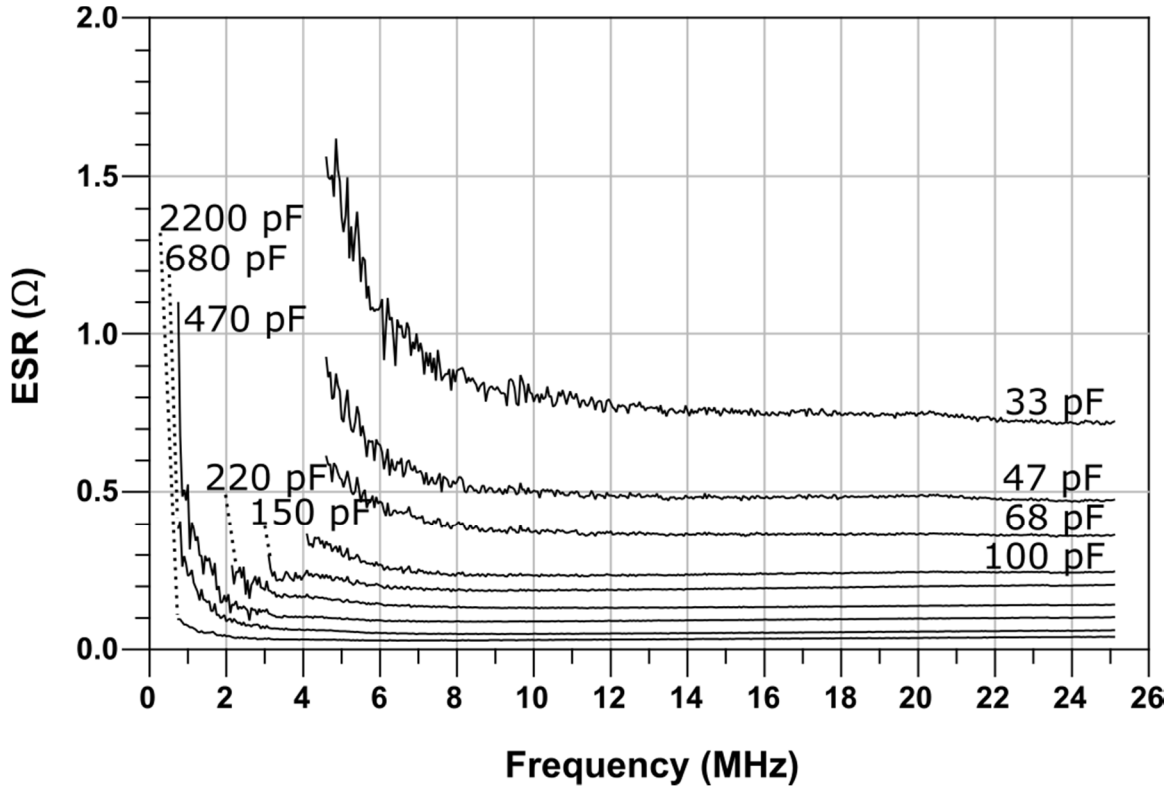


Figure 2.24 – Equivalent Series Resistance of polypropylene capacitor FKP2 Series (WIMA) measured up to 25 MHz with the Agilent E5061E VNA.

	Value	Material	Maximum Voltage	Series	Mounting
C1[8]	100 pF±5%	Polypropylene	100 Vdc 63 Vac	FKP2 – WIMA	Hole
	24 pF±5%[9]	Ceramic	100 Vdc	-	
	3÷10 pF	Ceramic	100 Vdc	TZB4 – Murata	SMD
C2	47 pF±5%	Polypropylene	100 Vdc 63 Vac	FKP2 – WIMA	Hole
	3÷10 pF	Ceramic	100 Vdc	TZB4 – Murata	SMD
C3	15 pF±5%	Ceramic	100 Vcc	RCE – Murata	Hole
	3÷10 pF	Ceramic	100 Vdc	TZB4 – Murata	SMD
C4	2.2 nF±5%	Polypropylene	100 Vdc 63 Vac	FKP2 – WIMA	Hole
	470 pF±5%				
	33 pF ±5%				
	10÷120 pF	Ceramic	100 Vdc	TZ03 – Murata	Hole
C5	680 nF±5%	Polypropylene	100 Vdc 63 Vac	FKP2 – WIMA	Hole
	150 pF±5%				
	150 pF±5%				
	10÷120 pF	Ceramic	100 Vdc	TZ03 – Murata	Hole
C6	680 nF±5%	Polypropylene	100 Vdc 63 Vac	FKP2 – WIMA	Hole
	68 pF±5%				
	47 pF±5%				
	10÷120 pF	Ceramic	100 Vdc	TZ03 – Murata	Hole

Table 2.14 - Characteristics of the capacitive trimmers and capacitors.

[8] The total value of C1 is given by the parallel of the capacitances reported in the column "*Value*". The same for the next capacitors in Figure 2.21a.
[9] Value not present in the FKP2 Series.

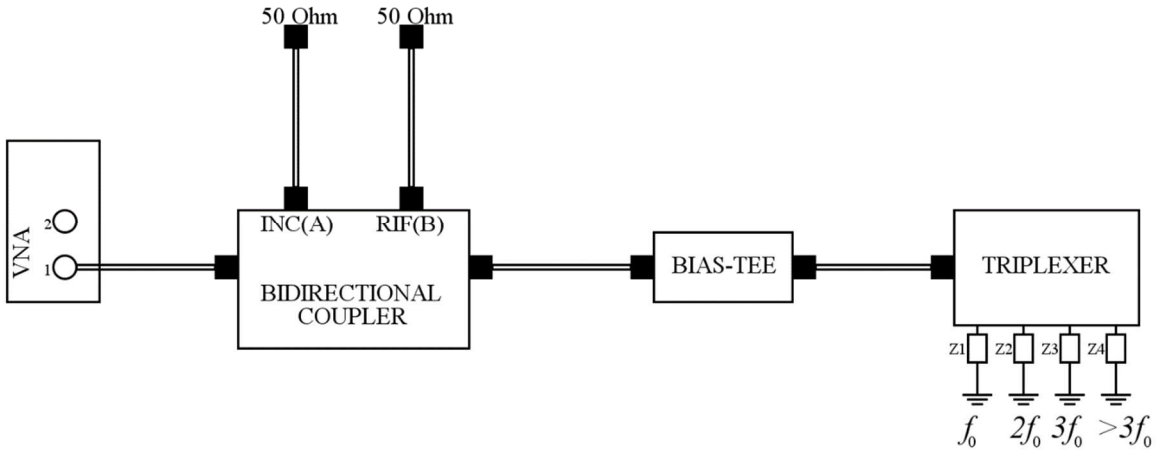


Figure 2.25 – Block diagram for tuning of the multiplexer.

Due to the interactions between the inductors and the layout of the electronic board, the following calibration technique was developed.

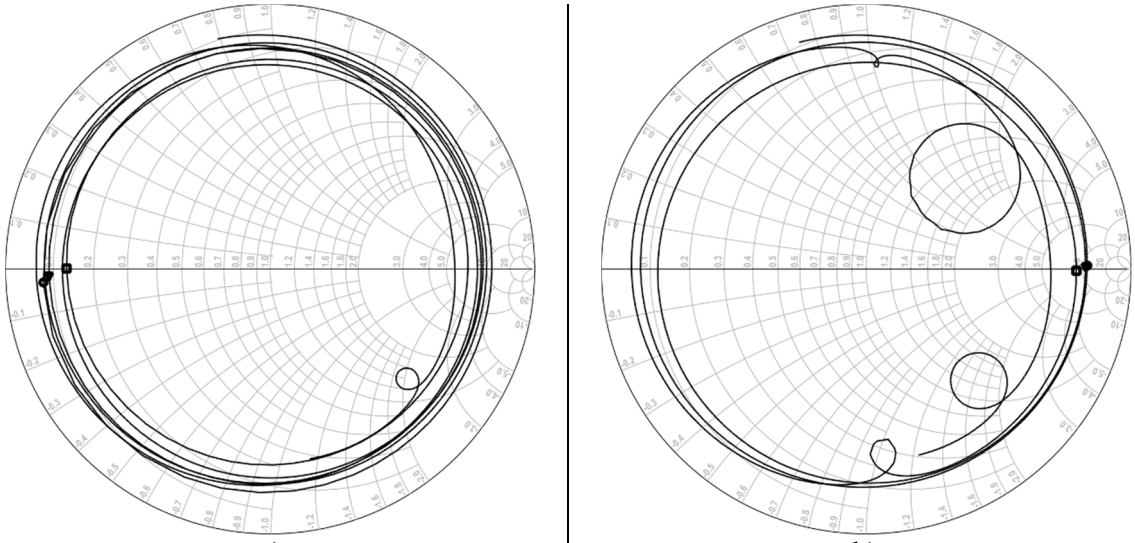
The tuning of the parallel resonant cells (for the branch at frequencies > $3f_0$) is achieved by closing the branches at frequency f_0, $2f_0$ and $3f_0$ on open circuits and the branch at the frequency > $3f_0$ on short circuit and adjusting the notch-filter capacitive trimmers to synthesize a resistive impedance at f_0, $2f_0$ and $3f_0$ (these values represent the maximum resistance values that the multiplexer can synthetize). In the next calibration step, the branch at f_0 is terminated with a short circuit and the capacitive trimmer of its LC series cell is used to synthesize a resistive impedance at f_0 (this is the minimum resistance that the multiplexer can synthetize at the fundamental frequency). In this step the other not-tuned LC series cells are terminated with an open circuit, whereas the notch filters are terminated with a short circuit. Then the same procedure is repeated for the other LC series cells at the frequency of $2f_0$ and $3f_0$.

Table 2.15 reports the minimum and maximum measured resistance that the multiplexer may set, while Figures 2.26 shows the trend of the measured reflection parameters using the Agilent E5061E-VNA between 1 MHz and 26 MHz (from which the values in Table 2.15 have been obtained).

	Minimum Resistance (Ω)	Maximum Resistance (Ω)
2 MHz	3.8	552
4 MHz	4.5	532
6 MHz	6.5	436
> 6 MHz	3.5 at 8 MHz	-

Table 2.15 – Minimum and maximum resistance that the multiplexer may impose. The maximum resistance is achieved by terminating the band pass filters on open circuits and notch filters on short circuits.

Figure 2.27 shows the impedance magnitude measured up to 26 MHz, imposing a short circuit at all the frequencies. As can be seen, due to the layout and the self-resonance frequency of the inductors, it is not possible to set a low-impedance condition at the harmonics above 8 MHz (4th harmonic).



a) b)

Figure 2.26 – Reflection parameter measured using the Agilent E5061E-VNA between 1 MHz and 26 MHz related to minimum (a) and maximum (b) resistances that can be applied at fundamental frequency f_0 (circle), second harmonic frequency $2f_0$ (triangle) and third harmonic frequency $3f_0$ (square).

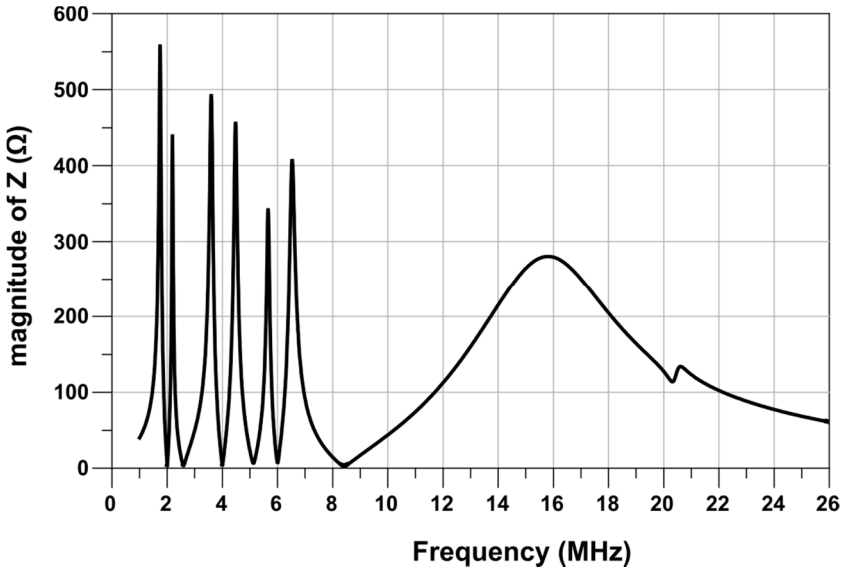


Figure 2.27 – Impedance magnitude measured up to 26 MHz, imposing the short circuit at all the harmonics (worst case).

The described multiplexer has been tested with the LF measurement setup by characterizing a GaN HEMT device. In Figure 2.28, LF measurements on a 0.5-µm GaN HEMT having a total periphery of 1 mm are reported for two different classes of operation at 2 MHz, i.e., tuned-load class-AB and class-F [9,10], with the device biased at V_{DQ} = 22

V, I_{DQ} = 50 mA. The comparison between the two classes of operation is shown for the same level of input power, whereas the fundamental load impedance has been properly selected to maximize the output power. It is very clear the different shape of the load lines, which corresponds to a different performance, as reported in Table 2.16.

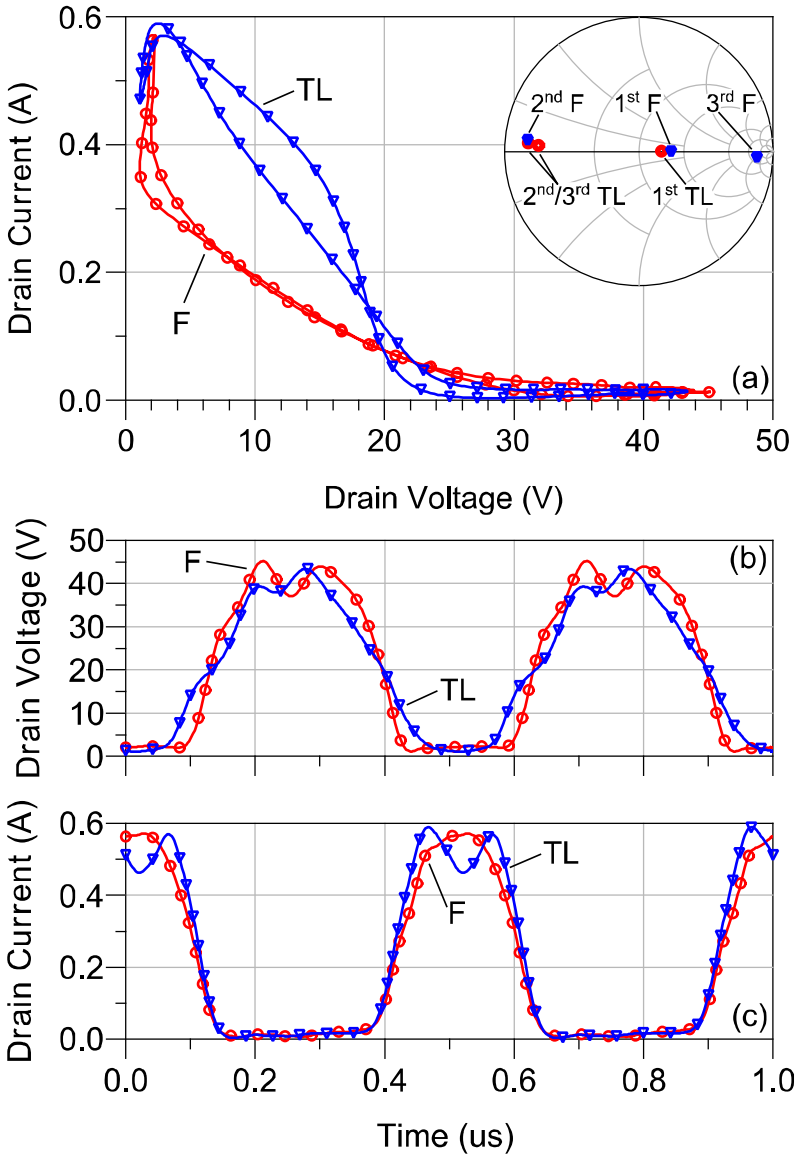


Figure 2.28 – Example of low-frequency measurements with harmonic tuning: tuned-load (TL) class-AB and class-F operations synthesized at the current-generator plane (2 MHz). (a) Load lines and harmonic terminations in the inset; (b) drain voltages; (c) drain currents.

Class	Available Input Power	Output Power	Drain Efficiency	Load Condition
AB TL	13.4 dBm	35.0 dBm (3.2 W)	69.4%	70.2 + j0.3 Ω @ f0 4.8 + j1.9 Ω @ 2f0 7.1 + j1.5 Ω @ 3f0
F		35.4 dBm (3.5 W)	78.7%	81.2 – j0.3 Ω @ f0 4.6 + j2.5 Ω @ 2f0 670 – j255 Ω @ 3f0

Table 2.16 – Comparison between measured tuned-load class-AB and class-F operating conditions at low-frequency.

In conclusion, the multiplexer allows handling the terminations at the frequency of 2, 4, 6 and 8 MHz. The range of load terminations at the fundamental frequency may vary from 3.8 Ω to 552 Ω and the system has been tested for transistor output powers at the fundamental frequency up to 5 W. When the power at the input of the multiplexer further increases, the losses caused by hysteresis and eddy currents on the ferrite inductors change the impedance at the fundamental frequency of 2 MHz. To overcome this issue, it is still in progress the evaluation of different technological solutions for the inductor L1.

Finally, to increase the coverage of the compensable area (see Figure 2.21d and Figure 2.22) of the band-pass filters, a capacitive trimmer with a higher maximum capacitance (i.e., 120 pF) can be used, while for the notch filters (see Figure 2.23) it is necessary to increase the inductance of the parallel cells. In this case, high-quality inductors must be used to guarantee the maximum resistances in Table 2.15.

2.6. Final Test

The bias tee, the LF multiplexer, and the LF tuner were used to characterize different transistors of different technologies and size during the PhD course. Here, an example for a GaN device with a total periphery of 1 mm is presented. Two different classes of operation at 2 MHz were synthesized, i.e., tuned-load class-AB and class-F [9,10], with the device biased at V_{DQ} = 30 V, I_{DQ} = 100 mA. Figure 2.29 shows the impedances at the fundamental frequency applied to the DUT by means of the designed tuner. The LF tuner and multiplexer have been calibrated as described in the previous paragraphs.

Thirteen real impedances between 30 Ω and 150 Ω have been synthesized as shown in Figures 2.26 and 2.28, respectively for the tuned load and class F configuration. The dispersion of the impedance seen at the fundamental frequency in Figures 2.29 and 2.31 is due to the increase of losses in the ferrite inductors (eddy currents and hysteresis power loss), while the dispersion of impedances at the harmonics in Figures 2.29 and 2.31 is caused by noise superimposed on the waveforms acquired.

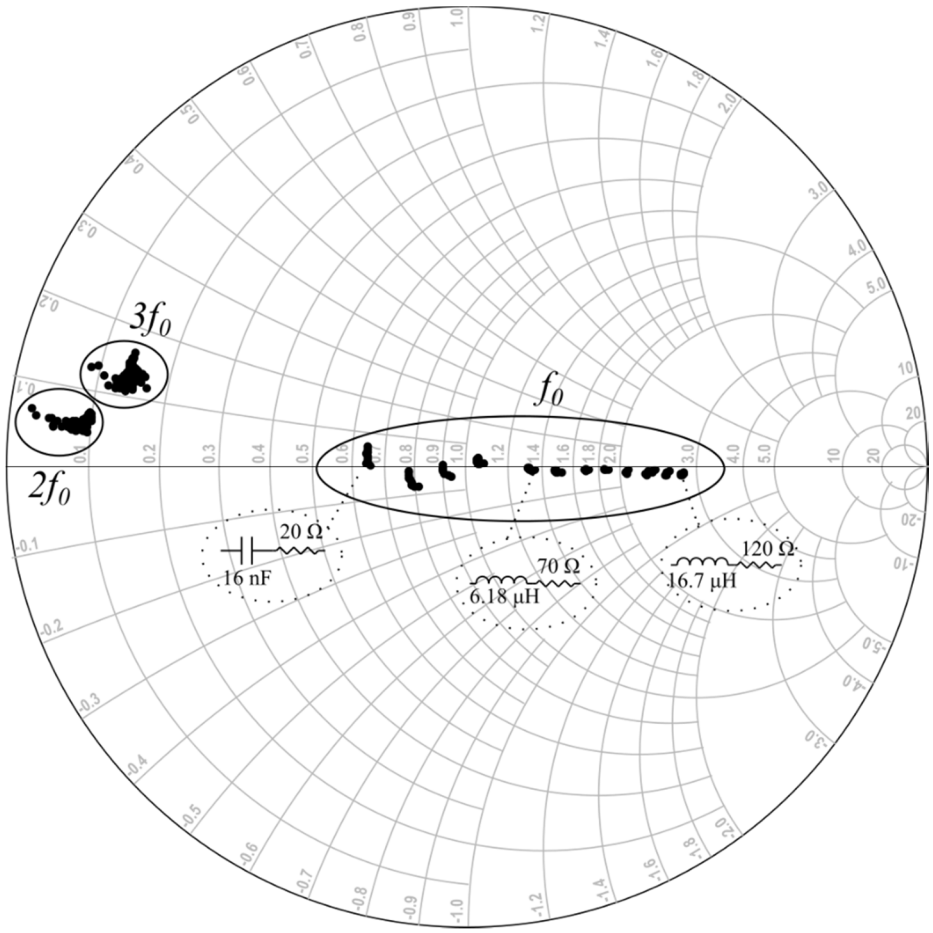


Figure 2.29 – Synthesized impedances at the fundamental frequency (2 MHz) and harmonics by varying the available input power (Pav) between -2.2 dBm and 17.7 dBm for the tuned load configuration. The dotted ellipses embrace some examples of tuner configurations.

Figures 2.30 and 2.32 show the output power and drain efficiency as a function of the synthesized real impedances for Pav = 17.7 dBm under tuned-load and class F operations.

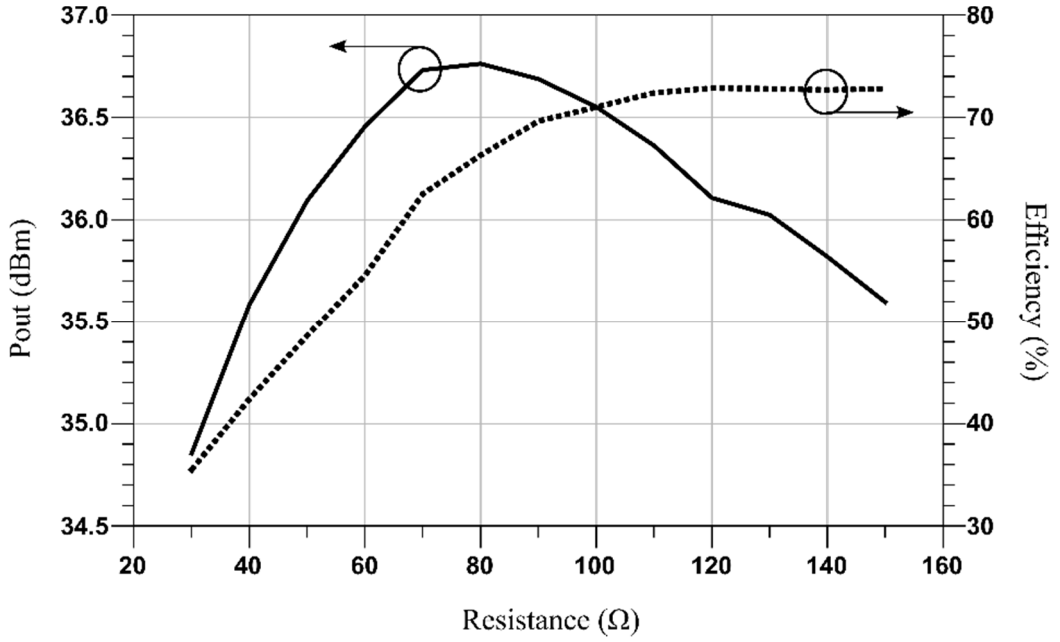


Figure 2.30 – Output power and drain efficiency for Pav = 17.7 dBm (tuned load).

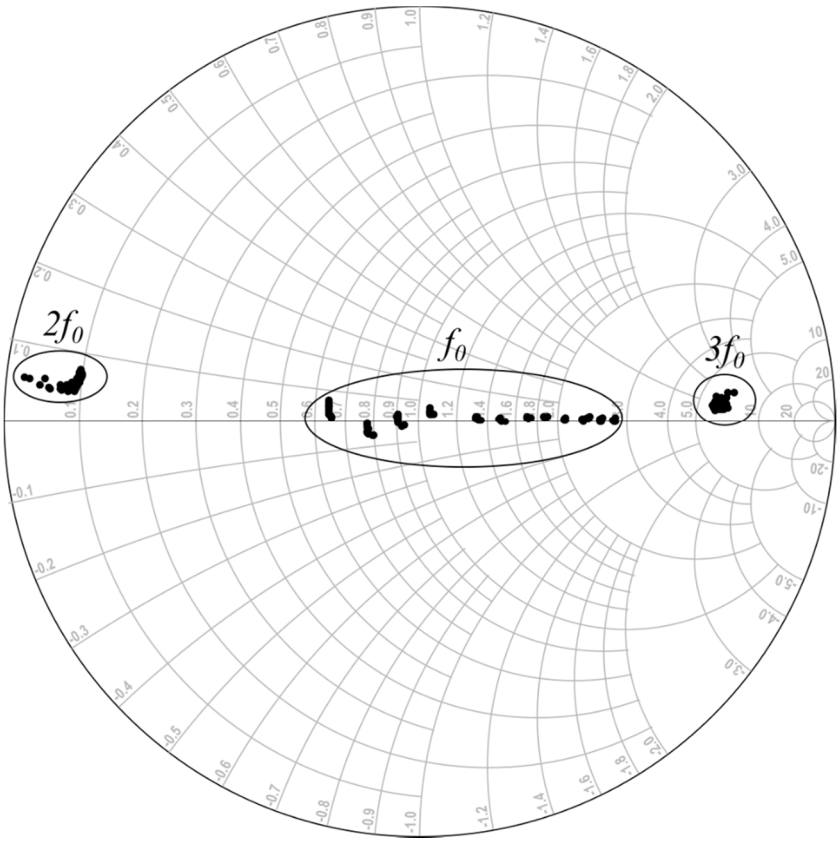


Figure 2.31 – Synthesized impedances at fundamental frequency (2MHz) and at the harmonics by varying the Pav between -2.2 dBm and 17.7 dBm for Class F operation. The dotted ellipses embrace some examples of tuner configurations.

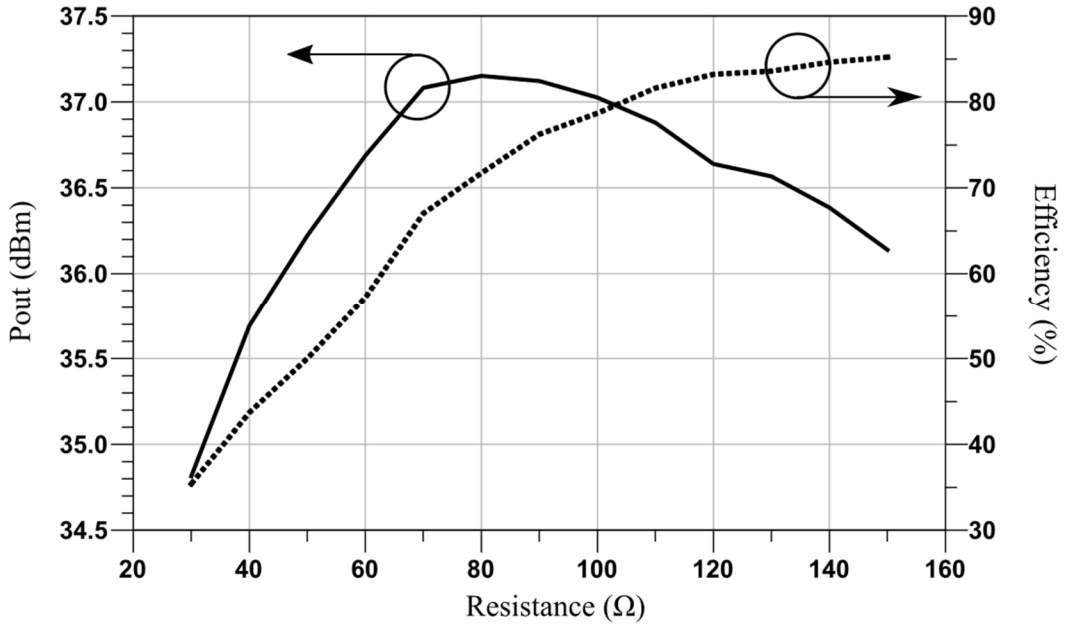


Figure 2.32 – Output power and drain efficiency for Pav = 17.7 dBm (class F).

Table 2.17 reports the performance for tuned-load and class F operation, with 95 Ω set at the fundamental frequency.

Class	Available Input Power	Output Power	Drain Efficiency	Load Condition
AB TL	17.7 dBm	36.5 dBm (4.5 W)	71%	92.7 – j1.5 Ω @ f0 4.4 + j2.9Ω @ 2f0 7.3 + j7.1 Ω @ 3f0
F		37 dBm (5 W)	78.7%	93.3 + j1.8 Ω @ f0 4.8 + j3.5 Ω @ 2f0 301 + j48.2 Ω @ 3f0

Table 2.17 – Comparison between measured tuned-load class-AB and class-F operation at low frequency.

In these measures, the branch of the multiplexer at frequencies > $3f_0$ was terminated on 50 Ω to prevent oscillations of the DUT. This termination resistance determines a deterioration of the quality factor of the parallel resonant cells, causing an impedance reduction at the third harmonic for class F compared to the case shown in Table 2.17. Nevertheless, using a more accurate tuning the impedance at $2f_0$ and $3f_0$ could be accurately placed on the real axis of Smith chart.

The bias tee, tuner and multiplexer realized for the LF load-pull system, allow the transistor characterization in different operating classes. The synthesis of loads at the fundamental frequency and the harmonics is simpler and faster compared to the active load-pull system (20 minutes respect to 3 hours for ten impedances and ten power levels). In fact, in the active system the impedance strongly depends on the device output power level, i.e., the reflected waveform to be synthesized by the function generator varies with the power. Finally, the designed measurement system guarantees excellent performance in terms of impedance stability and power handling capability.

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Chapter 3

LDMOS Power Amplifier Design Based on the Waveform Engineering

3.1. Introduction

Power management is one of the most critical issues in modern electronic systems. Besides reducing the energy costs, an efficiency-oriented design translates itself into a simplified cooling system, a better component reliability, and therefore, a reduction of the maintenance costs.

In the majority of electronic apparatuses, the electronic elements that draw the greatest part of the energy are the Power Amplifiers (PAs). Today, their impact on the overall energy consumption of an electronic system is of paramount importance for any kind of application, like audio [1], [2], medical [3], Radiofrequency (RF) [4], [5], and so on.

The use of operating classes based on a reduced conduction angle (e.g., class B and C) surely improves the efficiency, at the price of detriment of other important parameters, such as linearity and power gain [6], [7] as well as transistor ratings and size. Thus, new classes of operation [6]-[10] have been developed to increase the PA efficiency. They are mainly based on tuning the transistor harmonic terminations to shape the transistor waveforms and get two theoretical requirements:

- No overlap between the output current and voltage waveforms to reduce the power dissipated on the active device.
- No active power delivered at the harmonic frequencies.

If these conditions are both satisfied, a theoretical 100%-efficiency is achievable [7]. As an example, the switching class-E power amplifier is a very common choice for PA operating in the megahertz range, whereas for application at RF and microwaves, class-J [11] and class-F [12] operations are largely diffused together with some architectural implementations oriented to furtherly improve the efficiency [5], [13].

On the other hand, increasing the efficiency by harmonic manipulation typically implies conditions that may be harmful for the transistor reliability, in particular for the

high electric fields induced by the peaks of the voltage waveforms [14], that have to be properly controlled to avoid any premature failure of the active devices [15-17].

Another drawback is related to the frequency selectivity of the matching networks, which is necessary when harmonic terminations need to be controlled. In Table 3.1, some examples of state-of-art PAs are reported. It is clear that for harmonically-tuned amplifiers, the efficiency becomes lower with respect to the theoretical values as larger design bandwidths are considered [18] because of the physical limitations of implementing the harmonic terminations over a wide range of frequencies. When broadband operation is required, the use of a reduced conduction angle condition (e.g., class-AB) may be more convenient since tuning the matching networks only at the fundamental frequency reduces the complexity of the circuit, ensuring the desired performance over a larger bandwidth.

Year	Technology	Class of operation	Fractional Bandwidth	Output Power	Efficiency
2013 [18]	GaN HEMT	AB	58%	100 W	51÷61%
2014 [19]	LDMOS	E	24%	6.5 W	> 60%
2014 [20]	GaN HEMT	F	0%	7.7 W	80.2%
2015 [21]	LDMOS	E	20%	> 70 W	82%
2016 [22]	GaN HEMT	AB	27%	4.9 W	68% (PAE)
2016 [23]	GaN HEMT	F	62%	9÷11 W	> 60%
2017 [24]	GaN HEMT	J	30%	4÷4.7 W	40÷50% (PAE)
2017 [25]	LDMOS	F^{-1}	62%	6.3÷10 W	73÷79%
This work	LDMOS	AB	20%	10 W	55÷63%
		F	0%	8 W	76%

Table 3.1 – State-of-the-art power amplifiers.

From a theoretical point of view, the waveforms at the input and output ports of the transistor in a PA are defined by considering the active device either as a switch (e.g., class-E) or, more generally, as a controlled current generator. Indeed, this is a strong simplification, because in an actual device, nonlinear intrinsic capacitances and linear parasitic effects alter the ideal device behavior and, as a consequence, hide the transistor reference plane where the proper waveforms should be implemented. Designers can deal with these effects by using some simplified models. As an example, for a class-E design, the capacitive behavior of the output port is typically modeled as either a linear or a nonlinear capacitor [15], [16], [21], according to the required level of accuracy.

In this chapter, the general methodology described in Paragraph 1.3 will be used for the design of laterally-diffused metal-oxide-semiconductor (LDMOS) field-effect transistor (FET) PAs, which exploits the waveforms measured at the current-generator plane as the

starting point. In particular, dynamic low-frequency (LF) measurements performed by means of the LF setup described in Paragraph 2.2 are used to describe the resistive core, while the capacitive core and the parasitic network are modeled starting from small-signal measurements. As discussed in Chapter 1, by using a model of the device parasitic extrinsic network, we can embed their contributions and get the proper terminations at the actual device terminals. This technique is referred as *nonlinear embedding* [26], since in the most general case such models are nonlinear. Although already presented within the framework of microwave applications, this methodology can be extended to different classes of devices and applications (i.e., LDMOS PA's for FM broadcasting systems), showing how it can be successfully adopted also in the field of power electronics.

With respect to conventional approaches, nonlinear embedding does not require extensive, time-consuming load/source-pull measurements or simulations for identifying the device optimum operating condition. This is due to the fact that the optimum condition, that is univocally defined by the power-amplifier design theory for each class of operation [7], represents the starting point of the nonlinear-embedding approach. We will use this approach for the design of two different PAs oriented to FM broadcasting systems. The first PA is targeted to operate under a high-efficiency condition by using harmonic manipulation. The design of the second PA is targeted to achieve a wideband performance. Both design examples put in evidence the capabilities of the nonlinear-embedding methodology. We will also compare this design approach with conventional ones which exploit a simplified linear model of the intrinsic capacitances showing how the nonlinear-embedding methodology allows more accurate results.

3.2. Transistor Model

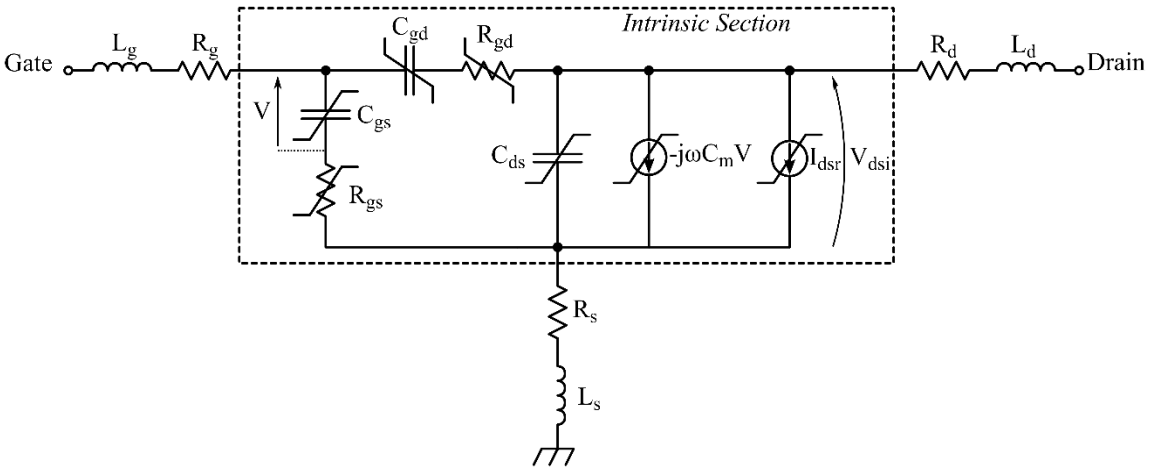


Figure 3.1 – Nonlinear model topology implemented for the LDMOS.

Figure 3.1 shows the topology of the nonlinear model of the LDMOS transistor. The extrinsic and intrinsic elements (see Paragraph 1.3) can be identified by means of appropriate measures on the DUT. The extrinsic elements represent the parasitic elements of the device, package and bonding and are considered linear and they are typically extracted by measuring the S parameters of the device under cold-FET operation.

The main element of the intrinsic core is the current generator that models the static (DC) and dynamic (I/V) characteristics of the device. The current generator model can be identified from LFLS measurement setup described in Paragraph 2.1, while the remaining elements describe the nonlinear dynamic effects of the transistor as discussed in the Paragraph 1.3. The capacitive core consists of the elements C_{gs}, C_{gs}, R_{gd}, R_{gs}, C_{ds} and C_m that can be obtained from multi-bias small-signal measurements [40].

3.3. Design of Two Power LDMOS Amplifiers

We will now discuss the design of two PAs by means of the nonlinear-embedding approach. Both of them are based on the 10-W LDMOS MRF6V2010N by Freescale, which can operate within the band 10 ÷ 450 MHz, covering the FM broadcasting band we are interested to, i.e., 88 ÷ 108 MHz.

The aim of the two designs is to point out the capabilities of the nonlinear-embedding methodology, by selecting two different operating conditions. For the first PA, we focused on the maximization of its efficiency, keeping the output power at a sufficiently high level under continuous-wave regime. In this case, tuning the load only at the fundamental frequency is not sufficient, and we needed to properly control also the harmonics [17], [27]. Such a kind of evaluation may be easily performed by exploiting the active load-pull setup shown in Figure 3.1a and described in Paragraph 2.2. The characterization of the device has been performed in an active manner by imposing the load terminations at the fundamental frequency and the harmonics (only for class F). Indeed, the AFG (Tektronix - AFG3252) allows the control of the harmonic components of the signals injected at the DUT ports. As previously discussed, harmonic tuning tends to limit the PA bandwidth because of the selectivity required for the matching networks. Therefore, as a second design, we considered a wideband PA. In this case, only the load impedance at the fundamental frequency is tuned and the nonlinear-embedding approach will be used to derive the transistor terminations within the whole FM broadcasting band.

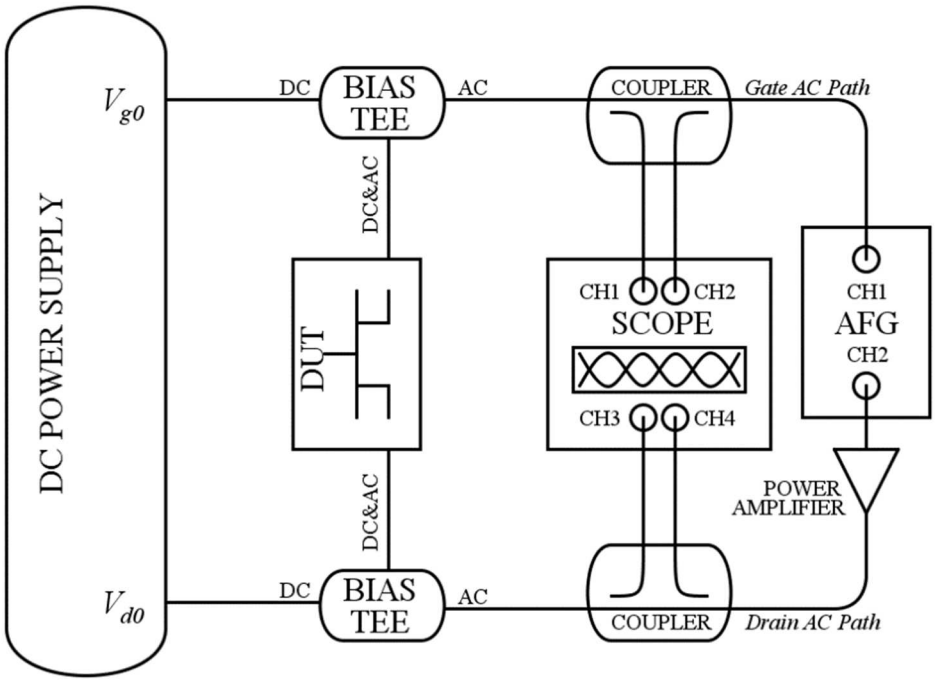
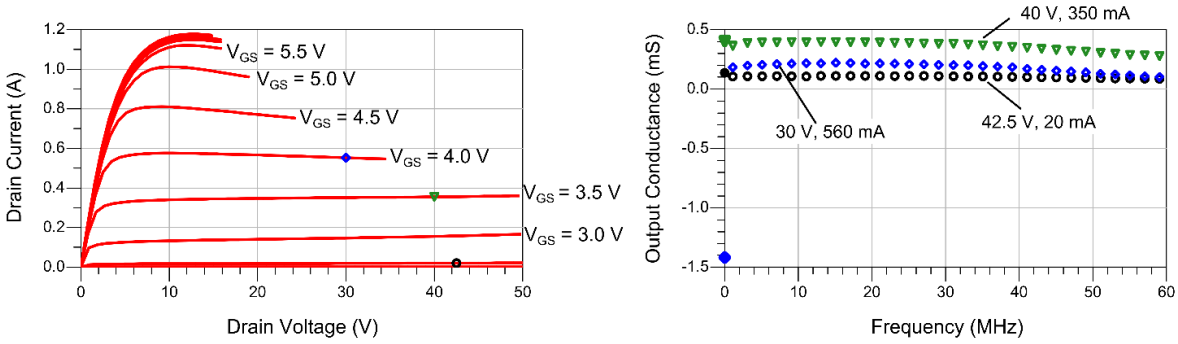


Figure 3.1a – Block diagram of the low-frequency measurement setup implementing the time-domain active load-pull system.

To connect the transistor to the setup, we mounted it on a customized PCB board fabricated on a Diclad 527 substrate (Figure 3.2). The device gate and drain flanges are soldered to two 50-Ω microstrip lines reaching the external SMA connectors. The characteristics of the lines have been designed to have negligible influence at LF (i.e., 2 MHz). In our experience, the frequency used for the large-signal characterization of the LDMOS was sufficiently high to get the behaviour of the current generator consistent with RF operation. Figure 3.1b shows the DC I/V characteristics, while Figure 3.1c reports the output conductance derived from the LDMOS S-parameters for different bias points as a function of frequency and the corresponding values derived directly from DC I/V measurements. It is well evident the different device behaviour under DC and dynamic operation due to the device self-heating. The output conductance remains practically constant in the bandwidth $1 \div 30$ MHz, above which it starts decreasing because of the device reactive effects. We carried out the low-frequency characterization at 2 MHz, so that the acquired large-signal data exploited for the nonlinear embedding lie where the device behaves consistently with RF operation, although the reactive effects are not yet noticeable.

The fact that the measurements on the fabricated PAs are consistent with the low-frequency data proves the validity of the characterization at 2 MHz.



(b) (c)

Figure 3.1 – DC I/V characteristics (b) and small-signal output conductance (c) of the LDMOS as a function of frequency for three bias points indicated on the left: V_{DS} = 42.5 V and I_D = 20 mA (circles), V_{DS} = 40 V and I_D = 350 mA (triangles), V_{DS} = 30 V and I_D =560 mA (diamonds). The filled symbols represent the values derived directly from DC I/V measurements.

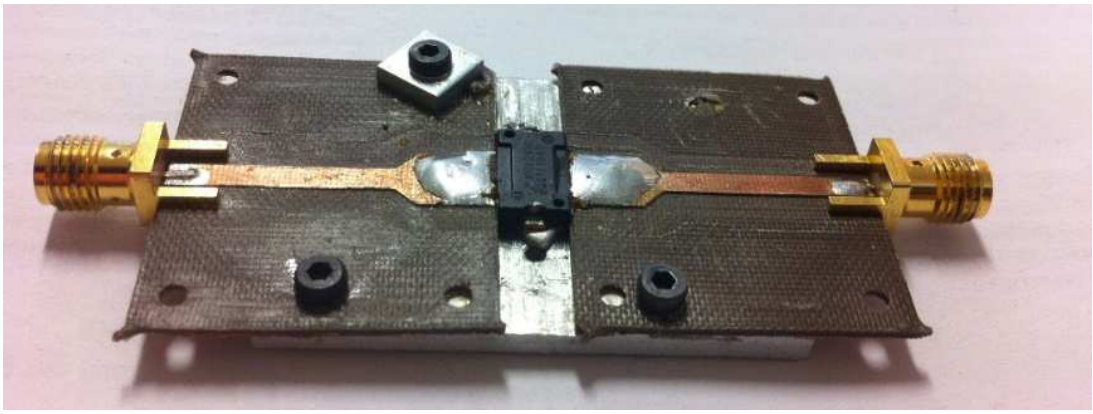


Figure 3.2 – LDMOS transistor mounted on the PCB board for the low-frequency characterization.

The transistor was preliminarily characterized by means of DC I/V conventional measurements for evaluating the best operating point for the device and a first estimation of its performance. Once the bias point was selected, i.e., V_{g0} = 2.4 V, V_{d0} = 42.5 V, I_{d0} = 20 mA, we identified the load lines corresponding to the two operations of interest, which are reported in Figures 3.3 and 3.4, together with the output waveforms. The high-efficiency load line (Fig. 3.3a) was obtained by actively synthesizing the load impedances reported in Table 3.3. They realize a class-F operation, which allows a higher output power than other conventional classes of operation with a reduced conduction angle (e.g., class C). In particular, with this load line, we achieved an RF output power of 8.5 W with a drain efficiency of 86.7%. By looking at the measured waveforms in Fig. 3.2, we can see that their shapes are consistent with the theoretical ones, i.e., a square wave for the voltage and a half-truncated sinusoid for the current, with a minimum superposition. In addition, we can easily monitor if the selected dynamic condition may affect the transistor reliability by comparing the data with the device maximum ratings. As an example, the maximum

drain voltage allowed for this device is 110 V, whereas the load line highlights a maximum dynamic value of approximately 88 V, which is sufficiently low to avoid any reliability issue.

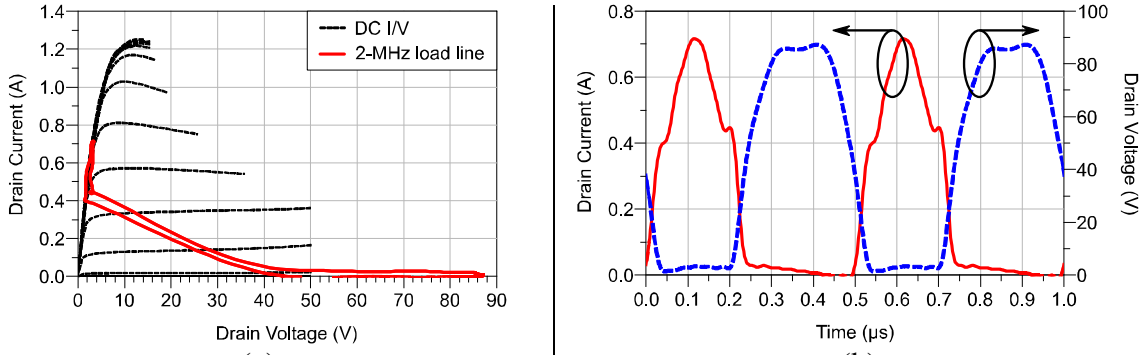
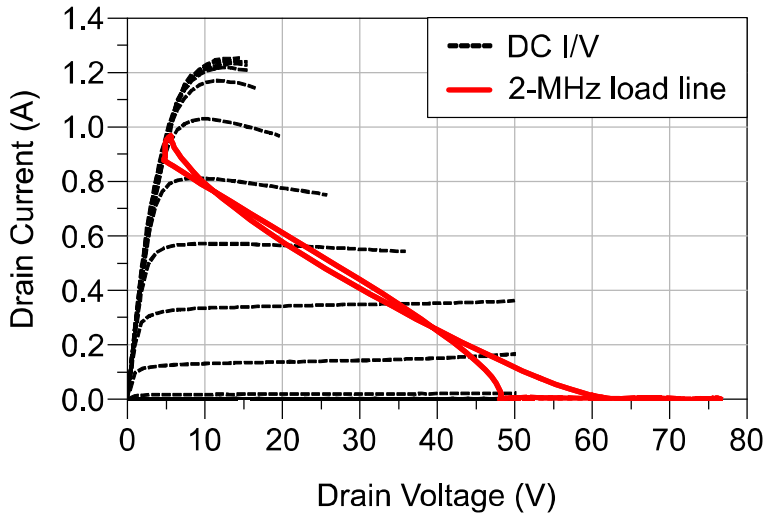


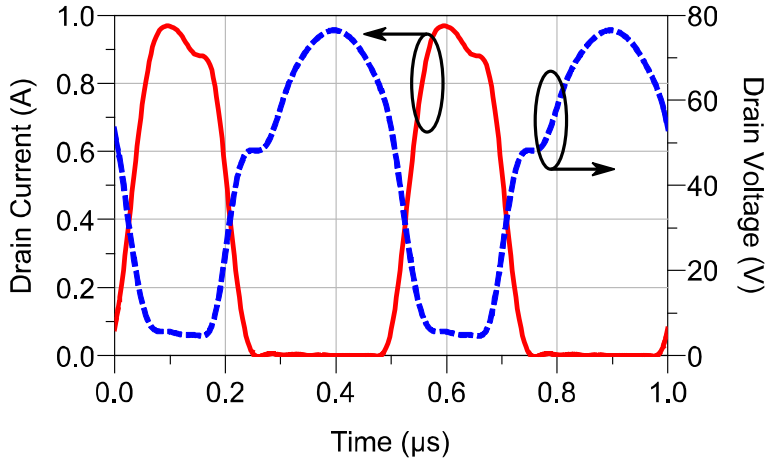
Figure 3.3 – High-efficiency class-F load line synthesized at 2 MHz superimposed to the DC I/V characteristics (a) and corresponding waveforms (b).

The class-AB load line and the corresponding waveforms are shown in Figure 3.4. As reported in Table 3.2, the impedances at harmonics were not set, focusing only on the fundamental one. Nevertheless, their values were controlled in order to keep them sufficiently low, avoiding a strong influence on the PA performance. The measured performance in this case was 9.4 W with a drain efficiency of 68.2%, which is consistent with the selected class of operation. It is also evident that the absence of harmonic tuning keeps the maximum value of the drain voltage lower than the class-F load line.

To apply the nonlinear-embedding procedure, we first need a model of both the intrinsic capacitances and the extrinsic parasitic elements. In this particular case, we identified these models from multi-bias S-parameter measurements [29], [30]. The parasitic network has been identified by means of cold-FET data using a conventional approach [31]. Then, by de-embedding the parasitic effects from the S-parameters, the intrinsic capacitive network can be easily determined and implemented as a look-up-table model for direct nonlinear simulations [28], [31]. Indeed, the use of a customized model is not mandatory. Alternative solutions, such as the use of foundry models, could be adopted, provided that the description of the intrinsic capacitances and the extrinsic parasitic elements are available.



(a)



(b)

Figure 3.4 – Class-AB load line synthesized at 2 MHz superimposed to the DC I/V characteristics (a) and corresponding waveforms (b).

Frequency	Class-F Load Impedance	Class-AB Load Impedance
2 MHz	145.6 + j6.5 Ω	73 – j10 Ω
4 MHz	0 + j6.2 Ω	30 + j17 Ω
6 MHz	1.3 + j*1.0 kΩ	39 + j26 Ω

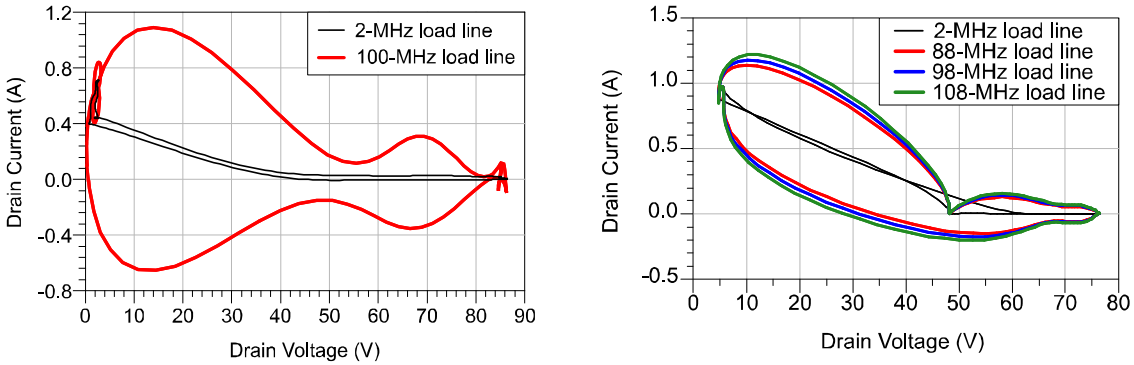
Table 3.2 – Load impedances corresponding to the low-frequency load lines.

Frequency	Load Impedances	Source Impedances
100 MHz	77.8 + j71.1 Ω	9.1 + j72.6 Ω
200 MHz	j2.0 Ω	-j2.1 Ω
300 MHz	j59.7 Ω	j1.8 Ω

Table 3.3 – Load/Source Impedances at the Design Frequency for the Class-F Load Line.

Frequency	Load Impedances	Source Impedances
88 MHz	69.7 + j17.5 Ω	14.1 + j94.5 Ω
98 MHz	68.2 + j20.1 Ω	13.7 + j84.8 Ω
108 MHz	66.5 + j22.5 Ω	13.3 + j76.9 Ω

Table 3.4 – Load/Source Impedances at the Design Frequencies for the Class-AB Load Line.



(a) (b)

Figure 3.5 – Low-frequency load lines (thin lines) and predicted load lines at design frequency (thick lines) for the high-efficiency class-F (a) and the wideband class-AB (b) conditions.

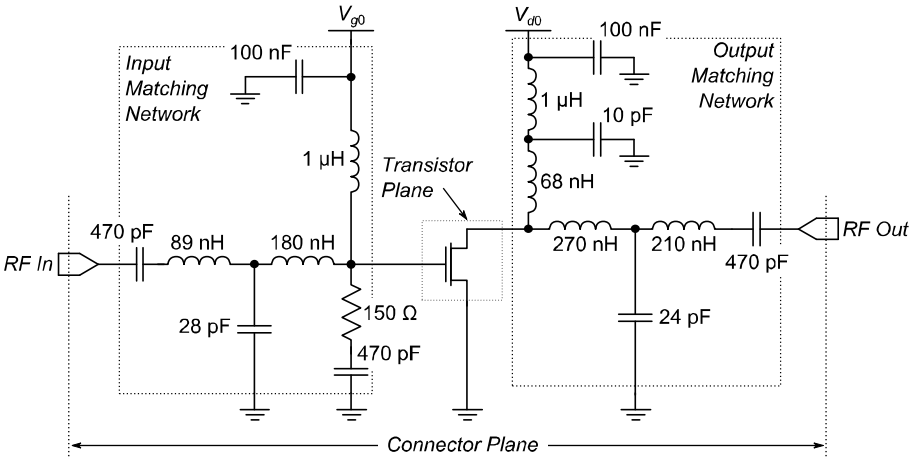
As a next step, we transposed the LF load lines of the two classes of operation, to the design frequency by exploiting the nonlinear-embedding procedure. For the high-efficiency class-F condition, we considered a design frequency of 100 MHz. In Table 3.3 we report the load and source impedances predicted by the nonlinear-embedding methodology and used for the synthesis of the PA matching networks. Since harmonic tuning was performed, we list the first three harmonics.

Regarding the class-AB load line, we applied the nonlinear embedding from 88 MHz to 108 MHz to get the design data for a wideband PA. For the sake of brevity, we report in Table 3.4 the source and load impedances just at the edges and at the center of the selected FM bandwidth.

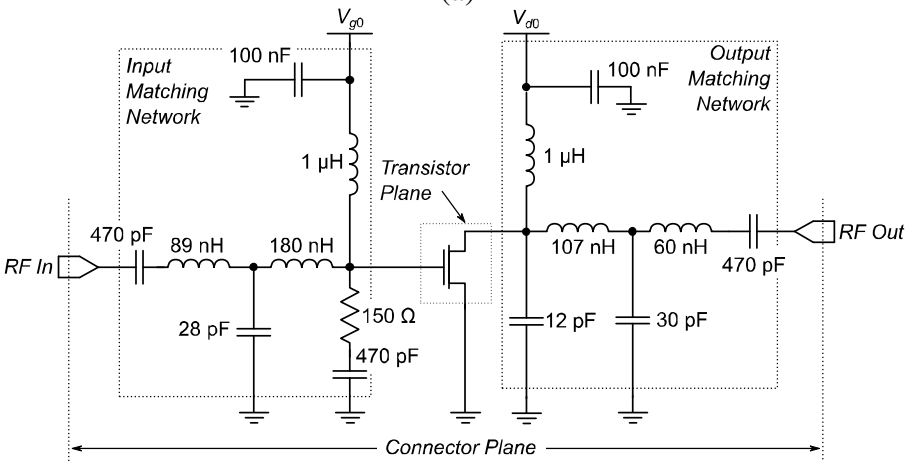
In Figure 3.5 the predictions of the load lines at the extrinsic plane compared with the measurements at the current-generator plane are reported. It is evident how the latter are masked by the contributions of the reactive elements of the device. In Figure 3.5b, it is also evident a slight variation of the extrinsic load lines with frequency, which reflects the values of the load impedances reported in Table 3.4.

3.4. Power Amplifier Fabrication

Figure 3.6 reports the schematics implemented for the fabrication of the PAs, where the matching and bias networks have been designed to synthesize the impedances derived from the nonlinear-embedding procedure.



(a)



(b)

Figure 3.6 – Schematics of the class-F (a) and class-AB (b) fabricated PAs with the indication of the connector and transistor planes.

The output-matching networks are quite complex in both cases, although for different reasons: the need for harmonic control in the high-efficiency class-F PA and the wideband requirement for the class-AB PA.

Regarding the input network, the R-C shunt has been introduced for stability issues in both cases. Moreover, to guarantee adequate matching also under small-signal operation, it is realized a trade-off between the source impedance values in Tables 3.3 and 3.4 and the ones, derived from S-parameter measurements at the selected bias point, that maximize the small-signal matching over the bandwidth 88 ÷ 108 MHz. The same L-C-L network was sufficient to get good performance over the required bandwidth in both the PAs, as will be shown in the following.

The circuits were fabricated on a conventional FR-4 substrate, and are shown in Figure 3.7.

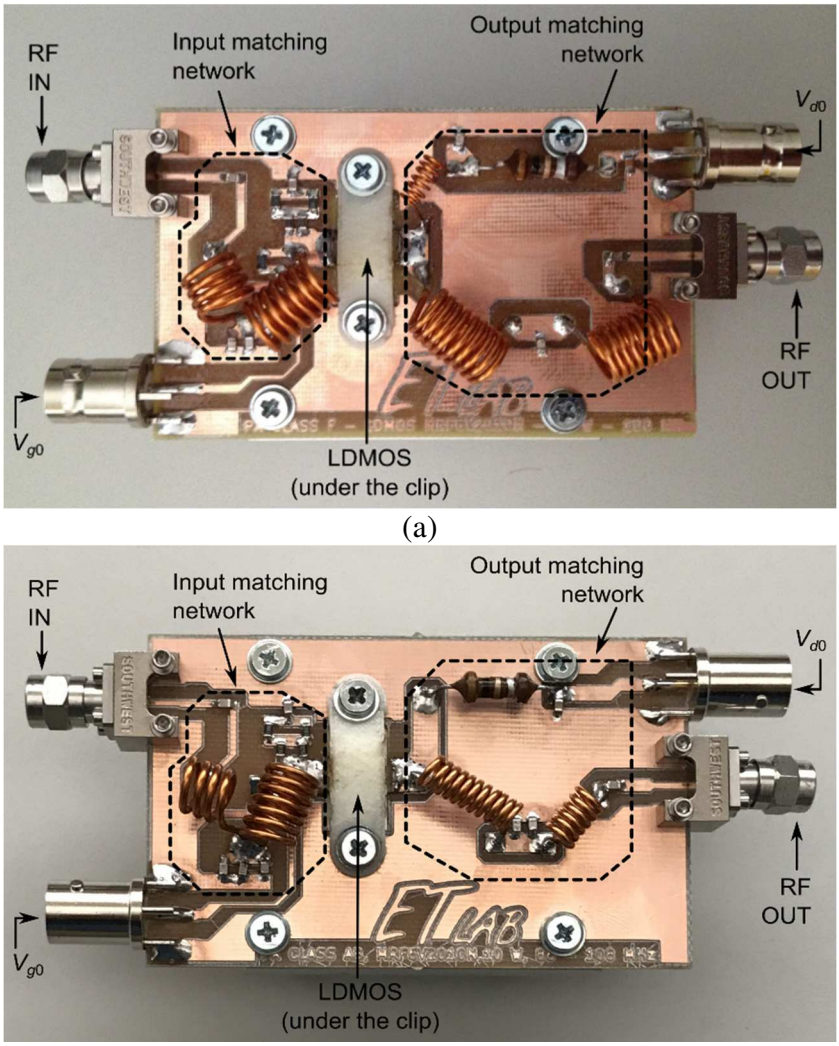


Figure 3.7 – Photos of the fabricated PAs: class F (a) and class AB (b).

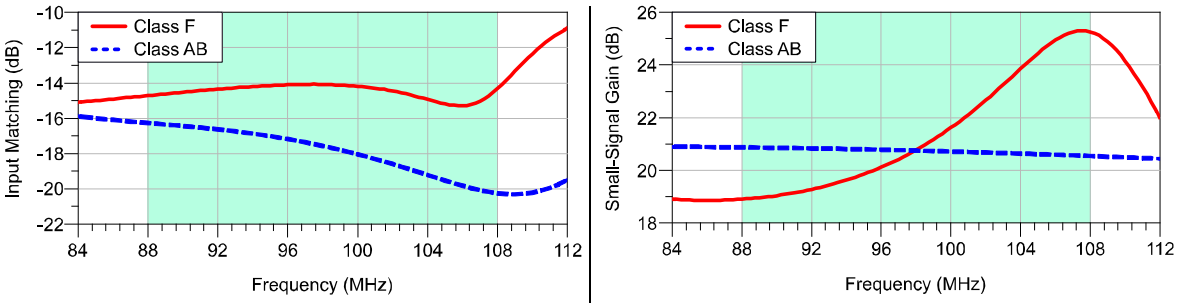
3.5. Power Amplifier Validation

3.4.1. Small-Signal Verification

We first measured first the small-signal behavior of the PAs for their nominal bias point, i.e., V_{g0} = 2.4 V, V_{d0} = 42.5 V, by using a vector network analyzer. The results in terms of input matching and small-signal gain are shown in Figure 3.8. In the bandwidth for which the input matching network was designed, we obtained an input matching better than -14 dB and -16 dB for the class-F and the class-AB PAs respectively.

The small-signal gain of the class-F PA shows a large variability in frequency related to the selectivity of the output-matching network. We expected the peak gain not necessarily lying at the design frequency, since no specification has been considered for

this parameter in the design phase, giving priority to the output power and efficiency under large-signal operation. On the contrary, the class-AB amplifier, for which the matching networks were optimized within the whole FM bandwidth, has an approximately flat gain, with a variability limited to 0.5 dB.



(a) (b)

Figure 3.8 – Input matching (a) and small-signal gain (b) of the fabricated PAs. The shaded areas highlight the bandwidth 88 ÷ 108 MHz.

3.4.2. Large-Signal Measurements

The next step was to verify the PAs performance under actual operation, i.e., large-signal conditions. To this aim, we exploited a simplified version of the setup described in Paragraph 2.2, removing the bias-tees (which are included in the fabricated PAs) and terminating the output port on a constant 50-Ω load.

We first measured the PAs performance for a constant level of input power over the bandwidth 88 ÷ 108 MHz. The results are reported in Figure 3.9. The class-F PA achieves a maximum output power for 100 MHz, whereas the maximum efficiency is reached at 105 MHz. The class-AB PA performance is instead more constant over frequency, consistently with its wideband design. As expected from this class of operation and for the selected design condition, it delivers more power with a lower efficiency.

In both cases the performance is lower than the designed one. This is indeed an expected result since the measurements include the losses of the matching networks, which lower the overall efficiency. On the contrary, the design data are referred to the transistor extrinsic reference plane. Therefore, for a fair comparison, we measured the S-parameters of the fabricated matching networks to shift the large-signal data at the transistor plane (see Fig. 3.6).

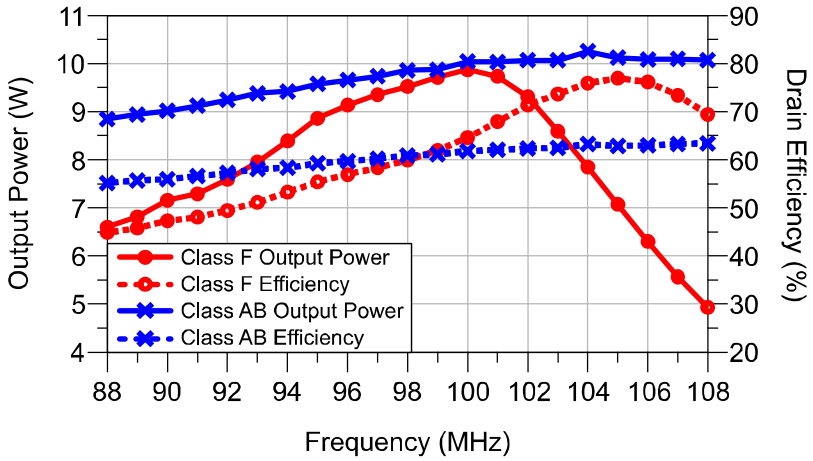


Figure 3.9 – Measured output power (solid red line) and drain efficiency (dotted blue line) for an input power of 14.4 dBm (class F) and 16.9 dBm (class AB) over the bandwidth 88 ÷ 108 MHz. Data refers to the connector plane (Figure 3.6).

The S-parameters of the class-F output-matching-network showed a frequency shift with respect to the designed network due to fabrication issues, so that the best match with the theoretical load impedances is achieved at 104 MHz. The best performance at the transistor plane is reported in Table 3.5 compared with the prediction of the nonlinear-embedding procedure. The good agreement suggests the transistor is operating with the same load line we have measured at LF at the current-generator plane. In Figure 3.10, we show the corresponding performance as a function of the input power. Here, the input power is defined on different planes, therefore eliminating the contributions of the matching networks, we move the dotted lines to the right and to the top. In fact, for higher input power we have more drain efficiency and more output power at the transistor extrinsic plane (solid lines in Figure 3.10).

It is also significant to observe the spectrum of the output power to monitor the harmonic distortion. Figure 3.11 shows the harmonic-to-fundamental output-power ratio for a fundamental frequency of 104 MHz as a function of the input power. The second harmonic is practically absent in the output spectrum, whereas there is a small third-harmonic component, which becomes evident only for the higher levels of power. This result is indeed consistent, since one of the aims of the class-F operation is to minimize the output power at harmonics to improve the PA efficiency.

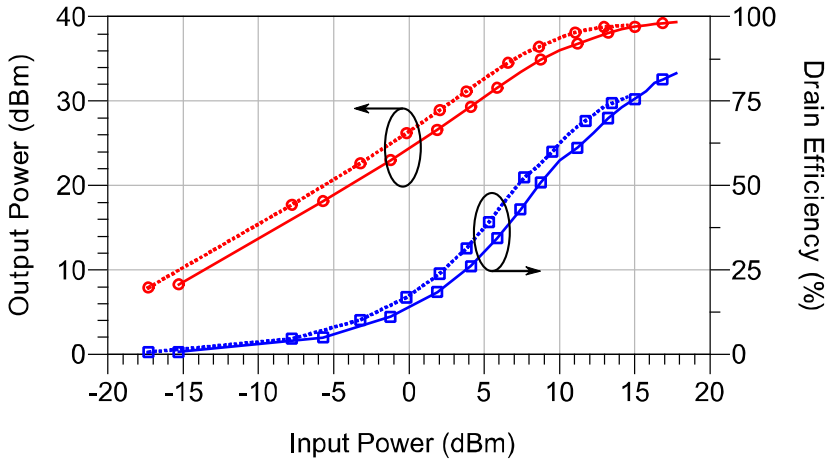


Figure 3.10 – Output power (red circled lines) and drain efficiency (blue squared lines) at 104 MHz. Solid lines refer to the transistor input and output extrinsic planes, dotted lines to the PA input and output connector planes.

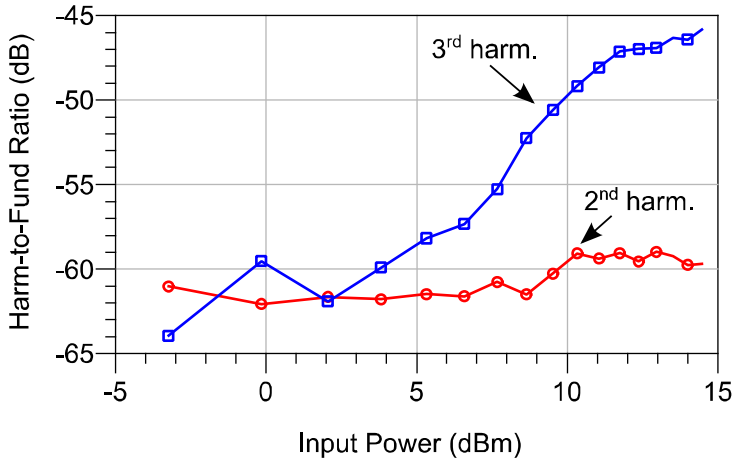


Figure 3.11 – Harmonic-to-fundamental output-power ratio for a fundamental frequency of 104 MHz.

Nonlinear Embedding	Performance	High-Frequency Measurement
8.5 W	Output Power	8.6 W
86.7%	Drain Efficiency	83.2%

Table 3.5 – Predicted and Measured Transistor Performance at 104 MHz.

In the same way, we shifted the measured data at the transistor reference plane for the class-AB PA. In Figure 3.12 the results over the FM bandwidth for a constant input power (i.e., 50 mW) are reported. The achieved performance is slightly lower than the expected one in terms of efficiency. The analysis of the output-matching-network S-parameters showed that the terminations at harmonics presented at the DUT plane, which were not controlled, were higher than expected, causing a slight detrimental effect on the PA efficiency.

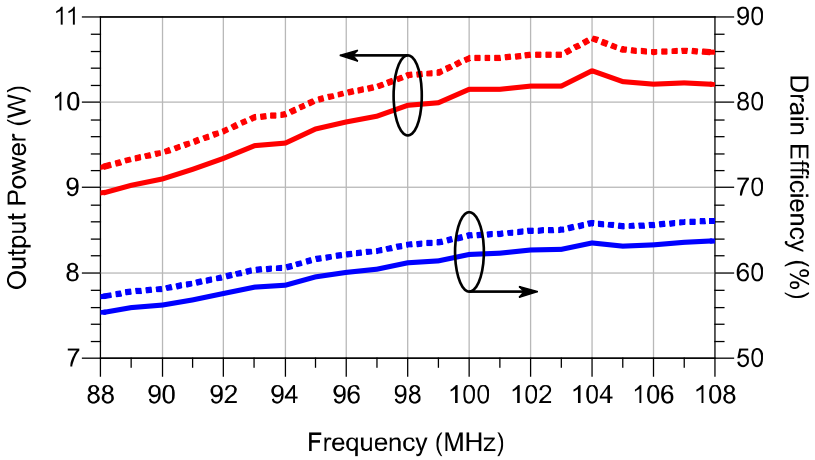


Figure 3.12 – Output power and drain efficiency for the class-AB PA for an input power of 17 dBm (50 mW). Dotted lines refer to the transistor extrinsic plane, solid lines to the PA connector plane.

3.4.1. Validation and Comparison with Conventional Design Approaches

As shown so far, the nonlinear-embedding methodology transposes the current-generator waveforms to the extrinsic plane by considering a full nonlinear model of the intrinsic capacitances and a complete linear parasitic network. This surely makes it more complicated than conventional but less accurate approaches usually based on a simplified linear approximation of the transistor nonidealities, can lead, as a consequence, to less accurate results. To provide some comparison, we applied two "linear" embedding procedures [32] starting from the class-F and class-AB load lines at the current-generator plane. For the first case (A), we only considered two linear capacitances, C_{gs} and C_{ds}, as the capacitive core and no parasitic elements have been included to transpose the data at the extrinsic plane. For the second case (B), we also included the effects of the parasitic elements and the linear capacitance C_{gd}. In case A there is no feedback element between the input and output ports of the device. Such a practical hypothesis is commonly adopted [15],[19]-[21],[24] since it strongly simplifies the evaluation of the extrinsic load impedances, by reversely isolating the two ports of the device. In case B we introduced the capacitance C_{gd} as a feedback element, in order to show that the limited accuracy is largely ascribable to the linearity hyphothesis.

Class of Operation	Frequency	Linear Embedding A	Linear Embedding B	Nonlinear Embedding
Class F	100 MHz 200 MHz 300 MHz	105 + j67 Ω j6.5 Ω 3.2 + j79.7	103 + j67.3 Ω j6.1 Ω 0.9 + j79.1	77.8 + j71.1 Ω j2.0 Ω j59.7 Ω
Class AB	100 MHz	74.3 + j13.2 Ω	72.0 + j13.0 Ω	67.9 + j20.6 Ω

Table 3.6 – Load impedances predicted by linear and nonlinear embedding approaches for at 100 MHz.

In Table 3.6, we report results of the impedances predicted by the linear approaches in comparison with the nonlinear one. The data provided by the linear approaches are very similar, which confirms the small influence of the parasitic network and of the feedback capacitance C_{gd}. On the contrary, compared with the nonlinear embedding, we note a considerable difference, especially for the class-F condition, where the effects of the capacitance nonlinearities is more noticeable and strongly influence the transistor operation.

To furtherly confirm the validity of the nonlinear-embedding procedure, we characterized the transistor performance at the design frequency. Starting from the impedances derived at design frequency (see Tables 3.3 and 3.4), we can directly synthesize them at the extrinsic plane by means of a time-domain load-pull setup based on a 4-channel 50-GHz oscilloscope [33], and compare the measured time-domain waveforms with the ones predicted by the nonlinear embedding. This comparison becomes very interesting for the class-F operation, since it involves some harmonic tuning up to the third harmonic. We report the results for a design frequency of 100 MHz in Figure 13. The main difference between predicted and measured waves is related to the limitation of synthesizing harmonic terminations with a theoretically zero real part, which increases the magnitude of the harmonics with respect to the ideal case. Despite this aspect, the agreement is very good and proves the accuracy of the predicted results.

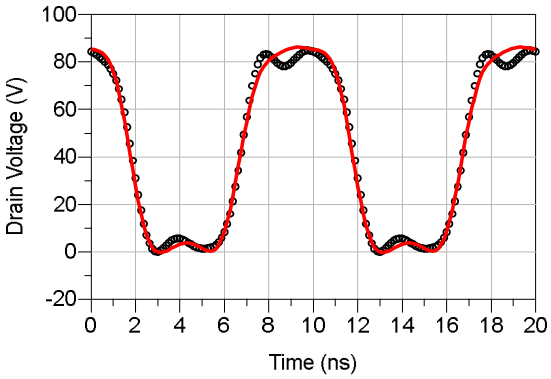


Figure 3.13a – Drain voltage waveforms at the transistor EP for the class-F PA measured at 100 MHz for an input power of 14.5 dBm (28 mW): expected waveforms derived by the nonlinear embedding (solid lines) and measured waveforms (symbols).

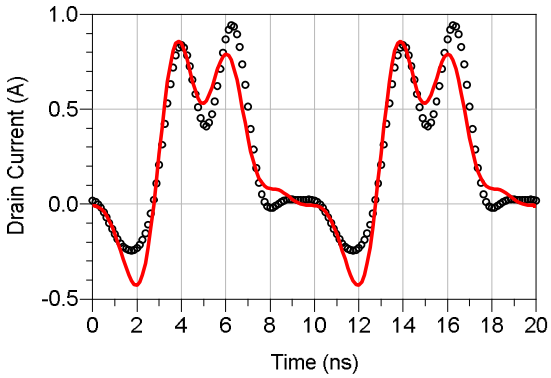


Figure 3.13b – Drain current waveforms at the transistor EP for the class-F PA measured at 100 MHz for an input power of 14.5 dBm (28 mW): expected waveforms derived by the nonlinear embedding (solid lines) and measured waveforms (symbols).

3.4.2. FM Signals

The PAs is also tested with FM modulated signals. Figure 3.14 shows the input and output spectra for a frequency-modulated signal, with a carrier frequency of 102 MHz and a modulating sinusoidal waveform at 1 kHz. The frequency deviation is 75 kHz, which is a typical value for FM broadcasting transmissions. A comparison between the performance of the fabricated PAs at 102 MHz is reported in Table 3.7.

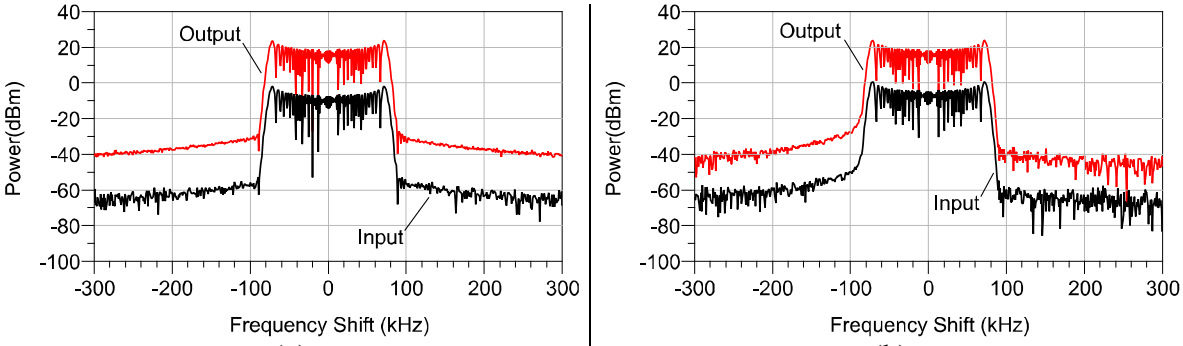


Figure 3.14 – Spectra of the input (black) and output (red) power for an FM signal for the class-F (a) and the class-AB PA (b). The total output power is 9.4 W in both cases.

Class of Operation	Drain Efficiency
F	71.3%
AB	61.2%

Table 3.7 – PAs Performance for FM Modulated Signals at 9.4-W Output Power.

3.6. Conclusion

The nonlinear-embedding technique [26] has been applied as a general approach for the design of LDMOS PAs. In particular, the capabilities of the LF measurement setup dealt with in Chapter 2, have been exploited to describe the resistive core behavior of the LDMOS transistor. Two PAs, operating in the FM broadcasting band, were designed and realized. In particular, high-efficiency class-F and wideband class-AB operations were considered. The performance of the fabricated PAs shows a very good agreement with design predictions, proving the effectiveness of the proposed design technique and paving the way for further development of the nonlinear-embedding approach oriented to LDMOS technology.

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Conclusion

In this thesis, the design of electronic components for the efficient implementation of a passive low-frequency load-pull system has been described. Starting from the study of the load-pull systems present in the literature, the characteristics of a *new* passive system have been identified. The system consists of a tuner, a multiplexer and a power bias tee realized to work at the fundamental frequency of 2 MHz. By operating at low frequency, only lumped component solutions were adopted, i.e., inductors, capacitors and resistors. The most important part of the activity concerned the choice of materials and the characterization of the components used in the realization of the circuits, as well as the search of circuit topologies suitable to overcome the technological limitations (e.g., losses on ferrite inductors) or to reduce the complexity of the circuit (i.e., the number of components to handle).

The fabricated tuner allows the synthesis, at the transistor current-generator plane, of any real impedance between 30 Ω and 300 Ω and the possibility to handle, by means of the multiplexer, the harmonic terminations for the most common types of amplifier classes (e.g., class F). The implemented system (tuner, multiplexer, and bias tee) was tested on a GaN HEMT transistor operating in class-F and tuned-load configurations. From these tests, it was observed, that when increasing the output power, the ferrite inductor losses of the multiplexer determine a variation of the synthesized impedance. This problem could be solved through the evaluation of inductors manufactured with different technology or changing the circuit topology.

The load synthesis at the fundamental frequency and at the harmonics with the developed low-frequency load-pull system is definitely simpler and faster compared to the active load-pull solution. Moreover, the implemented setup guarantees excellent performance in terms of impedance stability and power handling capability.

The research activity took its motivation from the study of the waveform engineering approaches for the design of high-frequency power amplifiers. In this context, the developed low-frequency load-pull system has been successfully used for the design of two LDMOS amplifiers in class AB and class F operating in the FM band.

List of Acronyms

AC	Alternating Current
AFG	Arbitrary Function Generator
CAD	Computer Aided Design
CGP	Current Generator Plane
DC	Direct Current
DUT	Device Under Test
EDA	Electronic Design Automation
EP	Extrinsic Plane
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
FET	Field Effects Transistor
GaN	Gallium Nitride
HB	Harmonic Balance
IP	Intrinsic Plane
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LF	Low Frequency
LSLF	Large Signal Low Frequency
LSNA	Large Signal Network Analyzer
PA	Power Amplifier
PAE	Power Added Efficiency
PAs	Power Amplifiers

Pav	Input Available Power
PCB	Printed Circuit Board
RF	Radiofrequency
S	Scattering
VNA	Vector Network Analyzer
VSWR	Voltage Standing Wave Ratio

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