Scalability of Multi-Finger HEMT Performance

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***Abstract*—This letter aims at investigating the impact of the gate width on microwave FET performance, focusing on GaAs HEMT technology as a case study. To accomplish this complex task, the small-signal equivalent-circuit elements together with the major RF figures of merit are thoroughly analyzed for seven HEMTs based on an interdigitated layout. The gate-width impact on device performance is quantitatively and exhaustively estimated using a mathematical and systematical approach.**

***Index Terms*—equivalent circuit, GaAs, high electron-mobility transistor (HEMT), multi-finger layout, scalability.**

I. Introduction

As well known, the gate width (W) is a key physical parameter for microwave FET applications, since widening the active channel enables the achievement of higher output current, transconductance, and output power capability. A thorough analysis of the gate-width impact on the device performance is therefore essential for allowing device manufacturers and circuit designers to exploit advanced FET technologies at their best. The relevance of this research subject can be seen in the large number of articles dealing with the gate-width influence on microwave FET performance [1]-[8]. Although standard scaling rules can be quite straightforwardly applied to the intrinsic bias-dependent section, the specific transistor layout can critically impact the scaling of the extrinsic bias-independent section, especially when mm-wave frequencies are investigated.

The multi-finger layout is widely used to achieve wider conducting channel and, consequently, larger drain current. Thus, the total gate width is given by the product of the number of fingers (N_f) and their length (W_0). A key advantage of this layout consists in reducing the extrinsic gate resistance, which strongly affects the RF noise performance and the maximum frequency of oscillation (f_{max}) [9].

Within this context, the present letter is aimed at investigating the small-signal equivalent-circuit parameters (ECPs) versus W for pseudomorphic HEMTs (pHEMTs) in GaAs technology, which is well-established and very well-suited for mm-wave applications. In particular, the ECPs and the major RF figures of merit are analyzed to identify and quantify the impact of W-variations on performance, putting together new experimental data on state-of-the-art devices and well assessed results. As will be discussed, the scaling of the extrinsic ECPs can critically depend on the layout peculiarities, like the position of the via holes, and certain deviations of the intrinsic ECPs from the ideal scaling behavior can have a strong impact on device performance, like the power gain. This investigation extends our previous scaling analysis for the HEMT technology, in which the attention was focused on exploring the increase of the kink effect in S_{22} with W [10].

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II. Experimental Results

Fig. 1 depicts the equivalent circuit used for the studied multi-finger GaAs pHEMTs with a gate length of 0.15 μm and different W: 2x25 μm, 4x25 μm, 2x50 μm, 6x50 μm, 8x50 μm, 10x60 μm, and 12x60 μm. Scattering (S-) parameters have been measured from 2.5 to 65 GHz. Part of the parasitic access structures have been de-embedded from measurements by using an on-wafer thru-reflect-line (TRL) calibration [11]. This calibration process shifts the input/output reference planes from the probe tips to the gate and drain manifolds, thus eliminating probe pads and launchers and enabling determination of device behavior as when applied in a realistic microwave circuit. The extrinsic ECPs have been extracted from "cold" S-parameters (i.e., V_{DS} = 0 V) [10], [12], thereby enabling calculation of the intrinsic ECPs from the intrinsic admittance (Y-) parameters at the bias point of interest: V_{GS} = -0.6 V and V_{DS} = 6 V. Due to the well-known limitations of the "cold" modeling approach that does not allow distinguishing clearly between extrinsic and intrinsic output capacitances [12], C_{pd} is assumed to be equal to C_{pg}. As an example of the model validity, Fig. 2 compares measured and simulated S-parameters for the largest device.

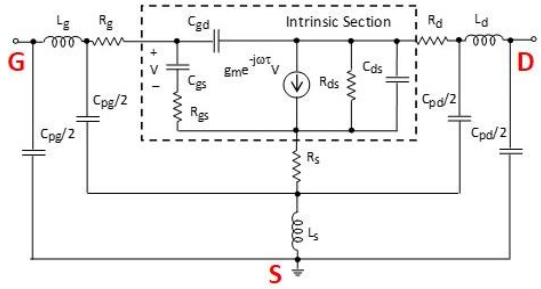
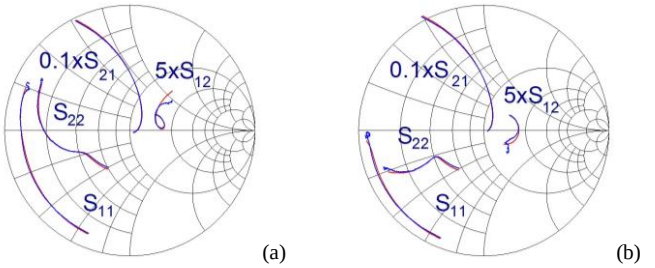


Fig. 1. Small-signal equivalent circuit for the studied GaAs HEMTs.



(a) (b)

Fig. 2. Measured (blue) and simulated (red) *S*-parameters for 720-µm device: (a) before and (b) after de-embedding the extrinsic ECPs.

Table I reports I_D, ECPs, transition frequency f_T (i.e., $g_m/(2\pi C_g)$ with $C_g=C_{gs}+C_{gd}$), and voltage gain A_V (i.e., g_m/g_{ds}) for the tested devices. In line with the well-known expectations that I_D, g_m, g_{ds}, C_{gs}, C_{gd}, and C_{ds} should be linearly dependent on W, their achieved good scaling allows taking the average of the gate-width normalized quantities as the reference values: I_{Dwav} = 0.118 mA/µm, g_{mwav} = 0.454 mS/µm, g_{dswav} = 0.017 mS/µm, C_{gswav} = 1.259 fF/µm, C_{gdwav} = 0.13 fF/µm, and C_{dswav} = 0.244 fF/µm. R_{gs} exhibits the opposite trend, decreasing with W in accordance with the expectation that R_{gs} should be inversely proportional to W, but with more evident deviations, reflecting the fact that its extraction is a more challenging task. Its reference value can be estimated taking the average of $R_{gs}W$: R_{gswav} = 494 Ωµm. Although τ, f_T, and A_V are expected to be gate-width insensitive, the obtained values show some deviations from ideal behavior, which can be attributed to fabrication tolerance, measurement uncertainty, and model approximation. To define a reference value to estimate the deviation, their average values (τ_{av}, f_{Tav}, and A_{Vav}) are evaluated: 1.1 ps, 52.1 GHz, and 25.9.

Although the conventional scaling rules can be applied quite straightforwardly to the intrinsic section, they can strongly depend on the specific layout in case of the extrinsic ECPs. This is the main reason for which, in order to obtain accurate prediction capabilities, electro-magnetic (EM) approaches [5] or extraction techniques based on all the investigated peripheries are adopted. Nevertheless, to properly calibrate the EM simulator, some on-wafer test structures are required (e.g., lines having different lengths) that are not always available. The same applies to the different gate-width devices that are not necessarily all available for characterization. These considerations justify the importance of empirical scaling rules, as the ones discussed in this paper.

The anomalous value of C_{pg} for the largest device is due to the layout that is very different with respect to the other devices (see Fig. 3(d)). The different positions of via holes and how these are very adjacent to the gate/drain manifolds/fingers, thus increasing extrinsic capacitances, is well evident. As the via holes are closer to the gate than to the drain, the assumption C_{pd} = C_{pg} leads to a slight overestimation of C_{pd}, turning into a slight underestimation of C_{ds} and overestimation of L_d (see Table I). The layout with via holes closer to the actual transistor is used to optimize the area consumption for achieving a more compact device, which is a critical feature especially for large devices.

TABLE I. PARAMETERS FOR HEMTS AT V_{GS} = -0.6 V AND V_{DS} = 6 V

W (µm)	*2x25*	*4x25*	*2x50*	*6x50*	*8x50*	*10x60*	*12x60*
I_D *(mA)*	5.6	10.3	11.9	35.4	51.2	74.3	86.7
C_{pg} *(fF)*	12.2	13.2	10	10.2	11.6	9.6	43.8
L_g *(pH)*	45.1	25.6	39.7	26.5	22.2	24.5	21.9
L_d *(pH)*	19.7	16.4	30	23.9	19.1	23.5	45.2
L_s *(pH)*	0	2.5	2.3	3.8	5.7	9.5	7.4
R_g *(Ω)*	6.5	3.7	6.2	1.5	1.4	0.7	0.7
R_d *(Ω)*	15.9	7.6	8.3	1.2	1.7	0.8	0.9
R_s *(Ω)*	6.3	3.3	3.4	0.4	0	0.1	0.2
g_m *(mS)*	24.5	47.1	50.1	131	171	254.6	309.6
R_{ds} *(Ω)*	1043.9	554.4	533.2	195.8	152.1	100.3	83.6
C_{gs} *(fF)*	63.1	133.4	137.4	366.2	470.6	705	916.2
C_{gd} *(fF)*	7.7	15.1	11.5	36.2	48.7	69.6	93
C_{ds} *(fF)*	12.9	30.6	26.1	70.9	89.8	133.7	145.4
R_{gs} *(Ω)*	4.2	1.4	1.5	2.5	1.8	1.4	0.9
τ *(ps)*	0.86	0.98	1.05	1.19	1.14	1.18	1.32
f_T *(GHz)*	55.1	50.5	53.6	51.8	52.4	52.3	48.8
A_v	25.6	26.1	26.7	25.6	26	25.5	25.9

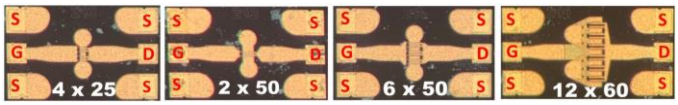


Fig. 3. Photo of four analyzed devices with different gate width.

As expected [2], both R_d and R_s decrease with increasing W. However, R_s is much lower than R_d and, by enlarging W, it can reach very small values that can be even difficult to extract [13]. This is consistent with the fact that the gate is placed closer to the source than to the drain for achieving a higher breakdown voltage and maximizing extrinsic transconductance as R_s has more impact on this parameter than R_d [14].

To put the different impacts of N_f and W_0 in the spotlight, we compare the results for two devices with a W of 100 µm: 4x25 µm and 2x50 µm. Table I shows that the achieved results are quite similar, except for R_g, L_g, and L_d, exhibiting a remarkable decrease by increasing N_f. This is consistent with the fact that a key advantage of using an interdigitated layout consists of reducing R_g. Hence, although W can be enlarged by increasing N_f and/or W_0, only a higher N_f enables reducing R_g. Such a consideration, along with the intrinsic distributed nature of the transistor behavior [15]-[19], discourages the exploitation of finger lengths above 50-60 µm at mm-wave frequencies. The behavior of R_g has been represented using the well-known scaling rule that the gate metallization resistance is proportional to W/N_f^2 (i.e., W_0/N_f), whereas the contribution of the contact resistance is inversely proportional to W and noticeable only at small gate width [2], [9]. In [2], it has been found that L_g scales in a similar way to the gate metallization resistance, while L_d has been observed to be proportional to $W_0/\sqrt{N_f}$ for the studied processes. Although these empirical formulas accounting for layout-dependent distributed effects cannot be straightforwardly applied to our case, they enable explanation of the observed behavior of L_g and L_d, mostly increasing with increasing W_0 and reducing N_f. The largest device has a high L_d that can be ascribed to the overestimation

of C_{pd} (see above) and to the large size of the drain manifold.

Fig. 4 shows the impact of removing the extrinsic ECPs on the measured performance: magnitude of the short-circuit current-gain (h_{21}), maximum stable/available gain (*MSG/MAG*), and the Rollet stability factor (K). Fig. 4(a) shows that the current-gain peak (CGP) [20] appears by increasing gate width, due to the resonance between intrinsic capacitances (i.e., C_{ds}//C_g) and extrinsic inductances (i.e., L_d+L_s). This finding is mostly a consequence of the good scaling properties of the intrinsic capacitances, leading to a reduction of the resonant frequency. The CGP appears to be less pronounced in larger devices, as can be mathematically predicted by using the definition of the damping factor (ζ) in terms of the equivalent-circuit elements [21]. To quantify the size of the CGP, two methods have been proposed in prior works, which are based on calculating the second order derivative of h_{21} in dB vs the frequency [22] or on estimating the area between the two h_{21} curves with and without peak [23]. Hence, depending on the given application, a proper selection of W can enable achievement of a peak in the current-gain at the frequency of interest. After de-embedding the extrinsic ECPs, CGP vanishes because of the subtraction of the extrinsic inductances. h_{21} becomes almost insensitive to W and exhibits a nearly ideal behavior that is approximately as g_m/(jωC_g), rolling off with a slope of approximatively -20 dB/dec and reaching unity at a frequency very close to f_{Tav} (i.e., 52.1 GHz) (see Fig 4(d)).

Fig. 4(b) shows that the power gain drops at a rate of 10 dB/dec and then 20 dB/dec, due to the transition from *MSG* to *MAG* at the frequency where K becomes unity (f_K). Figs. 4(c) and 4(f) illustrate that f_K is lower in larger devices, mainly due to the greater C_{gs}, and that it is increased after de-embedding of the extrinsic ECPs. By comparing the power gain of the two devices having a W of 100 µm, it is found that the device with two fingers exhibits a larger gain (see Figs. 4(b) and 4(e)). This can be attributed to the lower C_{gd} (see Table I), since *MSG* is given by $|Y_{21}/Y_{12}|$ that at low frequencies can be approximated with $|g_m/(j\omega C_{gd})|$. As shown in Fig. 4(b), the power gain is found to be degraded in the two devices with a finger length of 25 µm, due to an increase of the W-normalized C_{gd} that is ascribable to the enhancement of border effects, thereby discouraging the exploitation of too short fingers.

A clear and comprehensive understanding of the scaling of the small-signal parameters is an essential prerequisite for analysis and prediction of the scaling of large-signal and noise performance. Evidence of this statement can be found in the wide application of the small-signal ECPs as cornerstone for building noise and large-signal models [24-30]. As an illustrative example, Fig. 5 shows that, in line with the small-signal analysis, the 2x50-µm device exhibits a higher power gain than that of the 4x25-µm under relatively low-power conditions. This result indicates that 2x50-µm device should be chosen for applications requiring high linearity (e.g., LNA), whereas the gain performance becomes almost N_f-insensitive (at constant total gate width) in strong non-linear regime.

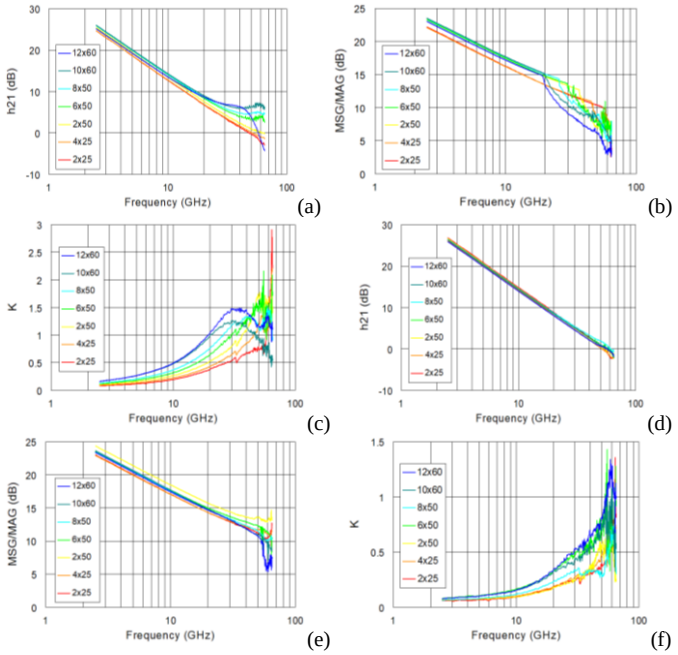


Fig. 4. Measured (a, d) $|h_{21}|$, (b, e) *MSG/MAG*, and (c, f) K for HEMTs with different W: (a, b, c) whole and (d, e, f) intrinsic devices.

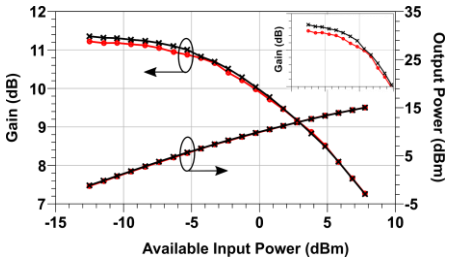


Fig. 5. Measured gain and output power versus available input power at f_0 = 3 GHz, V_{GS} = -0.6 V, and V_{DS} = 6 V in a 50-Ω environment for two 100-µm HEMTs: (black crossed lines) 2x50 µm and (red circled lines) 4x25 µm.

III. Conclusions

The reported empirical analysis provides microwave engineers with valuable information, simply achievable by conventional instrumentation able to measure *S*-parameters. The analysis can be very useful for properly choosing the device periphery, depending on the application constraints. Although the GaAs HEMT technology has been considered as a case study, the developed analysis is technology independent and extensible to other FET types. Furthermore, this study yields to outcomes that can be viewed as representative of any FET technology. On the other hand, it has been shown that the analysis of the impact of the W-scaling on microwave FET performance is not always really straightforward and of general validity as the results can strongly depend on the specific technology and layout. Even when a standard equivalent-circuit model is used, the device performance scaling can strongly depend on the combined effects of the circuit element values.

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