Impact of the Programming Algorithm and Temperature on the Interface-Driven 1st Reset Operation in HfO_2-based 1T1R RRAM Devices

Eduardo Pérez[a], Mamathamba Kalishettyhalli Mahadevaiah[a], Cristian Zambelli[b], Piero Olivo[b], Christian Wenger[a,c]

[a] *IHP, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany*
[b] *Università degli Studi di Ferrara, Dipartimento di Ingegneria, Via G. Saragat 1, 44122 Ferrara, Italy*
[c] *Brandenburg Medical School Theodor Fontane, Fehrbelliner Str. 38, 16816 Neuruppin, Germany*

Abstract

In this work, the increase on the conductive filament conductivity during the 1st Reset operation, by using the incremental step pulse with verify algorithm, in HfO_2-based 1T1R RRAM devices is investigated. A new approach is proposed in order to explain the increase of conductivity by highlighting the crucial roles played by both metal-oxide interfaces. The top metal-oxide interface (HfO_{2-x}/Ti_xO_y) plays a crucial role in the forming operation by creating a strong gradient of oxygen vacancies in the hafnium oxide layer. The bottom metal-oxide interface ($Ti_xO_yN_z/HfO_{2-x}$) also creates oxygen vacancies, which strengthen the conductive filament tip near to this interface at the beginning of the 1st Reset, leading to the reported conductivity increase. After the 1st Reset operation the conductive filament stabilizes at the bottom interface suppressing this behavior in the subsequent reset operations. By modifying the programming parameters and the temperature, it was confirmed a constant current increase of about 9 μA during the 1st Reset regardless the operation conditions imposed.

Keywords: RRAM, HfO_2, 1st Reset, Metal-Oxide Interfaces, Oxygen Vacancies, Temperature

1. Introduction

The resistive random access memory (RRAM) technology has emerged in recent years as a promising platform to carry out several electronic device applications such as non-volatile memories (NVM), artificial synapses in neuromorphic networks and random number generators (RNG) [1, 2, 3]. In RRAM devices based on HfO_2 the resistive switching (RS) effect is attributed to the creation and disruption of nanometer scale conductive filaments (CFs) in the insulator layer, consisting of oxygen vacancies (V_O) [4]. The creation process, referred as set operation, moves the RRAM

devices in a low resistive state (LRS), whereas the disruption process, referred as reset operation, brings the device in a high resistive state (HRS) [5]. To activate these switching operations a preliminary soft breakdown in the insulator, referred as forming operation, is required [6, 7]. This operation plays a fundamental role in determining the subsequent devices performance [8].

The 1st Reset operation has been reported in the literature as a particular case compared to the subsequent reset operations [9, 10, 11]. This difference can be understood regarding the operation performed before the considered reset operation. The 1st Reset is performed after the forming operation, whereas the subsequent reset operations are performed after set operations. The creation of a percolation path through the insulator layer during the forming operation demands the use of substantially higher voltage values compared to those demanded for the reconstruction of the CF during the set operations [7]. Caused by the parasitic capacitances present in the RRAM device and by such high voltage values applied on it during the forming operation, a large amount of charge can be released during the forming transition leading to a current overshoot [13]. This current overshoot flows through the formed CF, which modifies its morphology and impacts dramatically on the switching behavior during the following reset operation, namely, the 1st Reset. The need of lower voltage values during a set operation prevents the current overshoot, the modification of the CF morphology, and thus the impact on the following reset operation. Up to now, the previous explanation has been appropriate for the studies reported in the literature.

However, it does not suit with the experimental measurements reported in one of our previous works [14]. Therefore, a new approach to explain this particular behavior during the 1st Reset was proposed, which highlights the role of both metal-oxide interfaces, namely, $Ti_xO_yN_z/HfO_{2-x}$, referred as bottom interface (BI), and HfO_{2-x}/Ti_xO_y, referred as top interface (TI). In addition, in this work, since the temperature has a strong impact on the formation and diffusion of V_O [15], different temperatures in the range from -40 to 150 °C were used for the experimental measurements in order to assess its impact on the 1st Reset operation.

2. Experimental

All the experimental measurements reported in this study were performed on batches of 128 1T1R devices. Each 1T1R device is constituted by a NMOS transistor, manufacturated in 0.25 μm CMOS technology at IHP, whose drain is connected in series to the metal-insulator-metal (MIM)

resistor, placed on the metal line 2 of the CMOS process (Fig. 1). The MIM cell consists of a TiN/Oxide/Ti/TiN stack of 150 nm TiN layers and a 7 nm Ti layer (under the TiN top electrode) deposited by magnetron sputtering, and a 6 nm oxide layer based on HfO_2 grown by atomic layer deposition (ALD). After patterning the MIM cells with an area of about 0.4 μm^2, an additional thin Si_3N_4 layer was deposited to protect the MIM cell.

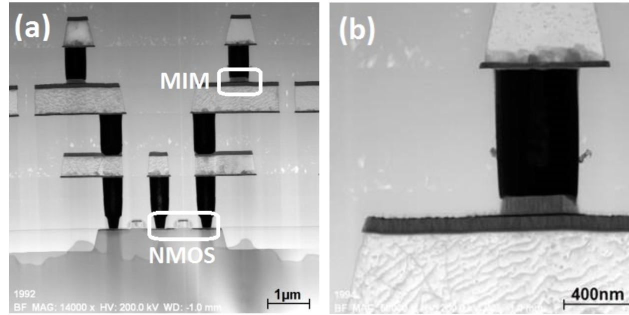

Figure 1: Cross-sectional TEM image of the 1T1R integrated cell (a), and of the MIM cell in more detail (b) [16].

In order to reduce the cell-to-cell variability, the incremental step pulse with verify algorithm (ISPVA) has been the programming strategy used to perform the switching operations (forming, reset and set) in our studies for recent years [17, 18, 19]. The ISPVA technique consists of a sequence of increasing voltage pulses (Fig. 2) applied on the drain terminal during set and forming operations, whereas this sequence is applied on the source terminal during reset operations. After every pulse a read-verify operation is performed by using a read-out pulsed voltage of V_{READ} = 0.2 V. In this work each pulse featured a duration of t_{PULSE} = 10 μs. The programming operation is stopped on a cell when the read-out current reach a specific target value, referred as threshold current (I_{th}).

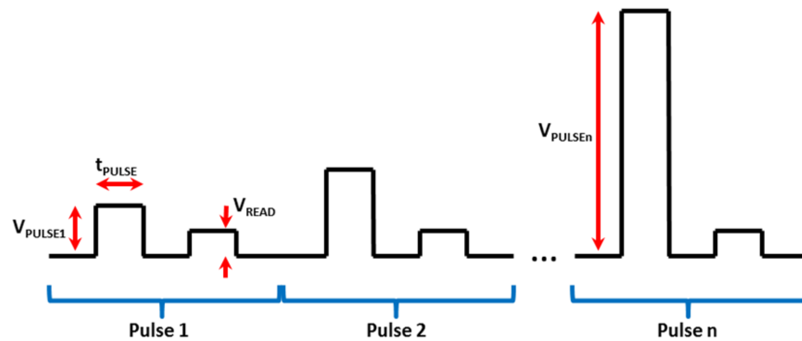

Figure 2: Schematic illustration of the incremental step pulse with verify algorithm (ISPVA) [20].

3. Results and Discussion

During the forming operation the amplitude of voltage pulses in the ISPVA was swept in the range of 2-5 V with a voltage step of 0.01 V, applying a gate voltage (V_g) of 1.4 V and defining I_{th} = 30 μA. The evolution of the current values measured after each pulse in the sweep is shown in Fig. 3(a). For the reset and set operations the amplitude of programming pulses was swept between 0.2 and 3.5 V with a voltage step of 0.1 V. The reset operations were performed applying a V_g = 2.7 V and defining I_{th} = 5 μA, while during the set operations the values used for these two parameters were the same as in the forming operation. As shown in Fig. 3(b), the evolution of current values measured for the 1st Reset features a significant increase before performing the reset transition. Such a current increase is suppressed in the subsequent reset operations, as shown in Fig. 4(b) for the second reset operation.

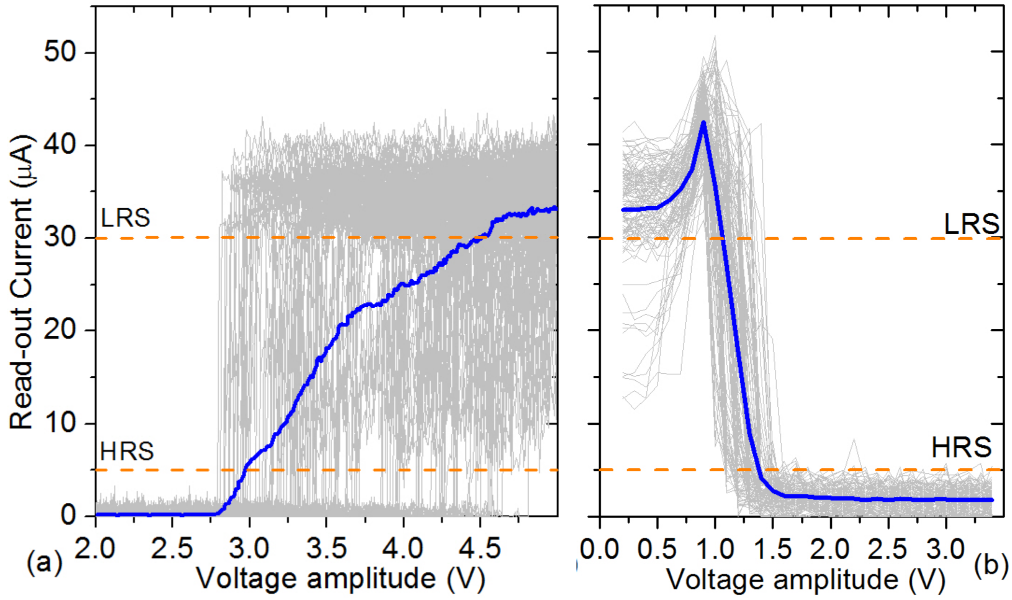

Figure 3: Evolution of the read-out current values during the ISPVA for the forming (a) and the 1st Reset (b) operations on 128 devices (grey) and its average (dark blue).

As previously mentioned, this difference is usually attributed to a current overshoot occurring during the forming transition, which does not occur during the set transitions, caused by the parasitic capacitances present in the RRAM device [21, 22]. However, caused by the use of the read-verify scheme this increase in the CF conductivity during the 1st Reset must be related with a modification in the CF morphology at that specific time. Thus, we propose a new approach to

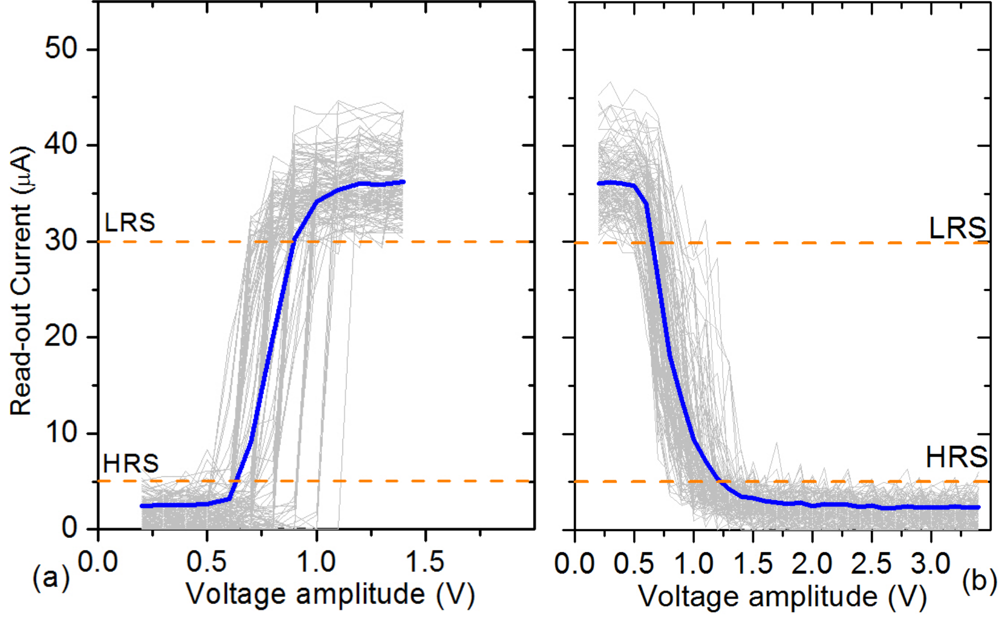

Figure 4: Evolution of the read-out current values during the ISPVA for the set (a) and the second reset (b) operations on 128 devices (grey) and its average (dark blue).

explain this conductivity increase during the 1st Reset by highlighting the crucial role played by both metal-oxide interfaces, namely, the BI ($Ti_xO_yN_z/HfO_{2-x}$) and the TI (HfO_{2-x}/Ti_xO_y).

In order to discard the ISPVA as the responsible of this behavior, additional values of its two main parameters, namely, I_{th} and V_g, were tested during the forming operation. By applying the same V_g (1.4 V) and changing the definition of I_{th} to 20 and 40 μA, the evolution of the read-out currents during the 1st Reset, as shown in Fig. 5(c) and (d), respectively, feature the same change already shown in Fig. 3(b) regardless the I_{th} defined. Furthermore, by defining the same I_{th} (30 μA) and changing the applied V_g to 1.0 and 1.6 V, the evolution of the read-out currents during the 1st Reset feature the change shown in Fig. 5 (a) and (b), respectively. Although the current values at the peak are obviously different regarding the V_g applied during the forming operation, the current increase featured before the reset transition is essentially the same. As depicted in Fig. 6, the current values at the peak (Maximum) increase linearly with the applied V_g, from about 20 to about 50 μA, similarly as the current values at the beginning of the reset process (Initial), from about 10 to about 38 μA. Therefore, the difference between the Maximum current values and the Initial current values (Maximum - Initial in Fig. 6) is almost constant regardless the applied V_g, with a value of about 9 μA. According to this result, the lineal dependency of the Maximum

current values with V_g is a consequence of the lineal dependency of the Initial current values with V_g, which is indeed established during the forming operation.

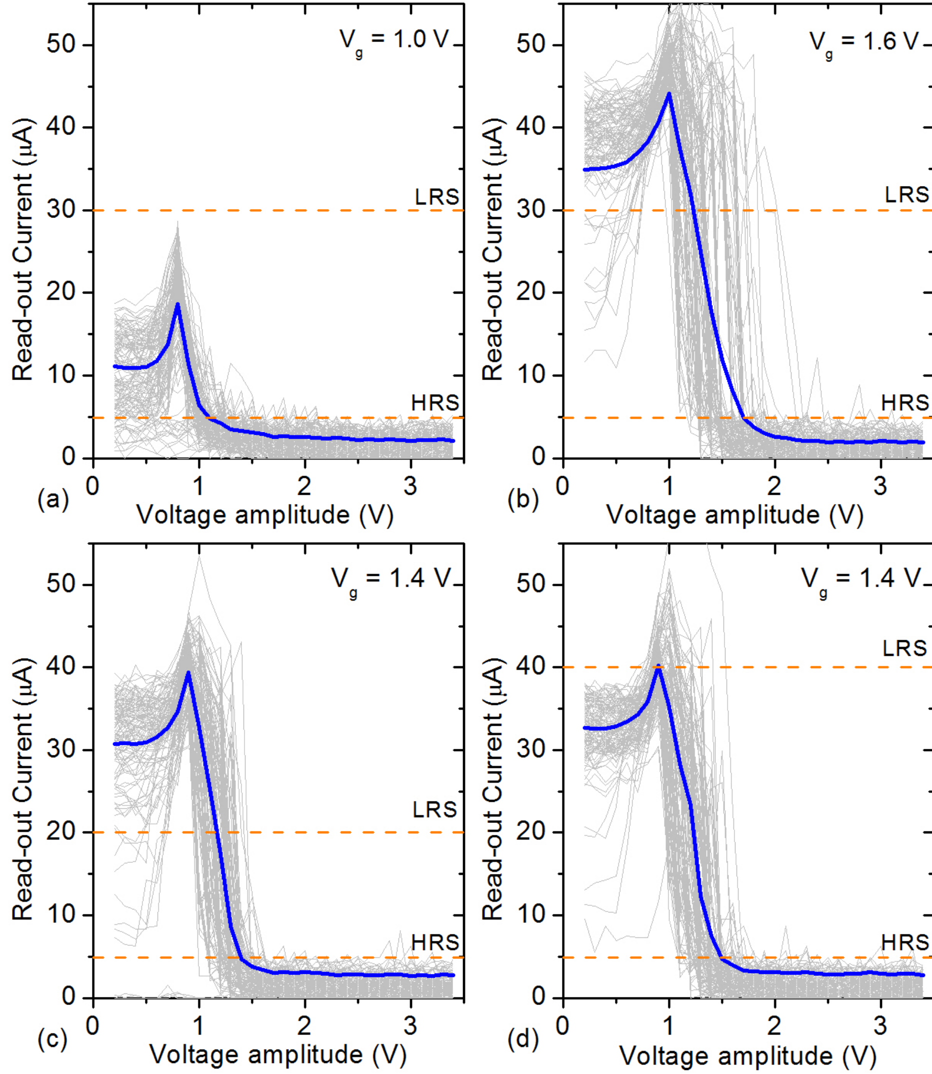

Figure 5: Evolution of the read-out current values during the ISPVA for the 1st Reset operation on 128 devices (grey) and its average (dark blue), by using different values of V_g: 1.0 and 1.6 V (a)-(b), respectively; and I_{th}: 20 and 40 μA (c)-(d), respectively; during the forming operation.

Once the ISPVA is rejected as the responsible of the current increase during the 1st Reset, the results shown in the following will be those obtained by using I_{th} = 30 μA and V_g = 1.4 V during the forming. In Fig. 7 the cumulative distribution functions (CDFs) of read-out currents are illustrated corresponding to the CF morphologies depicted in Fig. 8 for five relevant scenarios. During the forming, the drift of V_O, formed by the scavenging ability of Ti in HfO_2 layers, creates

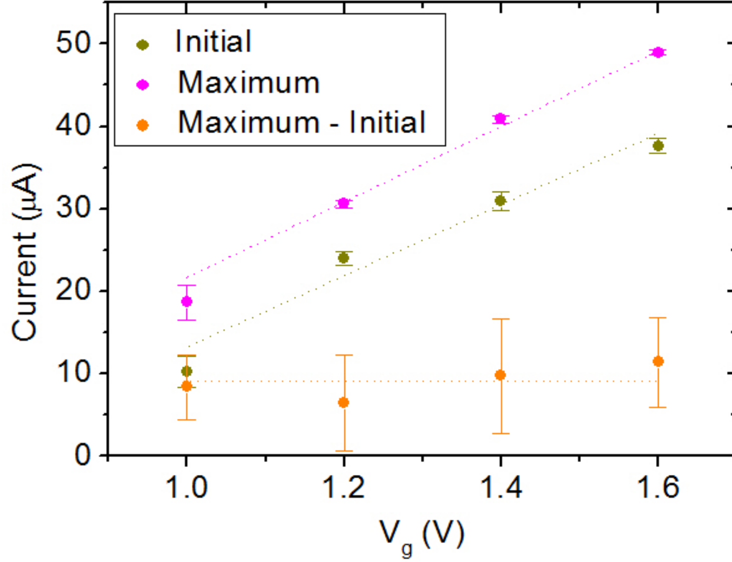

Figure 6: Average and dispersion values of the read-out currents at the beginning of the 1st Reset process (Initial), at the peak (Maximum), and of the difference between them (Maximum - Initial), by using several V_g values during the forming operation.

a CF with a weak tip near to the BI, as illustrated in Fig. 8(a) [23]. The CDF of read-out currents in this scenario, that is, after the forming transition, is depicted in red in Fig. 7, ranging between 30 and 40 μA.

According to previous publications a thin $Ti_xO_yN_z$ layer appears at the BI, which supports the formation of V_O close to this interface [24, 25, 10]. At the beginning of the 1st Reset, these V_O drift strengthen the tip of the CF near to the BI, as illustrated in Fig. 8(b). This behavior is in line with the increase of read-out currents depicted in Fig. 3(b). The current increase attains a peak at a voltage value of about 1.0 V. The CDF of current values measured at this peak is shown in dark green in Fig. 7, ranging between 35 and 50 μA, which shows a meaningful increase compared to the CDF of currents measured after the forming transition (in red). When reset voltage is further increased beyond 1.0 V, such a drift opens a gap along the CF, as illustrated in Fig. 8(c), driving the device to HRS, whose current CDF is shown in bright green in Fig. 7.

By applying the set operation (Fig. 4(a)) the CF is reconstructed, as shown in Fig. 8(d). The CDF of the currents measured after the set transition, in magenta in Fig. 7, ranging between 30 and 45 μA, shows that the conductivity of the resultant CF is slightly higher than after forming operation (in red) and, besides, quite lower than at the current peak during the 1st Reset (in dark

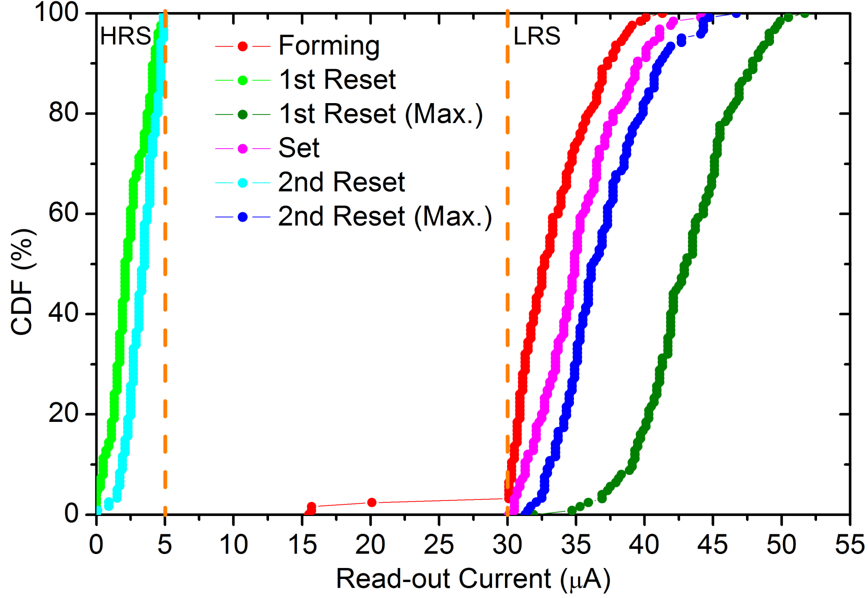

Figure 7: Cumulative distribution functions (CDFs) of the read-out currents measured after the forming (red), at the current peak in the 1st Reset (dark green), after the 1st Reset (bright green), after set (magenta), after the second reset (bright blue), and at the maximum current value in the the second reset (dark blue).

green). As shown in Fig. 8(d), the CF after the set operation is thicker near to the BI than after forming operation (Fig. 8(a)) and, therefore, its conductivity is higher, which is in line with the results shown by the CDFs in Fig. 7. Furthermore, according to the CDFs in Fig. 7, the CF after the set operation (Fig. 8(d)) is narrower than at the current peak during the 1st Reset (Fig. 8(b)). As illustrated in Fig. 9, the voltage values required to reconstruct the CF in the set operation (in magenta), ranging between 0.7 and 1.2 V, are dramatically lower than those required to create the CF in the forming operation (in red), ranging between 2.9 and 5.0 V. Therefore, during the set operation, the gap previously depleted is filled only by a few V_O (Fig. 8(d)) leading to a narrower CF compared to the CF present before the 1st Reset (Fig. 8(b)), which was created during the forming operation at much higher voltages.

The subsequent reset operations, as depicted in Fig. 8(e), open the gap without morphology changes in the tip of the CF near to the BI. This lack of morphology changes suppresses the current increase featured by the 1st Reset, as shown in the evolution of read-out current values in Fig. 4(b). Thus, as illustrated in Fig. 7, the CDF of the maximum current values achieved during the second reset (in dark blue) is essentially the same as the CDF of LRS currents after the set operation (in

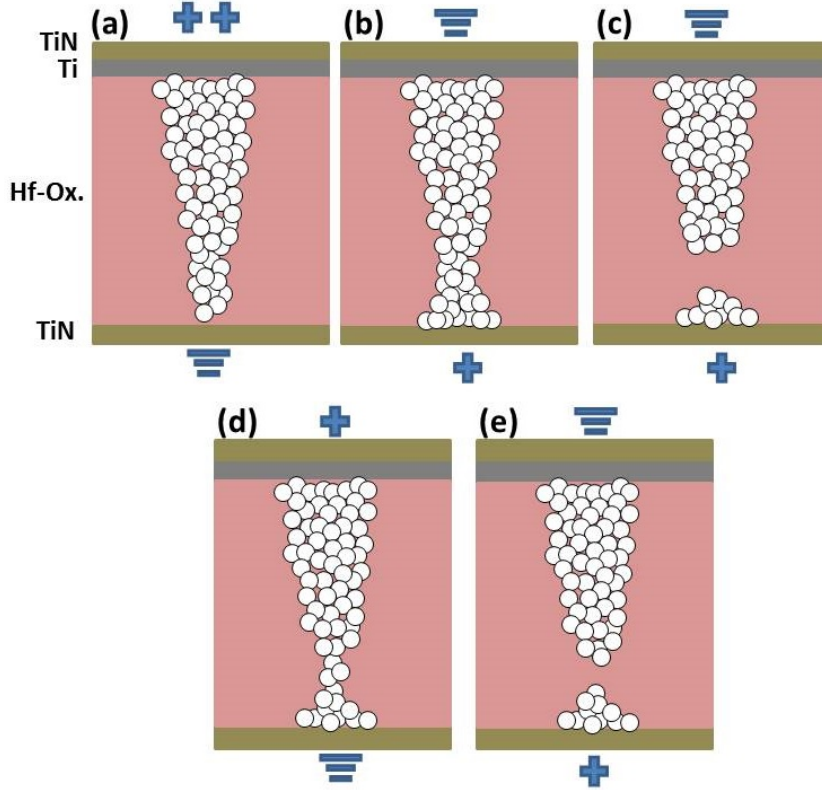

Figure 8: Conductive filament (CF) morphologies after the forming (a), at the current peak in the 1st Reset (b), after the 1st Reset (c), after set (d), and after the second reset (e).

magenta). Besides, the second reset leads to a more conductive HRS, as shown by the current CDF in bright blue in Fig. 7. The weaker electrical stress applied during the second reset compared to the 1st Reset, as shown by the CDFs of reset voltages in bright blue and bright green in Fig. 9, respectively, can be responsible for that difference. Weaker electrical stress during reset operation leads to a narrower gap along the CF and, therefore, to a HRS with higher conductivity [26]. In addition, the lower voltages required to disrupt the CF during the second reset compared to the 1st Reset supports the statement that during the set operation only a few V_O filled the gap (Fig. 8(d)) leading to a narrower CF compared to the CF present after the forming operation (Fig. 8(a-b)).

Since the temperature has a strong impact on the formation and diffusion of the V_O inside of the HfO_2-based switching layer and thus on the CF morphology [15], the forming and the 1st Reset operations were also carried out by using additional temperature values: -40, 85 and 150 ^{o}C. As shown in Fig. 10, the evolution of the read-out currents during the 1st Reset features

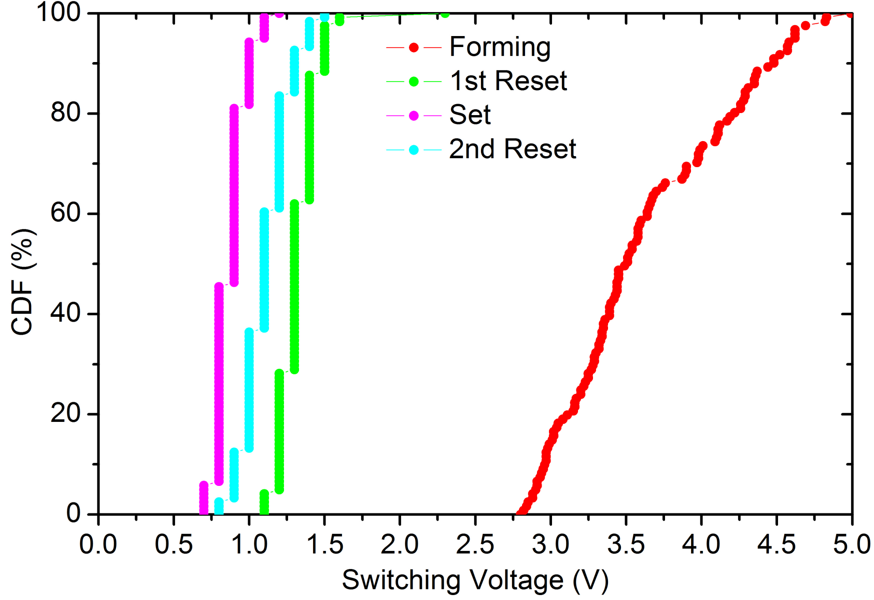

Figure 9: CDFs of the switching voltages in the forming operation (red), in the 1st Reset (bright green), in set operation (magenta), and in the second reset (bright blue).

essentially the same behavior already depicted in Fig. 3(b) at room temperature, that is, at 25 ^{o}C. Furthermore, a dramatic decrease of the Initial and the Maximum current values with the temperature is observed. As shown more in detail in Fig. 11, the Maximum current values decrease linearly with the temperature from about 45 to about 32 μA. The same trend with the increase in temperature is observed for the Initial current values from about 36 to about 24 μA. However, the difference between the Maximum and the Initial current values (Maximum - Initial in Fig. 11) is almost constant regardless the temperature, with a value, again, of about 9 μA. Therefore, the temperature variation just impacts the Initial current values, which are already established during the forming operation. In consequence, the variation with the temperature of the Maximum current values is only a consequence of the constant current increase featured during the 1st Reset operation.

4. Conclusions

The increase in the conductivity of the CF before its disruption during the 1st Reset operation has been studied by using the ISPVA in HfO_2-based 1T1R RRAM devices. The read-out currents measured in different scenarios were illustrated with the corresponding morphologies of the CF,

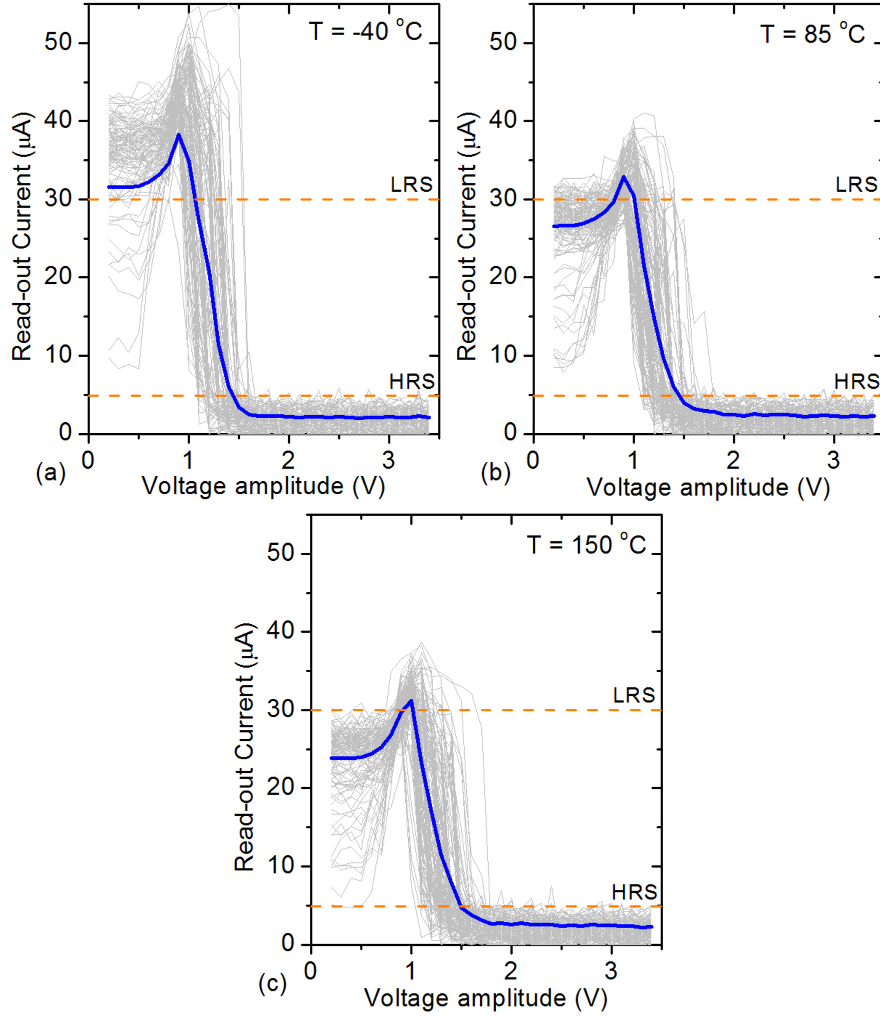

Figure 10: Evolution of the read-out current values during the ISPVA for the 1st Reset operation on 128 devices (grey) and its average (dark blue) performed at different temperatures: -40 (a), 85 (b), and 150 (c) °C.

which gives insights about the roles of both metal-oxide interfaces. Caused by the scavenging ability of Ti, the TI is crucial for the forming operation in HfO_2 layers leading to a strong gradient of the V_O content from the top electrode to the bottom electrode, whereas the BI seems to be the responsible of the current increase during the 1st Reset because of the formation of a thin $Ti_xO_yN_z$ layer, which supports the formation of additional V_O close to this interface. Since these changes in the morphology of the CF near to the BI are featured only during the 1st Reset, the increase of the CF conductivity before the reset transition is suppressed in the subsequent reset operations. By using different values for the two main parameters of the ISPVA (V_g and I_{th}) during the forming

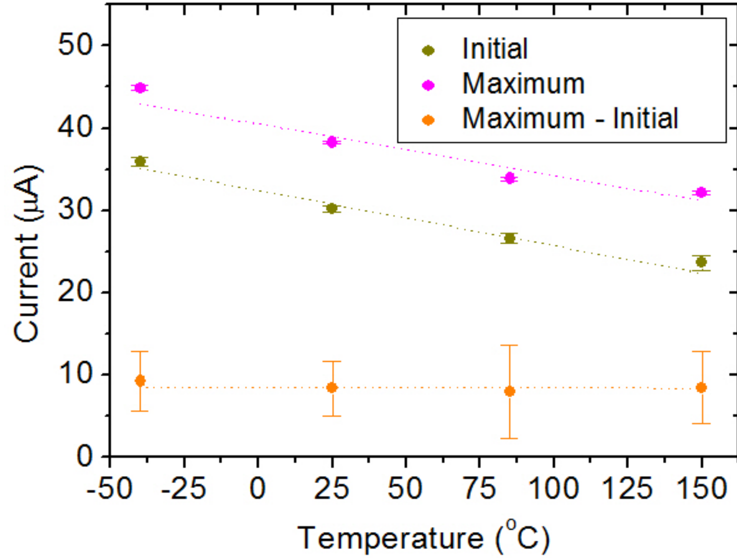

Figure 11: Average and dispersion values of the read-out currents at the beginning of the 1st Reset process (Initial), at the peak (Maximum), and of the difference between them (Maximum - Initial) at different temperatures: -40, 25, 85, and 150 °C.

operation, the programming algorithm was discarded as the responsible of such a conductivity increase during the 1st Reset. In addition, the impact of the temperature was tested in the range between -40 and 150 °C during the forming and the 1st Reset operations. In both cases only the conductivity values of the CF at the beginning of the reset operation were affected, which are effectively established by the forming operation. A constant increase of about 9 μA was confirmed regardless the operation conditions imposed during the forming.

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