Data Retention Investigation in Al:HfO_2-based RRAM Arrays by using High-Temperature Accelerated Tests

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In this work the feasibility of using accelerated tests at high temperatures to test the data retention on RRAM devices was evaluated on Al:HfO_2-based 1T1R 4kbit arrays. By baking the samples at three different temperatures (190, 210, and 230 °C) for 10 h, three different distributions of retention failure times were obtained and modelled by using the Weibull distribution. Based on the temperature dependency of these distributions, the Arrhenius activation energy of the degradation process was calculated (1.35 eV). In addition, the temperature that guarantee a retention time to failure of 10 years was extrapolated (120 °C). An acceleration factor of about 1.5×10^3 let to reduce the time for the retention test from 10 years to 30 hours.

Keywords: RRAM, Al-doped HfO_2, Data Retention, Accelerated Test, Weibull Distribution, Activation Energy.

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I. INTRODUCTION

Resistive random access memories (RRAM) based on HfO_2 with 1T1R architecture are one of the most promising candidates to replace Flash technology in non-volatile memory (NVM) applications[1–3]. RRAM behavior is based on the possibility of electrically modifying the resistivity of a metal-insulator-metal (MIM) stack, in other words, on performing resistive switching (RS)[4]. The set operation moves the cell in a low resistive state (LRS), whereas the reset switches the cell back to a high resistive state (HRS). In HfO_2-based technologies the RS is attributed to the creation and disruption of nanometer scale conductive filaments (CFs) in the insulator layer, consisting of oxygen vacancies (V_O)[5,6]. To activate the switching behavior a preliminary soft breakdown in the dielectric material is required, referred as forming operation[7,8]. This operation plays a fundamental role in determining the subsequent devices performance[9].

The capability of NVM devices to store the information programmed for a long period of time, referred as data retention, is one of the most crucial characteristics and still a key issue to solve in order to attain a reliable operation[10–17]. The most widespread target value for data retention is 10 years, which is an unpractical duration for reliability tests. In order to simulate such a long duration by consuming a practical amount of time, accelerated tests emerge as a very valuable strategy[18]. In this study, data retention of Al:HfO_2-based 1T1R cells integrated in 4kbit arrays was evaluated by using high temperatures as the stress acceleration condition. From the outcome of this test the activation energy of the degradation process was calculated and the working temperature that guarantees 10 years before retention failure extrapolated.

II. EXPERIMENTAL

The 1T1R cells in the 4kbit arrays (Fig. 1) are constituted by a select NMOS transistor manufactured in a 0.25 μm CMOS technology whose drain is in series to a MIM stack. The variable MIM resistor (Fig. 2) is composed by 150 nm TiN top and bottom electrode layers deposited by magnetron sputtering, a 7 nm Ti layer (under the TiN top electrode), and a 6 nm Al-doped HfO_2 layer deposited by atomic layer deposition (ALD) with an Al content of about 10 %. After patterning the MIM cells with an area of about 0.4 μm^2, an additional

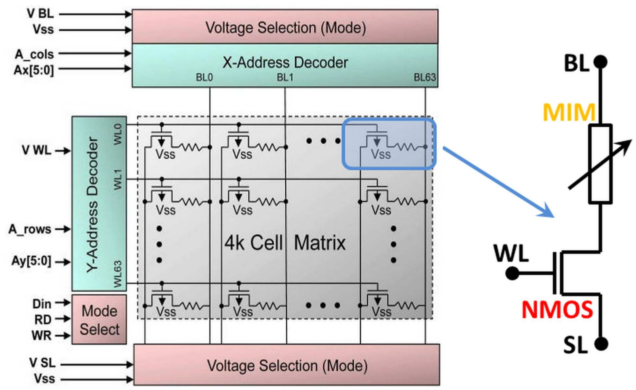

FIG. 1. Block diagram of the 4kbit memory array and schematic of the 1T1R cell integrated in the arrays.

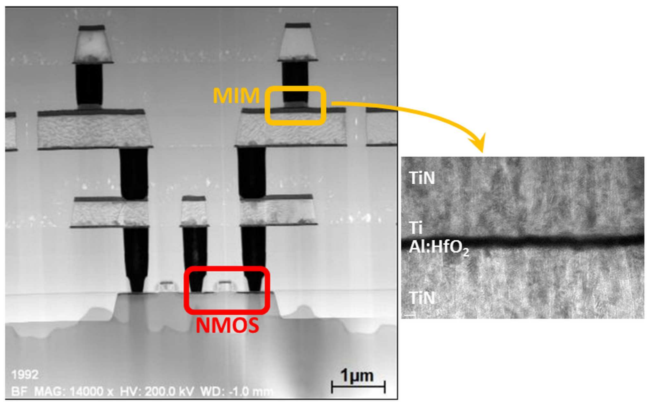

FIG. 2. Cross-sectional TEM image of the 1T1R integrated cell and of the MIM stack in more detail.

thin Si_3N_4 layer was deposited to protect the MIM cell.

Prior to the retention test, the forming operation and a first reset/set cycle were performed at room temperature (RT) on three batches of 128 1T1R cells by using the incremental step pulse with verify algorithm (ISPVA)[19]. The ISPVA technique consists of a sequence of increasing voltage pulses (of 10 μs) applied on the bit line (BL), connected to the MIM resistor, during forming and set operations, whereas this sequence is applied on the source line (SL), connected to the source terminal of the transistor, during reset operation. After every pulse a read-verify operation is carried out by using the BL. The programming operation is stopped on a cell when the read-out current reaches a specific threshold value (I_{th}). Afterwards, each batch was baked for 10 hours at one of the following temperatures: 190, 210, and 230 °C. The evolution of the LRS conductivity was monitored every hour by using the read-out operation at 0.2 V.

III. THEORETICAL BASIS

Since the retention failures are based on the drift of oxygen vacancies (V_O)[6,12], the degradation rate can be described by the Nerst-Einstein equation[20]. Thus, the mean time to failure (MTTF) can be modeled by the Arrhenius equation:

$$MTTF = A \times exp(E_a/kT), \tag{1}$$

where A is a preexponential constant, E_a is the activation energy of the degradation process, k is the Boltzmann's constant and T is the operating temperature of the device. Assuming the hypothesis that the failure mechanism is maintained during the acceleration stress, a linear transformation of time can be performed[20]:

$$MTTF_u = AF_{us} \times MTTF_s, \tag{2}$$

where the subscripts u and s mean use condition (at the temperature T_u) and stress condition (at the temperature T_s), respectively, and AF_{us} is the acceleration factor between T_u and T_s, defined by the following expression:

$$AF_{us} = exp[E_a/k \times (T_u^{-1} - T_s^{-1})). \tag{3}$$

Therefore, the retention test can be accelerated by using a high temperature T_s and afterwards the results can be extrapolated to the temperature of use T_u[18]. In order to calculate the MTTF values from a group of devices, the time to failure distributions can be modelled by using the Weibull distribution, according to the following equation[20,21]:

$$MTTF = \alpha\Gamma(1 + 1/\beta), \tag{4}$$

where α and β are the scale parameter (also known as characteristic lifetime) and the shape parameter, respectively, of the Weibull distribution, and Γ(x) is the Euler's gamma function.

IV. RESULTS AND DISCUSSION

To activate the resistive switching behavior, the forming operation was performed at RT by using I_{th} = 18 μA and a voltage on the word line (WL), connected to the gate terminal of

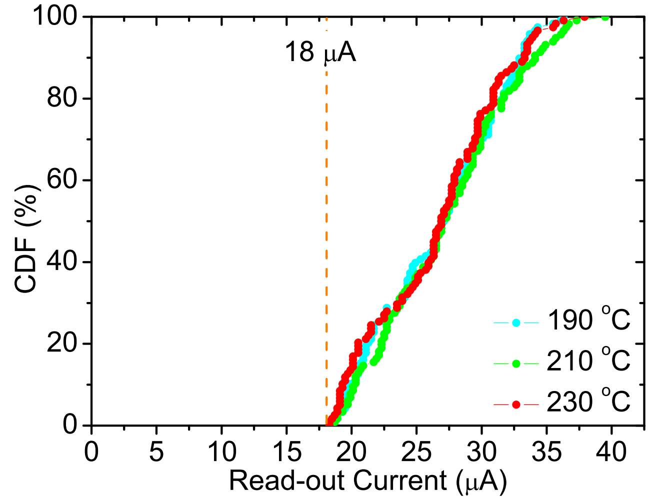

FIG. 3. Cumulative distribution functions (CDFs) of the read-out currents measured after the forming transition for the three batches of 128 RRAM cells.

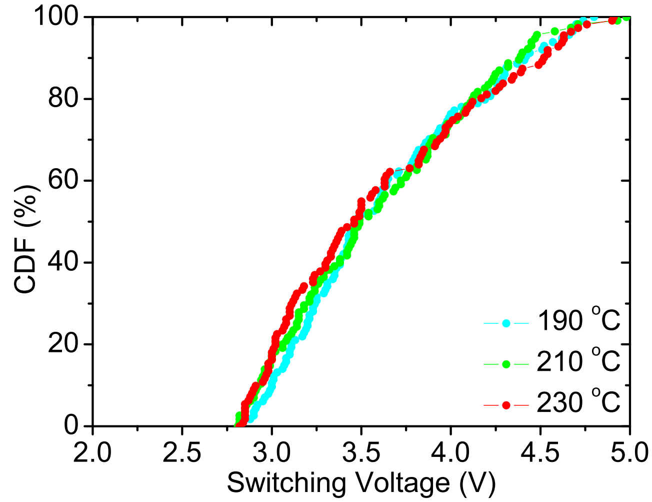

FIG. 4. CDFs of the switching voltages at the forming transition for the three batches of 128 RRAM cells.

the transistor, equal to 1.4 V. The amplitude of the voltage pulses in the ISPVA was swept in the range of 2-5 V with a voltage step of 0.01 V. In Fig. 3 and 4 are shown the cumulative distribution functions (CDFs) of the read-out currents after the forming operation and of the switching voltages at the forming transition, respectively, for the three batches of 128 RRAM cells.

Afterwards, the first reset/set cycle was carried out at RT in order to program all RRAM cells in a really stable LRS[22]. The amplitude of the ISPVA voltage pulses was swept during

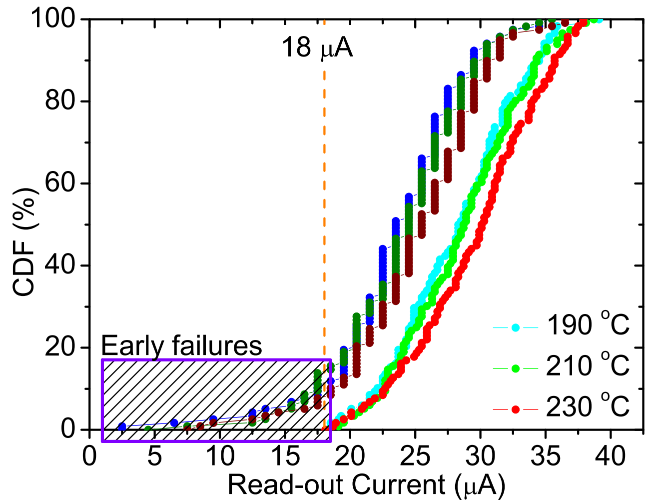

FIG. 5. CDFs of the read-out currents measured after the set operation (bright colors) and after the preliminary baking time, which is required to achieve the targeted temperature (dark colors).

both operations in the range of 0.2-3.5 V with a voltage step of 0.1 V. The reset operation was performed applying a $V_g = 2.7$ V and defining $I_{th} = 6$ μA, while in the set operation the values used for these two parameters were the same as in the forming operation. The CDFs of read-out currents after the reset operation are not shown, whereas those after the set operation are shown in bright colors in Fig. 5.

In order to determine the retention times of failure, a criterion of failure has to be defined: cells in the LRS whose read-out current cross down the I_{th} of the set operation (18 μA). After increasing the temperature to one of the corresponding baking values (190, 210, and 230 °C, respectively), caused by the metallic-like conduction of the LRS[23,24], a current shift of about 5 μA occurs in the CDFs, as shown in Fig. 5 in dark colors. During this preliminary baking time, until the targeted temperature is achieved, also a tailing of the CDFs occurs, attributed to the so called "infant mortality"[20,25]. All the cells that reached the criterion of failure during the temperature increase, referred as early failures, were not considered in the retention analysis regardless the cause of failure.

From the evolution of the read-out currents CDFs during the baking, as shown in Fig. 6 for several sampling times (0, 1, 5 and 10 hours) at the three different temperatures, the number of RRAM cells failing at each sampling time can be calculated. As a result, the distributions of the retention failure times are obtained for the three temperatures, as shown in Fig. 7. As depicted in Fig. 8, the distributions of the retention failure times can

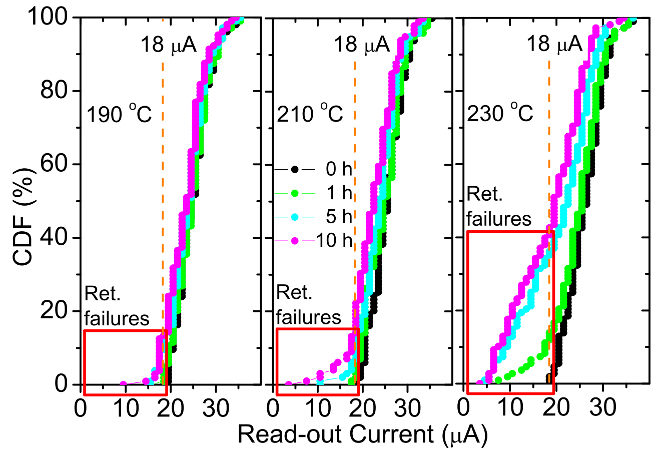

FIG. 6. CDFs of the read-out currents measured during the baking for several sampling times: 0, 1, 5 and 10 hours; at the three temperatures: 190, 210, and 230 °C.

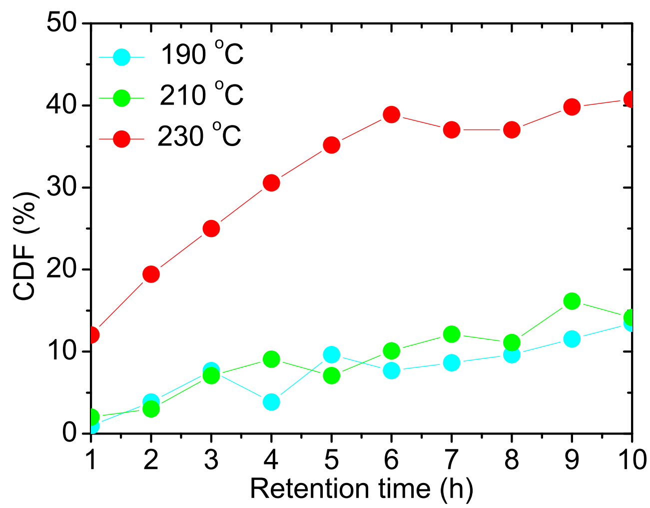

FIG. 7. Distributions of retention failure times at the three temperatures: 190, 210, and 230 °C.

be modelled by using the Weibull distribution. The scale and shape parameters (α and β, respectively) extracted from the Weibull fits at the three different temperatures are listed in Table I.

In order to calculate the MTTF values at each temperature, the resulting values for the Weibull parameters were substituted in Eq. 4. Based on the temperature dependency of MTTF described in Eq. 1, the calculated MTTF values were depicted in the Arrhenius plot shown in Fig. 9. From the slope of the linear fit a value for E_a equal to 1.35 eV was obtained. This value is in very good agreement with the value already reported by Zhao *et al.*[26], that is 1.36 eV, which was experimentally calculated by baking the samples in a

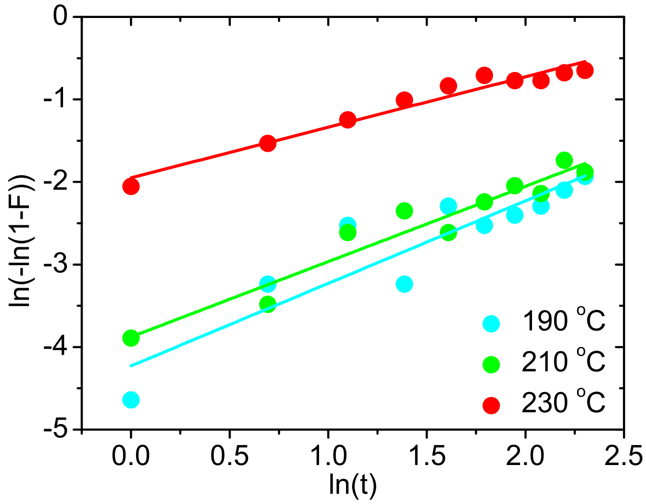

FIG. 8. Weibull plot for the distributions of the retention failure times at the three temperatures: 190, 210, and 230 °C; with the three linear fits.

TABLE I. Summary of the Weibull fit parameters for the retention failure times distributions at the three temperatures.

Temperature (°C)	Scale parameter α	Shape parameter β
190	68.65	1.00
210	70.06	0.91
230	24.21	0.61

range of temperatures from 175 to 230 °C, very similar to the one used in our study. In addition, the E_a value is also in good agreement with the experimental value reported by Traoré *et al.*[12], that is 1.75 eV, calculated by baking the samples in a range of temperature from 200 to 300 °C. The disagreement between these two energy values could be caused by the different definition of the criterion of failure used during the retention test. According to the *ab initio* calculations performed by Traoré *et al.*[12], the E_a value is quite different with a value between 2.08 and 2.69 eV. In this specific case the disagreement could be linked to the fact that the *ab initio* simulations only take into account the migration of V_O caused by bulk diffusion in the Al-doped HfO_2 switching layer, which neglects, for instance, the influence of the metal-insulator interfaces on the retention behavior[27].

Assuming that T_s = 210 °C, the $MTTF_{210}$ value in the linear fit is equal to about 57 h. From this value, the MTTF can be extrapolated by using Eq. 2 to a working temperature

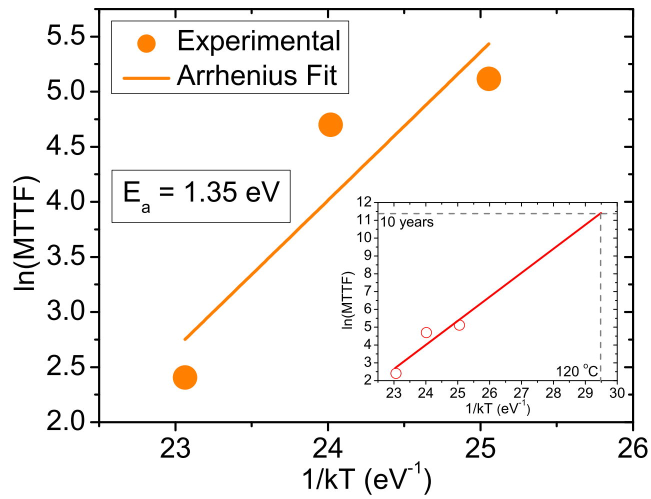

FIG. 9. Temperature dependence of the MTTF with the corresponding Arrhenius fitting. In the inset, the extrapolation of MTTF to a value of 10 years is illustrated.

(T_u) where the value of the MTTF ($MTTF_u$) is equal to 10 years. According to the extrapolation shown in the inset of Fig. 9, the temperature value T_u that guarantee a MTTF of 10 years is about 120 °C. Therefore, the AF value achieved between these two temperatures in the present retention test was about 1.5×10^3, which let us to reduce the time for the retention test from 10 years to only 10 hours for every temperature considered: 30 hours in overall in our study.

V. CONCLUSIONS

In conclusion, accelerated tests by using high temperatures as stress acceleration condition have proved to be an effective strategy to evaluate data retention and provide the activation energy of the degradation process. In Al:HfO_2-based 4kbit RRAM arrays it was shown an acceleration factor of about 1.5×10^3 between the test temperature and the temperature that guarantee a data retention of 10 years. Such an acceleration lead to a reduction of the duration of the test to 30 hours. Therefore, in future evaluations of reliability on RRAM devices the use of this approach would be strongly advised.

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