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# NONLINEAR TRANSISTOR MODELS AND DESIGN TECHNIQUES FOR HIGH-EFFICIENCY MICROWAVE POWER AMPLIFIERS

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# PREFACE

In recent years, electronic technologies oriented to communications went through a continuous and pressing development due to several factors. On one hand, the development of the internet network and its related information systems caused an increasing interest of the people in using devices capable of ensuring a constant connection to those services. This aspect greatly improved the wide diffusion of mobile devices and new generation technologies, such as 3G and 4G/LTE, were developed to satisfy more and more demanding requirements. On the other hand, other systems such as geolocation services (e.g., GPS and GLONASS), initially built for military purposes, are now diffused and commonly adopted by an increasing number of people.

While the consumer market has given a significant boost to communication technologies, other sectors have seen a tremendous development. As an example, satellite systems for Earth observation (such as the COSMO-SkyMed system for the observation of the Mediterranean basin) plays today a fundamental role in the prevention and the management of natural phenomena.

The aforementioned examples of communication systems exploit microwave frequency technologies for the transmission of large amounts of data, thanks to the availability of larger bandwidths. This necessarily implies use of high-power and high-efficiency technologies in line with the requirements of the systems where they are exploited.

When these aspects are taken into account, the attention focuses on the basic element which mainly determines the performance of an electronic circuit: the transistor.

New technologies based on particular semiconductors such as Gallium Arsenide (GaAs) and Gallium Nitride (GaN) are revealing themselves as great solutions for the realization of transistors with excellent performance at micro- and mm-wave frequencies. Because of their relative immaturity compared to well-assessed technologies, such as Silicon, they are of great interest in the research field, in order to identify their limitations and margins of improvement.

The research activities carried out during my PhD program lie in this framework. In particular, the attention has been focused on the nonlinear modeling of transistors for microwave applications and on the study, as well as the application, of design techniques to optimize the performance of power amplifiers.

In Chapter 1 nonlinear transistor modeling techniques will be briefly reviewed. Then, the attention will be focused on the problem of the low-frequency dispersion affecting new generations of electron devices, which strongly influences their dynamic behavior and, therefore, their performance at high frequency. To this end, a low-frequency measurement setup oriented to the analysis of this phenomenon will be described since it has been widely used throughout the research activity.

Successively, two different modeling approaches, namely the compact and the behavioral ones, will be considered. Two techniques based on the setup described in Chapter 1 have been analyzed and developed in the PhD activity and will be presented in Chapters 2 and 3 respectively.

Finally, Chapter 4 will be devoted to the design of microwave power amplifiers. In particular, the problem of identifying the optimal operating condition for an active device will be analyzed, with particular interest in the maximization of the efficiency. In this context, a recently proposed design technique, based on large-signal low-frequency measurements will be applied to obtain accurate information on the transistor behavior. This technique will be also compared with conventional approaches (e.g., load pull) and validated with the realization of a prototype of a microwave power amplifier.

# PREFAZIONE

Negli ultimi anni, le tecnologie elettroniche per le comunicazioni hanno attraversato un continuo e pressante sviluppo a causa di diversi fattori. Da un lato, lo sviluppo della rete internet e dei sistemi informativi ad essa associati hanno causato tra le persone un crescente interesse nell'utilizzo di dispositivi in grado di garantire una costante connessione a questi servizi. Tale aspetto ha notevolmente incrementato la diffusione di dispositivi mobili, e tecnologie di nuova generazione, quali il 3G e il 4G/LTE, sono state perfezionate per soddisfare requisiti sempre più stringenti. D'altra parte, altri sistemi come i servizi di geolocalizzazione (e.g. GPS e GLONASS), inizialmente creati per scopi militari, sono oggi diffusi e comunemente adottati da un numero sempre maggiore di persone.

Se il mercato dei beni di consumo ha dato una significativa spinta alle tecnologie per le comunicazioni, altri settori hanno visto un enorme sviluppo. Ad esempio, i sistemi satellitari di osservazione della Terra (come il sistema COSMO-SkyMed per l'osservazione del bacino del Mediterraneo) svolgono oggigiorno un ruolo fondamentale nella prevenzione e nella gestione dei fenomeni naturali.

Gli esempi di sistemi di comunicazione precedentemente indicati sfruttano tecnologie per le microonde per la trasmissione di una grande quantità di informazioni, grazie alla disponibilità di bande di frequenza molto ampie. Questo implica necessariamente l'utilizzo di tecnologie ad alta potenza ed efficienza, in linea con i requisiti dei sistemi in cui sono inserite.

Quando questi aspetti vengono presi in considerazione, l'attenzione si focalizza sull'elemento fondamentale che determina le prestazioni di un circuito elettronico: il transistor. Nuove tecnologie basate su particolari semiconduttori quali l'Arseniuro di Gallio (GaAs) e il Nitruro di Gallio (GaN) si stanno rivelando come ottime soluzioni per la realizzazione di transistor con eccellenti prestazioni alle frequenze delle microonde e delle onde millimetriche. A causa della loro relativa immaturità rispetto a tecnologie ben assestate, come quella del Silicio, esse sono di grande interesse nell'ambito della ricerca, al fine di identificare le loro limitazioni e i loro margini di miglioramento.

Le attività di ricerca sviluppate durante il mio corso di dottorato si collocano in questo contesto. In particolare, l'attenzione è stata focalizzata sulla modellizzazione non lineare di transistor per applicazioni a microonde e sullo studio, oltre che sulla loro applicazione, di tecniche di progetto finalizzate all'ottimizzazione delle prestazioni di amplificatori di potenza.

Nel Capitolo 1, verranno brevemente riassunte le tecniche di modellizzazione non lineare di transistor. Quindi, l'attenzione si focalizzerà sul problema della dispersione in bassa frequenza che interessa le nuove tecnologie di dispositivi elettronici e che influenzano fortemente il loro comportamento dinamico e quindi le loro prestazioni ad alta frequenza. A questo scopo, sarà descritto un sistema di misura in bassa frequenza orientato all'analisi di questi fenomeni e che è stato largamente utilizzato durante tutta l'attività di ricerca.

In seguito, due diversi approcci di modellizzazione, compatto e comportamentale, verranno considerati. Durante il dottorato di ricerca, sono state analizzate e sviluppate due tecniche basate sul setup descritto nel Capitolo 1 che verranno presentate nei Capitoli 2 e 3 rispettivamente.

Infine, il Capitolo 4 sarà dedicato al progetto di amplificatori di potenza a microonde. In particolare, sarà analizzato il problema della identificazione della condizione operativa ottima per un dispositivo attivo, con particolare interesse alla massimizzazione dell'efficienza. In questo contesto, sarà applicata una tecnica di progetto recentemente proposta, basata su misure a grande segnale in bassa frequenza per ottenere informazioni accurate sul comportamento di un transistor. Questa tecnica sarà

confrontata con altri approcci convenzionali (e.g. load pull) e validata con la realizzazione di un prototipo di un amplificatore di potenza a microonde.

*Chapter 1*

# NONLINEAR MODELING OF ACTIVE DEVICES

In the last decades, great efforts have been spent in device technology for microwave electronics, by exploiting new semiconductor substrates, like gallium arsenide (GaAs) and gallium nitride (GaN), and new active devices have become more and more appealing in microwave electronics thanks to their high operating frequency and power densities, capable to satisfy more and more challenging requirements.

The development of new classes of operation for high-efficiency power amplifiers, commonly uses device nonlinearities to improve DC-to-RF power conversion [1-5]. Therefore, the use of models that accurately mimic actual devices also in those conditions is an importat tool for designers. However, this is still an open issue since conventional modeling solutions may not be eligible for new technologies. As an example, low-frequency dispersion, induced by the thermal and trap states of the device, affects new technologies with important degradation of device performance. These phenomena can be characterized by means of dedicated measurement setups (e.g., pulsed measurements [6, 7]) which can provide useful data although gathered in condition often different with respect to actual RF operation.

After a short description of the main devices that will be dealt with throughout this thesis, in this chapter the problem of nonlinear modeling will be briefly reviewed, considering the typical approaches oriented to nonlinear operation. Then, the attention will be focused on the *low-frequency dispersion* affecting microwave devices, and its effects on their behavior. Finally, a dedicated low-frequency setup for electron-

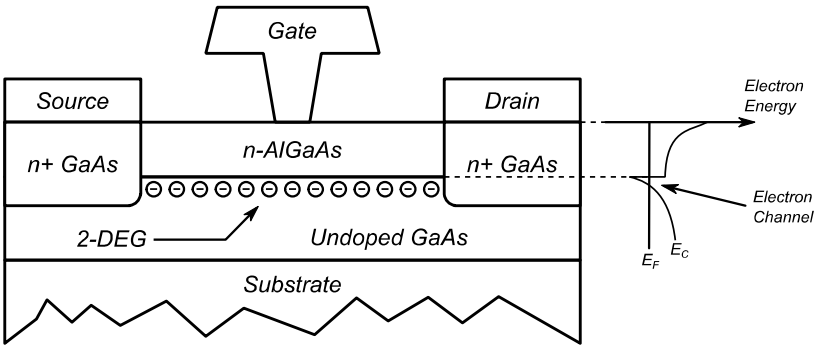


**Fig. 1.1** Cross section of an AlGaAs/GaAs HEMT.

device low-frequency characterization will be described, as it has been widely used for the activity presented in this work.

## 1.1. Field effect transistors for microwave applications

In microwave electronics, both bipolar and field effect transistors (FETs) can be exploited. Over the years, technology has been optimized in order to reach more and more ambitious specifications for microwave circuits as, for instance, high power gain at frequencies up to several gigahertz. For such a reason, new devices based on heterojunction structures have assumed a great importance in microwave electronics. In this field, FET devices represent one of the most promising technologies. An example is the high-electron mobility transistor (HEMT) [8,9] where the properties of a heterojunction are exploited to shift up the maximum operating frequency and the availability of free carriers in the channel, providing higher levels of current and, therefore, power.

For this thesis, these devices will be often considered, therefore it is convenient to briefly review their characteristics.

### *1.1.1. Gallium Arsenide HEMTs*

In Fig. 1.1 the cross-section of a GaAs HEMT is depicted [8,9]. The device has three terminals, i.e., *gate*, *drain* and *source*, and, as in other FET devices, when a positive voltage $V_{DS}$ is applied the current flows from drain to source (electrons move in the opposite direction) inside the *channel*, which lies in an undoped GaAs layer. The drain

current magnitude can be modulated by the voltage applied to the gate terminal, which is realized by a Schottky junction.

The key element of this device can be pointed out by observing the energy-band structure in proximity of the heterojunction AlGaAs/GaAs. Here, a wide-band gap material (i.e., AlGaAs) interfaces with a low-band gap material (i.e., undoped GaAs). In this condition, the conduction-band level decreases below the Fermi level, although for a limited area, in the undoped GaAs. The depth interested by this phenomenon is very limited, producing a very thin layer where the electron density is extremely high. This layer of electrons, which is referred to as two-dimensional electron gas (2-DEG), lies inside an undoped material, therefore charge mobility is very high, since scattering by impurities is not present. These characteristics guarantee high levels of drain current and very high operating frequency.

The most common HEMT type is the *depletion mode HEMT*[*]. In these devices, when no voltage is applied to the gate, the channel is open and current can flow through it by applying a voltage $V_{DS} > 0$. In normal operating condition, the gate terminal is inversely biased, i.e., $V_{GS} < 0$. This creates, in the underlying region, a charge-free area that can extend up to the undoped GaAs layer, according to the applied gate voltage. By varying its extension it is possible to modulate the electron density of the 2-DEG, and therefore the amount of current that flows inside the channel. When $V_{GS}$ is low enough, the electron density tends to zero and the channel becomes empty. This is called *pinch-off* condition and no current can flow through the device, defining its threshold voltage ($V_{TH}$). On the contrary, by increasing $V_{GS}$, the charge-free region pulls back, allowing the conduction inside the doped AlGaAs layer. Its mobility is lower because of the presence of impurities so the performance of the device tends to decrease. This is typically observed as a reduction of the device transconductance.

An evolution of the HEMT transistor is called *pseudomorphic HEMT* (pHEMT). This high-performance device is created by inserting a layer of undoped low band-gap material, as InGaAs, between the AlGaAs and GaAs layers. Since InGaAs has a different lattice constant with respect to GaAs, it produces a mechanical stress at the

[*] Also enhancement mode HEMTs do exist, but they are less used in microwave electronics and will not be dealt with here.

interface. However, for convenient levels of indium, this stress is not strong enough to create defects in the lattice. On the contrary, it increases electron mobility and improves charge confinement in the channel. These effects guarantee higher transconductance (i.e., power gain) and higher operating frequency with respect to HEMT devices.

### *1.1.2. Gallium Nitride HEMTs*

Gallium Nitride HEMTs constitute a relatively new technology for microwave electronics and its interest has rapidly grown in both academy and industries [10]. Their structure is similar to a GaAs HEMT, apart from the materials: AlGaN and GaN are used in place of AlGaAs and GaAs. The properties of these materials make GaN technology extreamely promising, allowing high-power density, high current and high breakdown voltage. The capability of handling high amount of power (approximately 5 W/mm versus 1 W/mm for GaAs technologies) is also due to the exploitation of excellent thermal conductors as substrate materials, like silicon carbide (GaN-on-SiC). Unfortunately, this makes such a technology very expensive, and this is why its diffusion is still pretty limited and new, cheaper substrate materials are explored today in order to reduce production costs [11, 12].

## 1.2. Nonlinear modeling of microwave FETs

A nonlinear model of a microwave device oriented to circuit design should be, at the same time, accurate, efficient and flexible. Accuracy is an important requirement since it guarantees reliable simulation results. Indeed, it is not possible to have a model able to perfectly mimic an actual device. As a matter of fact, sources of errors will be always present, being them related either to the model implementation (e.g., constitutive equations or equivalent circuits) which does not exactly fit the device behavior or to the measurements performed on the actual device to collect the data to be used for the model identification. On the contrary, a tolerance on the accuracy is actually acceptable and sometimes introduced by model developers: since two identical transistors do not exist, the typical approach adopted by foundries which provide models of their own devices is to measure a lot of samples and develop a model that fits their

"average" behavior. As a matter of fact, it is not infrequent for a foundry to provide data related to device tolerances. This plays an important role in a design flow to estimate statistical parameters (e.g., the yield).

Flexibility is intended as the capability for the designer to change some parameters of the model during the simulation phase, obtaining consistent results. Such parameters can be related to the operating condition of the device (e.g., the bias point) but also to some physical elements, as the gate length or the number of fingers. The latter allows to evaluate the use of devices with different layouts and, maybe, customize them to optimize circuit performance.

Actually, accuracy and flexibility are at odds with each others. As a matter of fact, although an accurate model can be identified for a precise operating condition and for a defined device, it is not trivial to maintain the same level of accuracy when different devices and operating conditions must be fitted.

Since a model is used in a simulation environment provided by a computer aided design (CAD) software, the computational efficiency is another important facet to be considered. For instance, in a nonlinear simulation (e.g., harmonic balance) the steady-state solution is obtained through iterative algorithms. Their ability to rapidly converge is obviously related to their own implementation but also to the properties of the models exploited for the simulation since they are evaluated at each iteration. As an example, the use look-up-table-based models could reduce the computational efficiency, because of the large-amount of data to be loaded in the computer memory and to be processed with interpolation and extrapolation algorithms. On the contrary, an analytical definition based on well-conditioned functions (e.g., bounded and differentiable) can be an extremely efficient solution.

These aspects are related to modeling choices and, firstly, to the selected approach. In the following sections a brief review of the two main approaches will be given, with particular reference to nonlinear models.

### *1.2.1. Compact models*

The first approach considered here is called *compact modeling* [13]. It is based on physical analyses and considerations on the device behavior by which it is possible to ob-

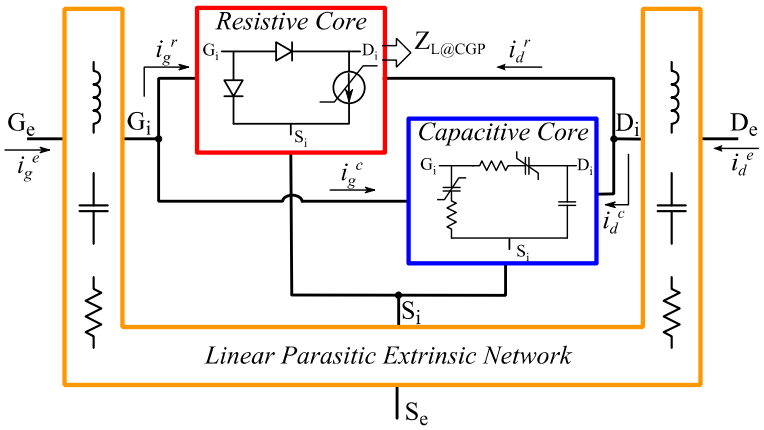


**Fig. 1.2** General topology of a nonlinear model of FET devices.

tain some equations and/or equivalent circuits capable of reproducing it [14-16]. In Fig. 1.2, the general topology of a nonlinear compact model is reported. It is possible to distinguish an *intrinsic* section and an *extrinsic* one. The intrinsic section corresponds to the actual device which is not directly accessible. Indeed, some access structures (e.g., metallizations, lines, bonding wires, etc) are used to make it possible contacting the device and distribute the signals to all its parts. These elements introduce delays and losses that are modeled by a *linear parasitic network* as reported in Fig. 1.2. It constitutes the most external shell which defines the extrinsic section of the device. The parasitic network can be implemented by lumped passive components identified by conventional procedures based on small-signal parameters directly measured on the device under specific operating conditions (e.g., cold-FET) [17,18]. The layout of the device, if available, can be also exploited to assess the parasitic network effects by using electromagnetic simulations, whose results can be directly used as a model [19-20] or to identify an equivalent lumped circuit [21].

The intrinsic device model can be split in two main blocks. The first one is the *resistive core*. Dedicated to reproducing the I/V characteristics of the actual device, it is typically assumed as a pure algebraic element, thus its behavior is frequency independent. It contains the *current generator* which reproduces, in typical operating conditions, the drain current $i_{D,R}$, and so it is responsible for the performance of the device in terms of output power and efficiency. Two diodes are exploited to describe the gate Schottky junction. In particular, under typical device operation, a gate-source diode

models its forward conduction while a gate-drain diode is exploited to reproduce its breakdown.

The *capacitive core* models the strictly-nonlinear dynamic effects of the device, thus determining the frequency dependence of the device performance (e.g., power gain). A typical implementation [9, 22, 23] in compact models consists of the definition of intrinsic nonlinear capacitances or, alternatively charge generators, dependent, in the most general form, on both the intrinsic voltages, i.e., $v_{GS,i}$ and $v_{DS,i}$. This description is indicated as *quasi-static* since, it assumes that the intrinsic device instantaneously responds to any change of the intrinsic signal. This approximation is typically adopted for models oriented to applications at frequencies well below the gain cut-off frequency of the actual device. If this is not the case, delay effects must be considered which are usually included by inserting time constants in the capacitive core model [23,24]. This is referred as *nonquasi-static* approach and guarantees accurate predictions for higher frequencies.

An advantage of compact modeling is the possibility to access every section of the device (e.g., intrinsic plane and current generator plane). This capability can be extremely useful for design purposes, when internal variables must be monitored to define the operating condition of interest [1, 2]. This aspect will be clarified in the next chapters.

As far as the identification steps are concerned, if conventional and well-established techniques to extract the capacitive core and the parasitic network models are available, the identification of an accurate model of the resistive core and, in particular, of the current generator is still, for some aspects, an open problem because of the presence, in actual devices, of *low-frequency dispersion phenomena*, which can cause important differences between DC and RF I/V [25-27]. This aspect will be the topic of the next paragraph.

Angelov's model [14] is one of the most diffused compact models for active devices in microwave electronics. It is oriented to GaAs transistors, although it can be properly adapted in order to fit other technologies [28-30]. It is based on a set of equations for each element of the model, selected to reproduce the physical characteristics of an actual device and with excellent convergence properties in nonlinear simulators.

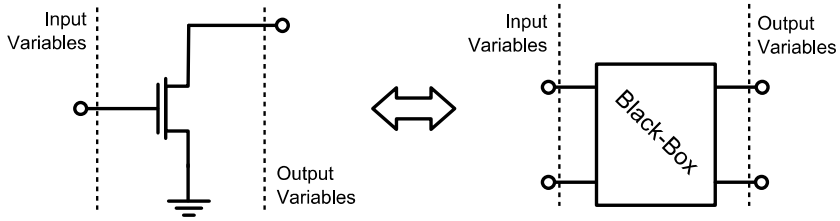


**Fig. 1.3** Schematic representation of the behavioral modeling approach.

Model parameters can be identified by a limited set of measurements performed in specific operating condition. Moreover, such a model can produce accurate results also outside the measured domain because of the consistency of the exploited equations. These aspects make the Angelov's model a very robust solution.

### *1.2.2. Behavioral models*

An alternative to compact modeling is *behavioral modeling* [31]. This approach consists of treating the object to be modeled as a "black-box" since just the external input and output signals are considered (see Fig. 1.3). This aspect implies the independence of the model definition from the technology or the circuit structure, therefore this approach has been largely considered at circuit level [32-34] due to the intrinsic advantages in terms of simulation time and convergence robustness.

In the last years, different solutions were defined to obtain predictive behavioral models starting from a set of measurements under different operating conditions to identify nonlinear functions used to describe the device nonlinearities with no need of the knowledge of the structure of the nonlinear device [35, 36]. Recently, the availability of setups for the device characterization in a large number of operating conditions, has inspired new measurement-based behavioral models, which are basically a set of measurements performed on an actual device, typically organized as *look-up tables* (LUTs). A simple example where this approach can be successfully used is represented by a power amplifier. Since it is typically designed for working under matching condition, a characterization under nearly matched operation can be considered exhaustive, so that a limited number of measurements are enough to completely describe its behavior. An equivalent compact model would be extremely difficult to

handle. Power amplifiers are complex circuits realized with several active devices and matching networks, which can severely affect simulation time and convergence. By using a behavioral model, the simulation reduces to a reading operation (and eventually some interpolations) of the LUT data.

At transistor level, the aforementioned advantages are not so evident, considering that the device actual operation must be exhaustively investigated and stored. If for a power amplifier this operation reduces to a pretty limited characterization since the operating condition is fixed, this is not true for a single transistor. For example, load and source terminations at the fundamental frequency and harmonics are not defined *a priori*, but chosen at design time. Therefore, the single device characterization oriented to its behavioral modeling must be exhaustive and, as a consequence, time-consuming. This consideration also impacts the cost of the instrumentation required to extract the model. High-frequency large-signal setups are often limited in both power and frequency. Measurements on devices characterized by high-power densities (e.g., GaN devices) could not be always feasible because of the power limitations of the instruments needed to implement high-frequency measurement setups. As far as the frequency band is concerned, the state of the art for large-signal network analyzer (LSNA), which constitutes the most complete system for high-frequency characterization since it provides time-domain data, is today limited by a total bandwidth of 67 GHz. This would be a strong limitation if data up to several harmonics need to be gathered. Moreover, the multi-harmonic tuners needed to vary harmonic impedances make these systems very expensive.

Another facet to be considered is that the large amount of data which must be collected to implement the model will be processed by the simulator. This operation could involve data interpolation to calculate the final solution, with associated big computational power.

At first blush, another important advantage of a behavioral model would be its accuracy. Indeed, this is only partially true. It is undisputed that when the model is exploited to simulate operating conditions that have been characterized, the accuracy of the results is the best possible since it corresponds to the measurement accuracy. However, some problems appear if the model is exploited outside the measured do-

main. When this is required, data are extrapolated. Since no physical constraints are applied to the behavioral model by the simulator, results are often inconsistent. This sensibly reduces the flexibility of the model, forcing the designer to use it only in the set of characterized operating condition.

Finally, an advantage of the behavioral approach is the possibility of protecting intellectual property, since no information related to device technology is directly accessible. However, this is also a great disadvantage for the designer: the impossibility of accessing to the internal parts of the model (e.g., the current generator plane) could result in a strong limitation for design purposes.

### 1.3. The low-frequency dispersion problem

In the previous paragraph, the resistive core has been introduced as a frequency independent part of the nonlinear model. As a matter of fact, some low-frequency nonlinear dynamic phenomena [7, 27] affect an electron device thus inducing a frequency dependence, although concentrated at low frequency. They are ascribed to thermal and trapping effects which are characterized by long time constants (i.e., seconds or milliseconds) [37-39] and are responsible for severe degradation of device performance at RF [40].

Self-heating is related to the dissipated power on the device, producing a temperature increase. In FETs, this induces a reduction of electron mobility, which is responsible for a reduction of the current flowing through the channel of the device.

The occupation state of traps is related to the electric field in the active region of the device, and then to the corresponding applied voltages [7, 41]. When a measurement of DC I/V characteristics is performed, thermal and trap states change according to the applied bias condition, that defines the dissipated power and the electric field in the device. Under large-signal operation, if the frequency is high enough, they cannot follow the signal dynamics, because of the high time constants they are characterized by. Thus, the thermal state remains fixed by the average voltages and currents and the AC output power the device is delivering to the load, whereas the trap state is *frozen* and determined, in first approximation, by the average voltage values applied to the intrinsic device.

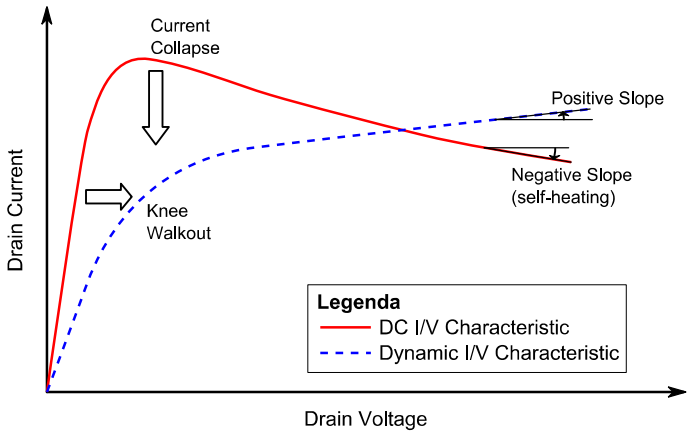


**Fig. 1.4** Qualitative example of the effects of low-frequency dispersion in active devices.

This produces a difference between DC and dynamic I/V characteristics, qualitatively reported in Fig. 1.4. Three main consequences can be observed:

- a reduction of the maximum drain current, indicated as *current collapse*;
- a variation of the slope in the linear region of the I/V characteristics which determines a deviation of the dynamic knee voltage with respect to the DC one;
- a change of the slope of the I/V characteristics in the saturation region, where the DC characteristics present a negative slope due to self-heating.

These effects can be also observed through small-signal measurements. Figure 1.5 reports an example of the Y-parameters measured with the setup proposed in [27] on a GaN HEMT. The frequency range of analysis is low enough to consider completely negligible the contribution of both reactive parasitic elements and intrinsic capacitances, therefore the device could be assumed "resistive". However, in the lower frequency range, it is evident a variation of the parameters up to a frequency of 500 kHz, ascribed to long-term memory effects mainly due to trapping phenomena. In particular, the output conductance significantly increases from 1.5 mS at low-frequency (i.e. 5 Hz) to about 7 mS. At frequencies above 500 kHz the parameters remain approximately constant.

The reported measurements put in evidence that there is a low-frequency band where long-term memory effects affect the behavior of the device, while above a cut-

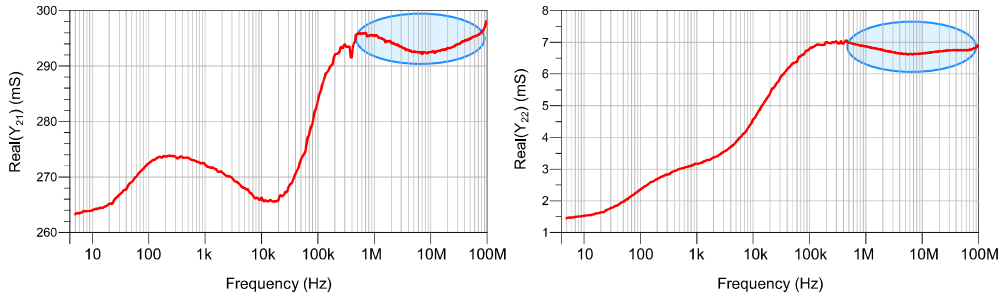


**Fig. 1.5** Y-parameters measured on a 0.25x8x125 μm² GaN HEMT biased in $V_{DS}$ = 20 V, $I_D$ = 200 mA. In the highlighted region, parameters can be assumed approximately constant.

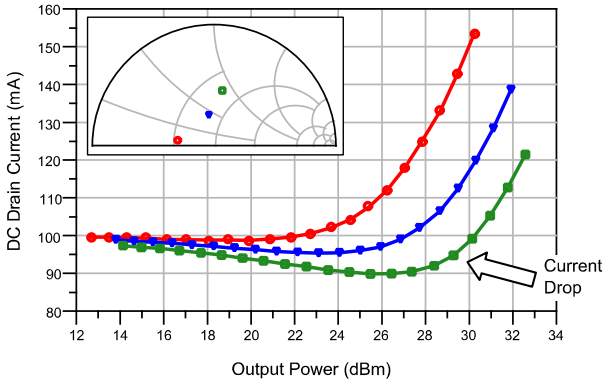


**Fig. 1.6** DC drain current vs output power measured on a 0.25x8x75-μm² GaN HEMT biased in class AB ($V_{DS}$ = 25 V, $I_D$ = 100 mA) at 10 GHz for three load impedances indicated in the inset: 26.7 + j2.80 Ω (red circles), 40.5 + j21.7 Ω (blue triangles), and 36.5 + j41.9 Ω (green squares).

off frequency that can be considered around 100 kHz-1MHz (in agreement with the time constants of some milliseconds/microseconds), the resistive core (i.e., the current generator) characteristics remains constant up to microwave frequencies.

In Fig. 1.6 another anomalous effect is highlighted. A power sweep measurement has been performed on a GaN device at 10 GHz under continuous wave (CW) operation. The device, biased in class AB ($V_{DS}$ = 25 V, $I_D$ = 100 mA), has been loaded with different impedances and the average drain current has been monitored during the sweep. The expected result should be a monotonic increase of the current as the output power becomes higher, due to the nonlinearities of the current generator operating under the selected bias condition. Indeed, by looking to the plots, it is evident that in the first part of the reported curves, where the device is still under a small-signal regime (that is, nonlinearities should be almost negligible), the average current de-

creases. The entity of this drop depends on the load impedance and can reach approximately 10% of the quiescent drain current (i.e., 100 mA). This phenomenon is considered [7, 41] the macroscopic evidence of fast-trapping phenomena. According to the hypothesis reported in the literature, when the electric field in the channel increases (i.e., when the intrinsic gate-drain voltage becomes higher), electrons can be trapped in deep-energy levels, assisted by the electric-field energy. This phenomenon is very fast and captured electrons cannot break free since the trap emission rate is related to thermal energy only, whose corresponding time constants are too low if compared with the RF signal period. Therefore, the number of carriers in the channel decreases, and the external effect is the reduction of the average drain current. This effect is typically more pronounced in newer technologies, like GaN, because they are affected by a higher number of defects in the lattice structure, especially at semiconductor interfaces, with respect to well-assessed technologies.

All the described phenomena make difficult to accurately reproduce the actual behavior of an active device starting from DC characteristics, which usually leads to important discrepancies in RF results. Thus, these effects must be taken into account if an accurate model of the device must be identified. A characterization based on RF measurements is not often convenient since, even if the macroscopic effects of low-frequency dispersion could be gathered, the variables they are dependent on (i.e., intrinsic voltages and currents) would be hidden by the capacitive core and parasitic element contributions. This makes their accurate characterization difficult and the need for dedicated measurement setup arises.

Pulsed measurements [6, 7, 42] are the typical approach for characterizing low-frequency dispersion in active devices. They allow to measure the dynamic I/V characteristics by applying short bias pulses from a starting bias point, covering all the operating regions of the device. Pulse timings are typically chosen in order to be short enough to not modify the thermal and trap occupation states but long enough to avoid the generation of harmonic components at too high frequencies, which can produce a non-negligible contribution of intrinsic capacitances.

Pulsed measurement techniques constitute a valid approach for low-frequency dispersion characterization, but they do not reproduce the device behavior under re-

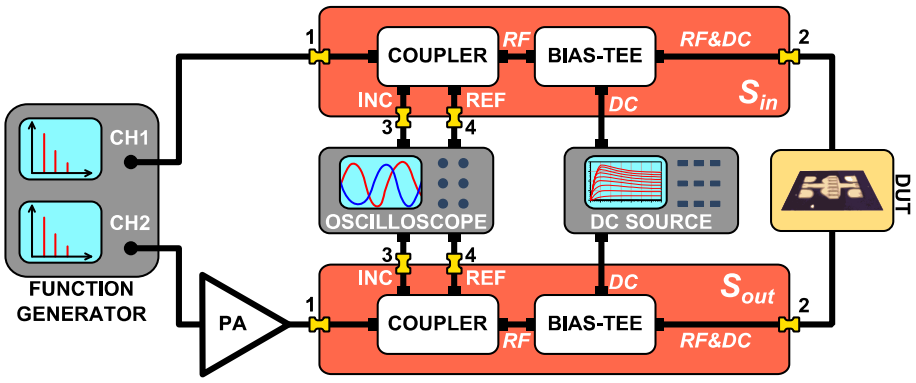


**Fig. 1.7** Block diagram of the low-frequency measurement setup.

alistic operating conditions. For instance, it has been recently demonstrated [43] that the effect of fast-trapping phenomena can be gathered by exploiting dedicated pulsing techniques, which could provide different results when the pulsing procedure is changed.

Therefore, the availability of measurements performed on an electron device under actual operating conditions is an important added value for modeling purposes. For such a reason, in this thesis the low-frequency measurement setup described in the following paragraph has been extensively adopted.

## 1.4. The low-frequency characterization setup

In Fig. 1.7 the low-frequency measurement setup that will be adopted throughout this thesis is shown [26]. The device under test (DUT) is excited with drain and gate incident waves generated by a 2-channel arbitrary function generator operating within [1 mHz – 120 MHz] whereas its bias point is imposed by a 20-W high-resolution (7 μV, 20 fA) and accurate DC source and coupled with the AC component by two wideband (200 kHz – 12 GHz) commercial bias-tees. A 30-W power amplifier (PA) may be adopted on the drain signal path when high-power devices have to be characterized. Reflected and incident waves, separated by two directional couplers (10 kHz – 400 MHz), are acquired by a four-channel oscilloscope (2 GSa/s) and the resulting data are post-processed by a mathematical procedure to obtain all the electrical quantities at the DUT plane.

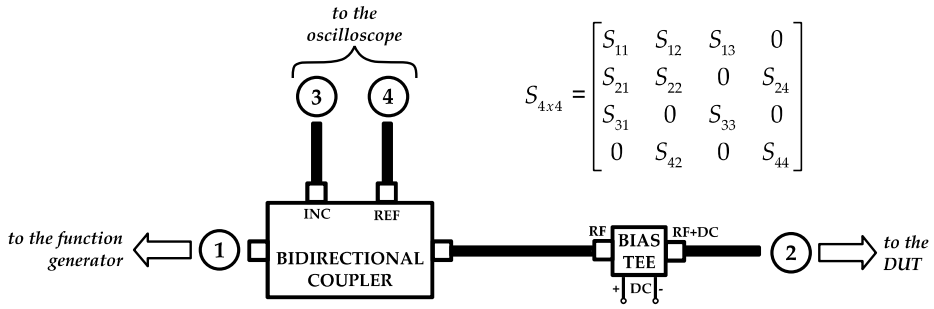


**Fig. 1.8** Structure of the signal paths characterized through small-signal parameters.

The system is conceived to operate within [200 kHz – 240 MHz], a bandwidth that can be considered as low-frequency for the largest part of microwave devices. In this frequency range of operation, all the setup components satisfy linear nondistortion conditions. This greatly simplifies the setup calibration procedure, which practically consists in the experimental characterization of the two four-port networks pointed-out in Fig. 1.8, in terms of their 4x4 S-parameters matrixes (i.e., $S_{in}$ and $S_{out}$). This is determined by a combination of two-port measurements performed with a vector network analyzer (VNA) operating in the frequency range of the low-frequency measurement setup. To further simplify the characterization procedure, some elements are assumed null by definition, e.g., the coupling effect between port 3 and port 4. This further simplifies the characterization procedure by introducing negligible errors.

As a matter of fact, the setup is a time-domain active load-pull system. By tuning the amplitudes and relative phases of the incident waves injected by the arbitrary function generator at both the fundamental frequency and harmonics and monitoring the response of the DUT, it is possible to synthesize any load condition under continuous wave (CW) operation. To clarify this point, an example is reported in Fig. 1.9. A 0.25x8x75-μm² GaN HEMT biased in class AB ($V_{DS,0}$ = 25 V, $I_{D,0}$ = 100 mA) has been characterized. The load impedance at only the fundamental frequency (i.e., 2 MHz) has been considered. A gate incident wave of amplitude $|A_{g,1}|$ = 0.55 V is applied while the drain incident wave is swept in terms of both its amplitude $|A_{d,1}|$ and relative phase φ. For the lowest level of $|A_{d,1}|$, its impact is almost negligible, therefore the

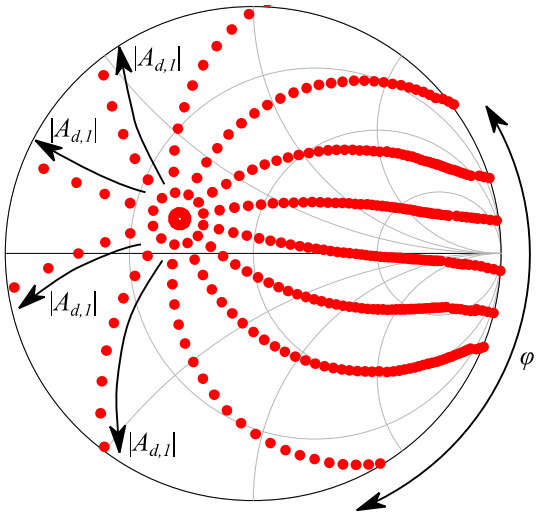


**Fig. 1.9** Example of load impedances (dots) synthesized by means of the low-frequency measurement setup on a 0.25x8x75 μm² GaN HEMT. The gate incident wave has an amplitude $|A_{g,1}|$ = 0.55 V. The drain incident wave has an amplitude $|A_{d,1}|$ such that 0.4 V ≤ $|A_{d,1}|$ ≤ $|A_{d,1}|^{max}$ where $|A_{d,1}|^{max}$ is the maximum value of $|A_{d,1}|$ for wich the synthesized impedance lies inside the Smith chart. The relative phase is 0° ≤ φ ≤ 330° with a step of 30°.

load impedance substantially coincides with the system impedance[†]. As long as $|A_{d,1}|$ increases, the synthesized impedance moves toward the boundary of the Smith chart, following a trajectory which depends on the relative phase φ. It is evident that, with the proposed setup, it is possible so synthesize any load condition of the Smith chart.

The typical operating frequency chosen for the setup is 2 MHz. This frequency is above the cut-off of low-frequency dispersion and, at the same time, the contributions of the reactive parasitic elements and its intrinsic capacitances are surely negligible. Therefore, the measurements performed with this technique allow to directly access the current generator plane of the device in actual operating condition, gathering information about the dynamic I/V characteristics of the DUT.

With this setup it is possible to characterize the effects of low-frequency dispersion. In Fig. 1.10, some load lines measured on a GaAs device are reported and compared with DC I/V characteristics. The measurements were performed considering a class-AB bias point (i.e., $V_{D,0}$ = 6 V, $I_{D,0}$ = 20 mA) and a sinusoidal gate incident wave at

[†] For this measurement, the power amplifier has been inserted on the drain path, so the center of the constellation depicted in Fig. 1.9 is equal to the output impedance of the amplifier, which does not perfectly correspond to the system impedance at the chosen fundamental frequency (2 MHz).

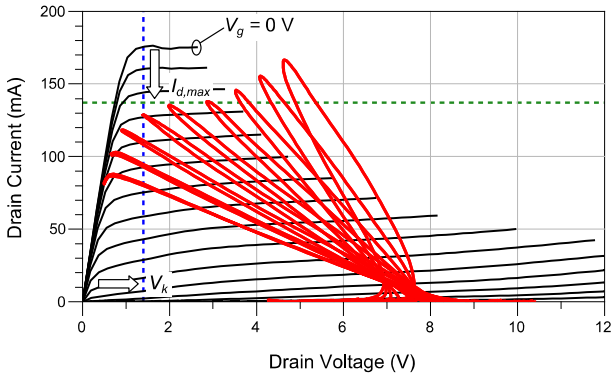


**Fig. 1.10** Load lines (red thick lines) measured for a 0.15x4x100 μm² GaAs pHEMT with the low-frequency setup at 2 MHz. The bias point is $V_{D,0}$ = 6 V, $I_{D,0}$ = 20 mA (class AB). The synthesized load impedance at the fundamental frequency varies between 3 Ω and 114 Ω. DC I/V characteristics are reported in thin black lines. Current collapse is pointed out as well as the dynamic knee voltage.

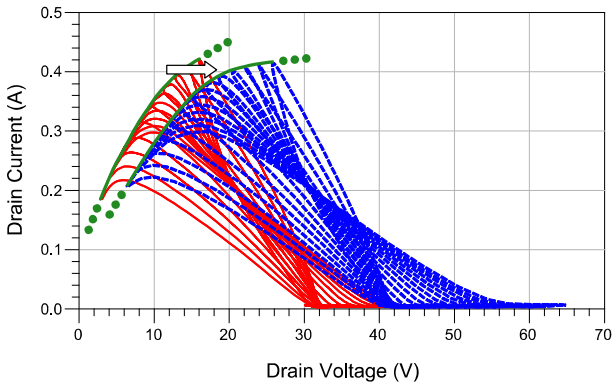


**Fig. 1.11** Load lines (red thick lines) measured for a 0.50x10x100 μm² GaN HEMT with the low-frequency setup at 2 MHz. For red solid lines the bias points is $V_{D,0}$ = 25 V, $I_{D,0}$ = 130 mA and the load impedance varies between 37 Ω and 158 Ω while for blue dashed lines the bias point is $V_{D,0}$ = 35 V, $I_{D,0}$ = 115 mA and the load impedance varies between 37 Ω and 190 Ω. The knee walkout as a function of the DC drain voltage is pointed out by the green thick solid lines.

2 MHz such that the gate voltage dynamically grazes the value of 0 V. By looking at the DC characteristic for $V_G$ = 0 V, it is evident the severe current collapse (about 23%) the load lines are affected by. It is also evident the difference in the slope of the dynamic I/V characteristics which is more pronounced with respect to DC ones. It is possible to evaluate the dynamic knee voltage $V_k$ that appears slightly higher than the DC corresponding value.

In Fig. 1.11 a similar set of measurements is reported for a GaN device. In this case, measurements were carried out in order to evidence the strong knee walkout

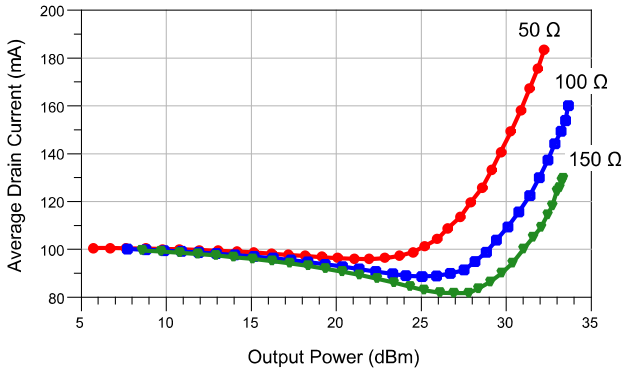


**Fig. 1.12** Average drain current as a function of the output power measured at 2 MHz on the 0.25x8x75 μm² GaN HEMT for a load impedance of 50 Ω (red circles), 100 Ω (blue squares), and 150 Ω (green triangles).

this technology is affected by. Two class-AB bias conditions were considered, with different DC drain voltage‡. The phenomenon of the knee walkout is evident, since the dynamic knee voltage seems to "follow" the quiescent drain voltage. This phenomenon, together with current collapse can produce a significant degradation of the device performance in RF operation (for instance, in terms of output power) that can be properly characterized with the proposed low-frequency setup. Moreover, this can give an immediate feedback on the quality of the device technology, and then if it is suitable for the design specifications.

It is worth noticing that the chosen frequency is also suitable to gather the effects of fast-trapping phenomena. In Fig. 1.12, a measurement performed on a GaN HEMT is reported, where the average drain current vs the output power is plotted. The typical drop of the current, observed under high-frequency operation, can be gathered also at the frequency of 2 MHz, since the period of the signal is short enough to allow trapped electrons to be released.

It is important to point out that the measurement system represented in Fig. 1.7 is composed of low-cost instrumentation if compared with the one necessary for high-frequency setups (e.g., LSNA); moreover, the system components, as the bias-tees and couplers, can be easily found in laboratories dedicated to microwave electronics.

‡ There is also a small difference in the quiescent drain current, although this is not critical for the result that is shown.

The harmonic response is not a problem since, operating at 2 MHz of fundamental frequency, up to sixty harmonics could be acquired with such a system. Moreover, at low-frequency the management of high levels of power is definitely easier. Indeed, the described setup handles output power levels up to 30 W (i.e., the limitation of the power amplifier on the drain signal path), which is an adequate value for a large part of microwave devices.

## 1.5. Aim of this thesis

In this thesis the low-frequency setup presented in the previous paragraph will be largerly exploited for two main purposes.

Firstly, the possibility of directly characterizing the current generator of an active device provides important data to be used for device model identification. This approach will be applied for two different cases. In the first one, an analytical compact model will be identified on the basis of large signal measurements only. In this case, it will be demonstrated how the exploitation of a set of low-frequency measurements can be sufficient to accurately extract the current generator description. The remaining part of the model (i.e., the capacitive core and the parasitic network) will be identified on the basis of time-domain high-frequency measurements under large-signal operation as well. The second example will propose a new approach to behavioral modeling where low-frequency measurements constitute a complete description of the current generator, overcoming some of the typical limitations the high-frequency setups commonly used for behavioral models.

Secondly, special attention will be paid on the exploitation of the low-frequency setup for circuit design purposes. In particular, the possibility of imposing the desired operating condition at the current generator plane will be used and it will be demonstrated how this can provide accurate information about the optimum operating condition at high frequency, through the application of a power amplifier design methodology based on the nonlinear embedding technique [44]. The harmonic control of the intrinsic waveforms will lead to deeply investigate high-efficiency operation and to optimize the power amplifier design.

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*Chapter 2*

# COMPACT MODELING THROUGH TIME-DOMAIN LARGE-SIGNAL MEASUREMENTS

In this chapter, an approach for nonlinear compact modeling based on the exploitation of time-domain large-signal measurements is described.

The use of such measurements implies some remarkable advanges. First of all, identification data refers to the device behavior in its typical operating condition. Therefore, effects as low-frequency dispersion [1, 2] can be gathered and directly included in the identified model.

Secondly, a small number of measurements can provide a lot of information related to device dynamics. As an example, if a class-AB operating condition is considered and enough input power is delivered to the device, the measured I/V loci can involve all the regions of the device characteristics (linear, saturation and interdiction regions). When the compact modeling approach is based on an analytical model providing a good description of the actual-device behavior, such data can be sufficient for its identification.

On the basis of these considerations, this approach will be considered for the identification of the model for a 0.15-μm, 400-μm periphery GaAs pHEMT. To this end, the Angelov's model [3, 4] will be used, which is dedicated to such a technology and each constitutive part, i.e., resistive core, capacitive core and parasitic network, can be easily split for a separate identification. This significantly simplifies the extraction technique, since it is possible to use a dedicated set of measurements for each element.

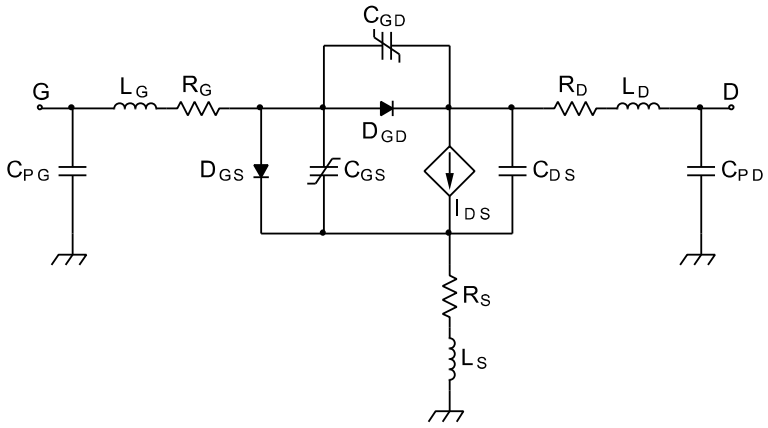


**Fig. 2.1** Model topology adopted for the proposed identification technique.

## 2.1. Description of the identification procedure

In Fig. 2.1, the topology adopted for the 400-μm periphery 0.15-μm GaAs pHEMT is depicted. It corresponds to the Angelov's model, apart for the insertion of two grounded capacitances, $C_{PG}$ and $C_{PD}$, as a part of the parasitic network.

The identification has been split in two steps [5]. As a first one, the resistive parasitic elements and the current generator parameters have been optimized. Their behavior has been considered only above the cut-off frequency of the dispersive effects [6]. To this purpose, large-signal low-frequency measurements have been carried out by using the setup described in Chapter 1. As a drawback, the model will not be able to reproduce DC characteristics, but will be oriented to the design of circuits under large-signal operation (e.g., power amplifiers).

The second identification step is focused on the reactive elements of the model, i.e., the linear reactive parts of the parasitic network and the nonlinear intrinsic capacitances. They will be identified on the basis of high-frequency large-signal measurements performed by means of an LSNA. Measured data provide vector information on voltages and currents at the device reference planes under actual operating conditions which are successively used in the optimization of the Anglelov's functions. To this aim, two cases will be considered:

- *1-tone measurements* [5] up to several dB of gain compression. In this case, the identified model will be oriented to strong non-linear operation, in particular close to power saturation.
- *Intermodulation measurements* [7]. Such data can be exploited for the identification of a model oriented to quasi-linear operation, that is to obtain accurate predictions of the device for highly-linear power amplifier design.

In the next part of the Chapter these two steps will be described and the proposed approach will be validated.

## 2.2. Identification of the current-generator model through low-frequency large-signal measurements

Angelov's model describes the current generator by using the following equation[§] [4]:

$$I_{DS} = I_{PK0} \cdot \left(1 + \tanh\left(\Psi\right)\right) \cdot \tanh\left(\alpha \cdot V_{DSi}\right) \cdot \left(1 + \lambda V_{DSi}\right) \tag{2.1}$$

where

$$\psi = P_{1m} \cdot \left(V_{GSi} - V_{pkm}\right) + P_2 \cdot \left(V_{GSi} - V_{pkm}\right)^2 + P_3 \cdot \left(V_{GSi} - V_{pkm}\right)^3 \tag{2.2}$$

$$\alpha = \alpha_R + \alpha_S \cdot \left(1 + \tanh\left(\psi\right)\right) \tag{2.3}$$

$$P_{1m} = P_1 \cdot \left(1 + \frac{B_1}{\cosh^2\left(B_2 \cdot V_{DSi}\right)}\right) \tag{2.4}$$

$$V_{pkm} = V_{pks} - \Delta V_{pks} + \Delta V_{pks} \cdot \tanh\left(\alpha_S \cdot V_{DSi}\right) \tag{2.5}$$

These equations contain a set of parameters to be determined in order to fit measurements. Each function is oriented to describe a specific region of the I/V characteristics. As an example, the function $\psi$ (Equation 2.2) models the shape of the transconductance as a function of the intrinsic gate-source voltage $V_{GSi}$, while the function $\alpha$ (Equation (2.3)) defines the slope of the DC I/V characteristics in the transition between the linear and the saturation region.

[§] Equations have been simplified by ignoring some parameters (e.g., breakdown description) that were not considered in this case study.

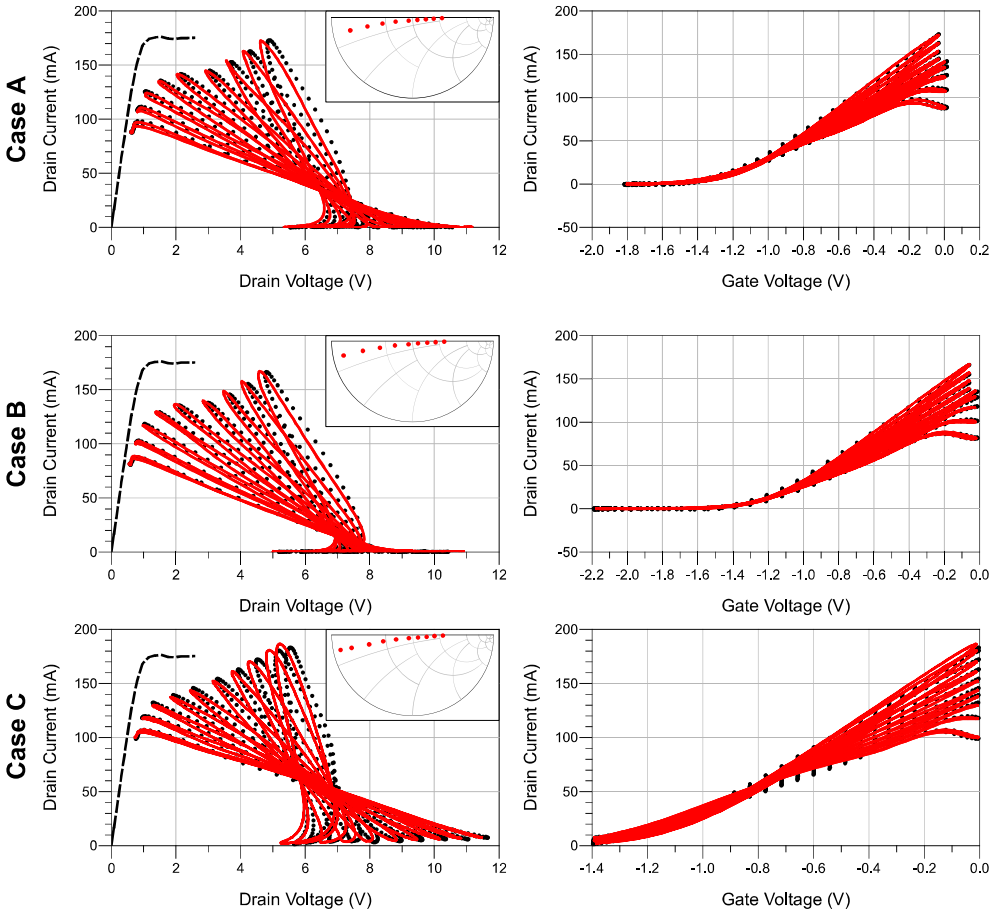


**Fig. 2.2** Measured (dots) and simulated (solid lines) load lines at 2 MHz. The bias points are: $V_{DS}$ = 6 V, $I_D$ = 42 mA (case A), $V_{DS}$ = 6 V, $I_D$ = 19 mA (case B), and $V_{DS}$ = 6 V, $I_D$ = 70 mA (case C). In the insets, the load impedances synthesized at 2 MHz for each case are shown. Cases A and B have been used for model optimization. DC characteristic at $V_{GS}$ = 0 V is shown (dashed line) for comparison.

The use of DC measurements for the identification of the parameters is the typical approach, since data corresponding to each region of the I/V characteristics (e.g., linear and saturation regions) can be easily gathered. However, as mentioned, the goal of this work is to accurately fit the RF behavior, thus low-frequency measurements for different bias-points have been considered instead. It must be pointed out that a single time-domain measurement allows to obtain a large amount of data relative to I/V characteristics, from pinch-off to saturation. As a consequence, the use of a limited number of load lines can provide a lot of information to be exploited for the determination of the model parameters.

In Fig. 2.2 an example is depicted. The selected device is biased under class-AB operation and some load lines measured at 2 MHz are reported. The amplitude of the gate voltage waveform has been set so that it grazes the value of 0 V. The DC characteristic for $V_{GS}$ = 0 V is also reported for comparison, showing the important effects of low-frequency dispersion. It is evident that the measured domain provides data for every region of the I/V characteristics, which are sufficient for parameter identification through numerical optimization. The latter has been carried out by using the ADS dedicated tool, where goals were defined for both the measured drain current and voltage in terms of their harmonic components up to the third order.

The conduction of the Schottky junction was prevented in the measurements considered for the identification; therefore, since no gate current flows in the device, it was not included in the optimization. In any case, to complete the model of the resistive core, diode parameters were determined through conventional DC data.

Cases A and B reported in Fig. 2.2 were chosen to identify the model parameter values, while case C, which corresponds to a different bias condition, was selected for the validation of the results. In each case the agreement with measured data is remarkable, confirming the robustness of the identification procedure.

## 2.3. Identification of linear and nonlinear dynamic elements

In the Angelov's model, the capacitive core is defined with three capacitances, i.e., $C_{GS}$, $C_{GD}$, and $C_{DS}$, as indicated in Fig. 2.1. $C_{DS}$ is considered as a linear element, whereas the following nonlinear functions [4] describe the capacitances $C_{GS}$ and $C_{GD}$:

$$C_{GS} = C_{GSPI} + C_{GS0} \cdot \left(1 + \tanh\left(\varphi_1\right)\right) \cdot \left(1 + \tanh\left(\varphi_2\right)\right) \tag{2.6}$$

$$C_{GD} = C_{GDPI} + C_{GD0} \cdot \left[\left(1 - P_{111} \tanh\left(\varphi_3\right)\right) \cdot \left(1 + \tanh\left(\varphi_4\right)\right) + 2P_{111}\right] \tag{2.7}$$

where:

$$\varphi_1 = P_{10} + P_{11} \cdot V_{GSi} + P_{111} \cdot V_{DSi} \tag{2.8}$$

$$\varphi_2 = P_{20} + P_{21} \cdot V_{DSi} \tag{2.9}$$

$$\varphi_3 = P_{30} - P_{31} \cdot V_{DSi} \tag{2.10}$$

$$\varphi_4 = P_{40} + P_{41} \cdot V_{GDi} - P_{111} \cdot V_{DSi} \tag{2.11}$$

Both equations (2.6) and (2.7) include physical data, as the capacitance value at pinch-off (i.e., $C_{XXPI}$) and their maximum variation as a function of the intrinsic voltages (i.e., $C_{XX0}$). The hyperbolic tangent functions reproduces the typical limited shape of intrinsic capacitances, modulated by the terms expressed in equations (2.8-11).

The parameters can be determined by using time-domain measurements performed at a frequency such that the contributions of reactive elements is sufficiently high. As a matter of fact, the same advantage described for the low-frequency measurements is exploited: the availability of current and voltage waveforms allow to evaluate and then optimize model parameters over a large set of dynamic conditions. Therefore, since the current generator has been already determined and is assumed frequency independent, only the parameters related to reactive elements must be optimized in order to fit high-frequency data.

As indicated in paragraph 1.1, two approaches have been considered, oriented to two different applications.

### *2.3.1. Exploitation of large-signal 1-tone measurements*

An identification based on large-signal measurements [5] up to several dB of gain compression is now considered. Figures 2.3 and 2.4 shows the measurements used for the numerical optimization compared with simulation results. The device is biased in class AB ($V_{DS}$ = 6 V, $I_D$ = 40 mA) and an input power sweep has been performed for two different load conditions at a frequency of 10 GHz. The optimization has been carried out to fit the current and voltage waveforms at the device extrinsic planes by defining goals up to the third harmonic. A good agreement was achieved up to 4 dB of gain compression, i.e., near the output power saturation.

It is remarkable that, since the identification is performed with high-frequency time-domain data, it constitutes by itself a preliminary validation of the developed model. However, additional measurements have been carried out and compared with simulations for further validation. An example is reported in Fig. 2.5 where a single-tone measurement at 10 GHz is considered for a different bias point ($V_{DS}$ = 6 V, $I_D$ = 20 mA). The results are still in good agreement with measured data.

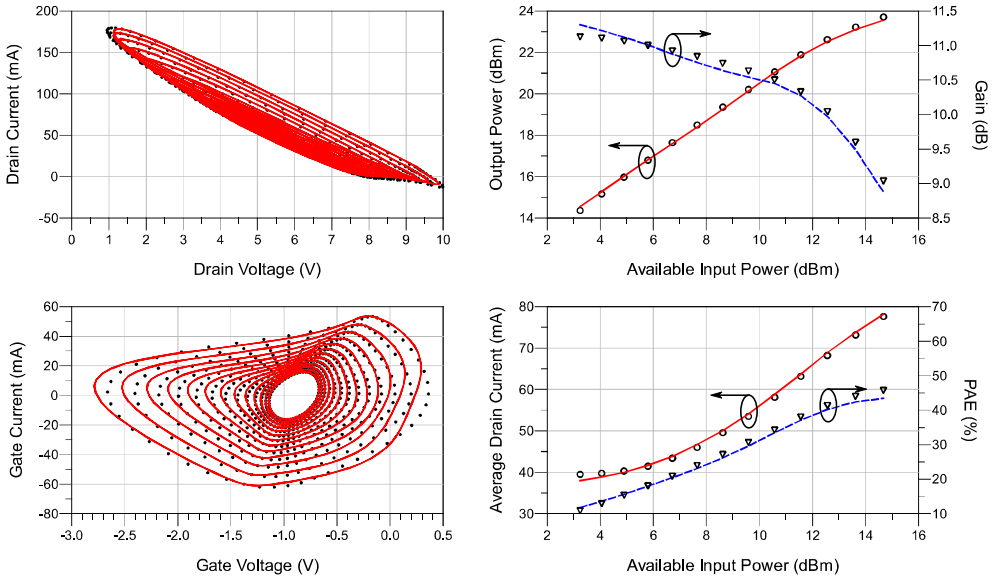


**Fig. 2.3** Comparison between 1-tone high-frequency measurements (symbols) and simulation data (lines) at 10 GHz. The bias point is $V_{DS}$ = 6 V, $I_D$ = 40 mA, the source impedance is 50 ohm and the load impedance is 47.7 + j6.5 ohm.

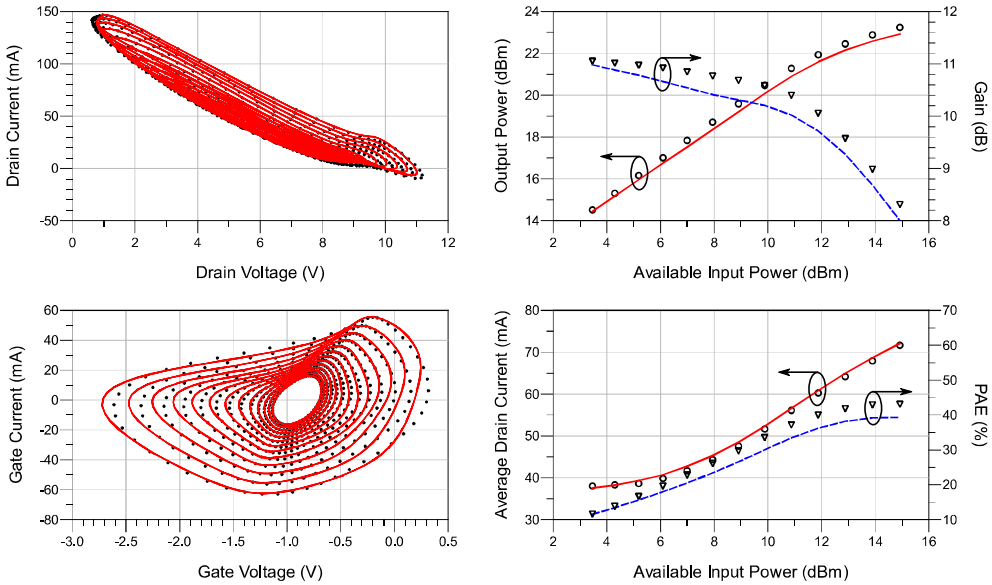


**Fig. 2.4** Comparison between 1-tone high-frequency measurements (symbols) and simulation data (lines) at 10 GHz. The bias point is $V_{DS}$ = 6 V, $I_D$ = 40 mA, the source impedance is 50 ohm and the load impedance is 70.0 + j10.3 ohm.

To evaluate the accuracy of the developed model in predicting the linearity of the device, intermodulation measurements performed by using an LSNA have been used. In Fig. 2.6, a comparison between the measured and simulation data is shown.

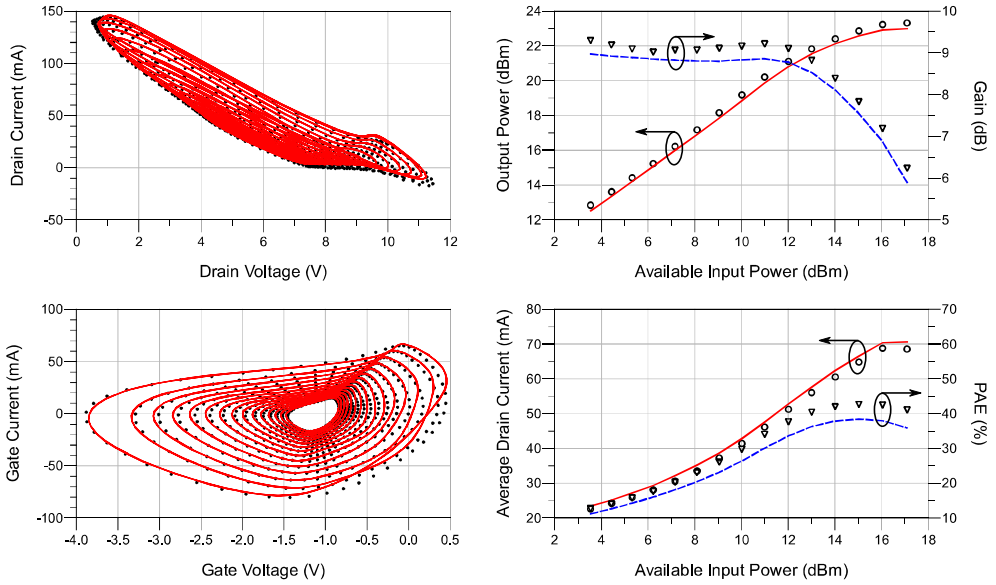


**Fig. 2.5** Comparison between 1-tone high-frequency measurements (symbols) and simulation data (lines) at 10 GHz. The bias point is $V_{DS}$ = 6 V, $I_D$ = 20 mA, the source impedance is 50 ohm and the load impedance is 70.0 + j10.3 ohm.

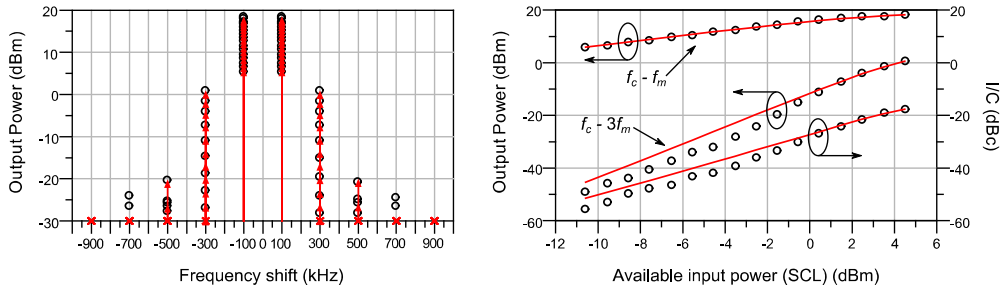


**Fig. 2.6** Comparison between intermodulation measurements (symbols) and simulation data (solid red lines). The bias point is $V_{DS}$ = 6 V, $I_D$ = 70 mA, the source impedance is 50 ohm and the load impedance is 59.0 – j7.0 ohm.

The bias point is $V_{DS}$ = 6 V, $I_D$ = 70 mA, the carrier frequency $f_o$ is 5 GHz, while the modulating frequency $f_m$ is 100 kHz. The available input power has been swept between -11 dBm and 5 dBm. Simulation results are fairly accurate, in particular for the higher levels of input power, which is consistent with the application the model was identified for.

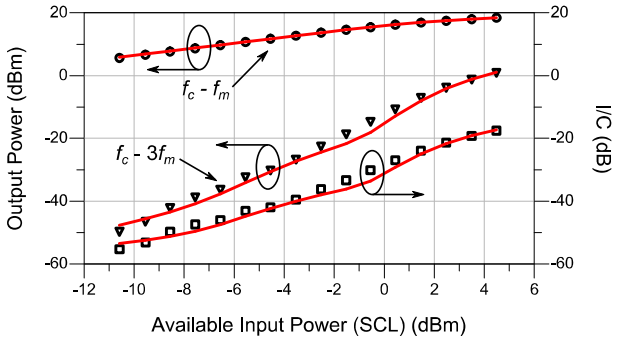


**Fig. 2.7** Intermodulation measurements (symbols) and simulations (solid lines) after the optimization procedure: $V_{DS}$ = 6 V, $I_D$ = 70 mA, $f_c$ = 5 GHz, $f_m$ = 100 kHz. Output power at $f_c - f_m$ (circles), $f_c - 3f_m$ (triangles) and I/C ratio (squares). The load impedance is 59.0 - j7.0 ohm.

### 2.3.2. *Exploitation of intermodulation measurements*

The exploitation of time-domain intermodulation measurements for the identification of the model allows its optimization for better linearity predictions [7].

A vector intermodulation measurement provides a lot of information about device dynamics since many harmonics can be simultaneously gathered. Therefore, a small number of measurements can be sufficient to accurately determine the model parameters.

To this end, the intermodulation measurement exploited for validation purposes in the previous identification procedure (carrier frequency $f_c$ = 5 GHz, modulating frequency $f_m$ = 100 kHz, input power from -11 dBm to 5 dBm, load impedance 59.0 – j7.0 ohm) was considered here for the identification of the reactive elements of the model, by keeping constant the parameters related to the current generator description, coherently with the hypothesis of its frequency independence.

The optimization procedure focused on the harmonic components above a minimum level of input power (i.e. -40 dBm) to avoid the influence of measurement noise on parameter identification. The low-frequency components have been ignored, since related to the current generator behavior only.

Measurement data and simulations are compared in Fig. 2.7. The accuracy of the model is increased with respect to Fig. 2.6 and the model fits very well the device behavior, both in terms of output power and I/C ratio.

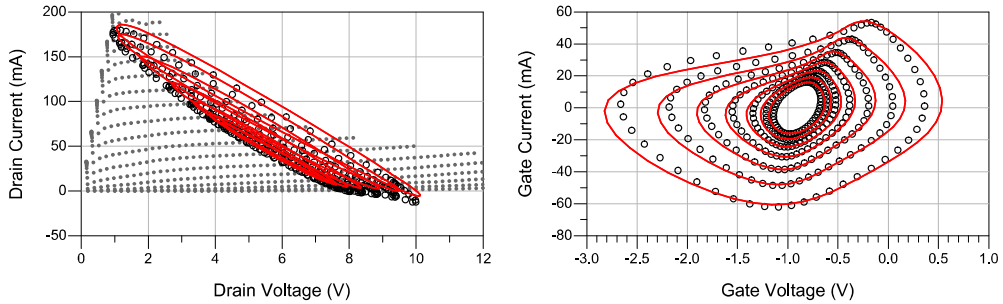


**Fig. 2.8** Measurements (symbols) and simulations (solid lines): $V_{DS}$ = 6 V, $I_D$ = 40 mA, $f$ = 10 GHz. DC output characteristics are shown in grey dots for comparison. The load impedance at the DUT plane is 47.7 + j6.5 Ω. Available input power has been swept between 3 dBm and 15 dBm.

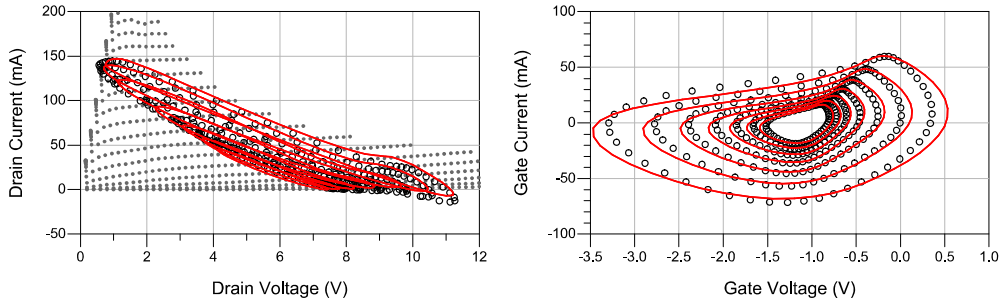


**Fig. 2.9** Measurements (symbols) and simulations (solid lines): $V_{DS}$ = 6 V, $I_D$ = 20 mA, $f$ = 10 GHz. DC output characteristics are shown in grey dots for comparison. The load impedance at the DUT plane is 70.1 + j10.4 Ω. Available input power has been swept between 3 dBm and 15 dBm.

To verify the robustness of the identification procedure, a validation in terms of 1-tone large-signal measurements has been performed, by using the data exploited for the identification of the model described in section 2.3.1.

In Figs. 2.8 and 2.9, some comparisons between measurements and simulations are shown. Despite the use of few intermodulation measurements (i.e., single bias and loading condition), the results provided by the model are in fair agreement with measurements. It is worth noticing the pretty good prediction of the gate current which is an important indicator of the accuracy of the capacitive part of the model. Indeed, apart from linear parasitic element influence, the gate current is mainly determined by the $C_{GS}$ and $C_{GD}$ capacitances (diode contributions are negligible in this case).

It is quite interesting the good fit of the model even for the highest power levels, which were not considered in the IMD measurement exploited in the identification phase. This is a consequence of the fact that the model definition, oriented to GaAs devices as in this case study, is implemented with functions that mimic very well the typical device behavior and then few measurements are sufficient for the robust identification of their parameters.

## 2.4. Conclusion

In this chapter, a nonlinear analytical model of a 0.15-μm GaAs pHEMT has been identified by considering an approach based on time-domain large-signal measurements.

To this end, the Angelov's model has been used, providing some great advantages. Firstly, it is oriented to GaAs FETs and implemented through analytical functions which well reproduce the typical characteristics of such a type of devices. Moreover, it allows to separate the identification of the resistive core from the capacitive one, by using dedicated sets of measurements.

For the current generator model, low-frequency large-signal measurements have been exploited, giving priority to fit its behavior above trap cut-off frequency with respect to the DC one, thus gathering the effects of low-frequency dispersion. The measurement data used for the model identification were carried out at 2 MHz for different bias conditions under class-AB operation and different load impedances. The collected data cover a wide region of the current generator I/V characteristics, which is necessary for a proper identification of its model parameters.

The capacitive core has been identified by using high-frequency time-domain measurements performed by using an LSNA. In particular, two approaches have been considered. In the first one, 1-tone power-sweep measurements were used, up to several dB of gain compression, with the aim of extracting a model able to predict device performance close to the saturated output power. For the second approach, time-domain intermodulation measurements were considered, in order to optimize the device model for highly-linear power amplifier operation.

In both cases, as for the identification of the current generator, the number of measurements involved in the parameter optimization is pretty limited, although sufficient to cover the different regions of the I/V loci.

The validation of the developed models showed a good agreement with measurements, also if different operating conditions with respect to the ones exploited for the identification phase were used.

Results confirm the robustness and the advantages of this modeling approach which is also related to the availability of a consistent description of the electron device provided by the Angelov's model.

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*Chapter 3*

# BEHAVIORAL MODELING OF GaN HEMTS

In Chapter 1 the problems of behavioral modeling oriented to transistors have been discussed. In this Chapter a new technique is presented, which can be defined as a *mixed* approach since involves both behavioral and compact techniques [1].

Considering the topology of a nonlinear transistor model, three different parts can be distinguished, i.e., the resistive core, the capacitive core and the parasitic network. For each part several identification techniques can be found in literature. As far as the capacitive core and the parasitic network are concerned, well-assessed techniques are available [2-9]. The resistive core is actually the most complex element to be described, in particular for recent technologies where the impact of low-frequency dispersion can induce nonlinear dynamic phenomena whose characteristics are still debating in the scientific community (e.g., fast-trapping phenomena [10-23]).

On these bases, the idea of the following approach comes out. Firstly, for both the capacitive core and the parasitic network a compact description is used, since an accurate identification of these parts can be performed by using conventional techniques. On the contrary, the behavioral approach is reserved to the resistive core and, in particular, to the current generator. As a matter of fact, its characterization can be obtained by using the low-frequency setup described in Chapter 1, easily measuring a lot of different operating conditions and gathering both thermal and trapping effects. Such a system is not affected by frequency and power limitations as high-frequency setups, since at few megahertz those problems can be easily overcome. Therefore, an exhaustive characterization is possible.

Another advantage of the *mixed* approach is the possibility of accessing each section of the model, and in particular the current-generator plane which is of great importance for circuit design techniques [13, 14].

The main drawback of this approach is that low-frequency measurements, once collected, must be post-processed in order to obtain proper datasets to be used in the simulation environment.

In the following paragraphs a detailed description of this new approach will be presented and discussed.

### 3.1. Definition of the current-generator behavioral model

Above the cut-off of low-frequency dispersion [15, 16], the transistor currents at the current-generator plane can be expressed, in the most general form, by

$$\begin{bmatrix} i_{G,R} \\ i_{D,R} \end{bmatrix} = \begin{bmatrix} f_G\left(v_{GSi}, v_{DSi}, X_{\vartheta,0}, X_{T,0}\right) \\ f_D\left(v_{GS,i}, v_{DSi}, X_{\vartheta,0}, X_{T,0}\right) \end{bmatrix} \tag{3.1}$$

where $i_{G,R}$ and $i_{D,R}$ are the instantaneous currents at the Schottky junction and current generator respectively, $v_{GSi}$ and $v_{DSi}$ are the instantaneous voltage values at the intrinsic device. $X_{\vartheta,0}$ and $X_{T,0}$ are state variables describing the states of thermal and trapping effects which are *frozen* due to their inability to follow the signal dynamics under actual operating conditions. In particular, since the case temperature and the intrinsic voltages completely define the device electrical and thermal state, $X_{\vartheta,0}$ and $X_{T,0}$ can be expressed, without introducing any approximation, as nonlinear functions of the voltage phasors and case temperature $T_C$:

$$\begin{bmatrix} X_{\vartheta,0} \\ X_{T,0} \end{bmatrix} = \begin{bmatrix} h_\vartheta\left(T_C, V_{GSi,0,} V_{GSi,1}, ..., V_{GSi,n}, V_{DSi,0,} V_{DSi,1}, ..., V_{DSi,n}\right) \\ h_T\left(T_C, V_{GSi,0,} V_{GSi,1}, ..., V_{GSi,n}, V_{DSi,0,} V_{DSi,1}, ..., V_{DSi,n}\right) \end{bmatrix} \tag{3.2}$$

where $n$ is the practically limited number of the spectral components. As a consequence, the device currents can be reformulated as

$$\begin{bmatrix} i_{G,R} \\ i_{D,R} \end{bmatrix} = \begin{bmatrix} p_\vartheta\left(T_C, V_{GSi,0,} V_{GSi,1}, ..., V_{GSi,n}, V_{DSi,0,} V_{DSi,1}, ..., V_{DSi,n}\right) \\ p_T\left(T_C, V_{GSi,0,} V_{GSi,1}, ..., V_{GSi,n}, V_{DSi,0,} V_{DSi,1}, ..., V_{DSi,n}\right) \end{bmatrix} \tag{3.3}$$

where the explicit dependence on $v_{GSi}$ and $v_{DSi}$ has been removed since the instantaneous voltages can be conveniently expressed in terms of their phasors. In the particular case where both the case temperature $T_C$ and the bias condition ($V_{GSi,0}$, $V_{DSi,0}$) are constant, equation (3.3) reduces to

$$\begin{bmatrix} i_{G,R} \\ i_{D,R} \end{bmatrix} = \begin{bmatrix} g_{\vartheta}\left(V_{GSi,1},\ldots,V_{GSi,n},V_{DSi,1},\ldots,V_{DSi,n}\right) \\ g_{T}\left(V_{GSi,1},\ldots,V_{GSi,n},V_{DSi,1},\ldots,V_{DSi,n}\right) \end{bmatrix} \tag{3.4}$$

The number of voltage harmonics to be controlled in (3.4) depends on the specific application. Nevertheless, when the transistor is used at its proper operating frequencies, there is an intrinsic shorting effect at harmonic frequencies due to the transistor capacitances. As a consequence, when harmonic tuning is not involved, controlling the voltage phasors only at the fundamental frequency in (3.4) is adequate to guarantee a high level of accuracy. This is an important feature of this approach since it greatly simplifies the identification procedure.

In addition, when harmonic tuning has to be performed, the principle of harmonic superposition [17] could be applied to (3.3) and (3.4). Such a choice could represent a good solution to limit the amount of data and measurement time. Nevertheless, when the harmonic superposition is not applicable, i.e., the number of voltage harmonics to be controlled in (3.3) and (3.4), and, consequently, the complexity of constitutive model equations increases, the proposed modeling approach still provides a great advantage with respect to the existing behavioral models. In fact, by performing measurements at few megahertz with the low-frequency setup to characterize the current generator, it is possible to control up to 60 harmonics, by exploiting a low-cost arbitrary function generator, without the need for expensive harmonic tuners.

The model structure description that has been given so far is actually technology independent. To prove its capabilities and verify its limitations, it has been applied for a 0.25x8x75 μm² GaN-on-SiC HEMT since modeling GaN transistors still represents an important challenge. Some foundry specifications for this technology are reported in Table 3.1.

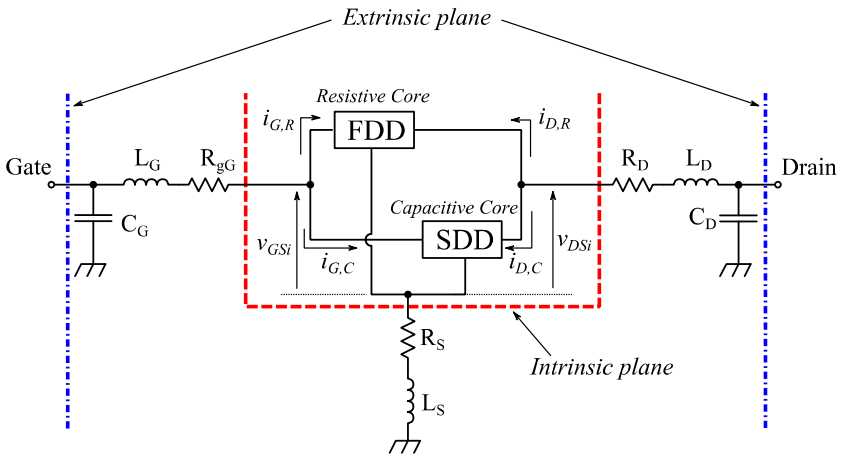



**Fig. 3.1** Topology of the proposed model.

TABLE 3.1. 0.25-μm GAN HEMT TECHNOLOGY SPECIFICATIONS

| *Quantity* | *Value* |
|---|---|
| *Breakdown Voltage* | -70 V |
| *Pinch-off Voltage* | -3 V |
| $I_{DSS}$ | 700 mA/mm |
| *Saturated Output Power* | 5 W/mm |

## 3.2. Model topology and implementation in CAD environment

Equation (3.4) accurately describes the behavior of the transistor current generator, but to obtain a complete device model, also the parasitic network [3, 7, 9] and the capacitive core [2, 4-6, 8] must be identified and implemented. As mentioned, a compact approach has been exploited for these elements.

In Fig. 3.1 the model topology implemented in the CAD environment Advanced Design System (ADS) by Agilent Technologies is reported. For the linear parasitic network a lumped component structure has been chosen, where each element has been identified by using standard cold-FET S-parameter measurements [3, 7], performed up to 40 GHz. In Table 3.2 the values of the identified lumped components are reported.

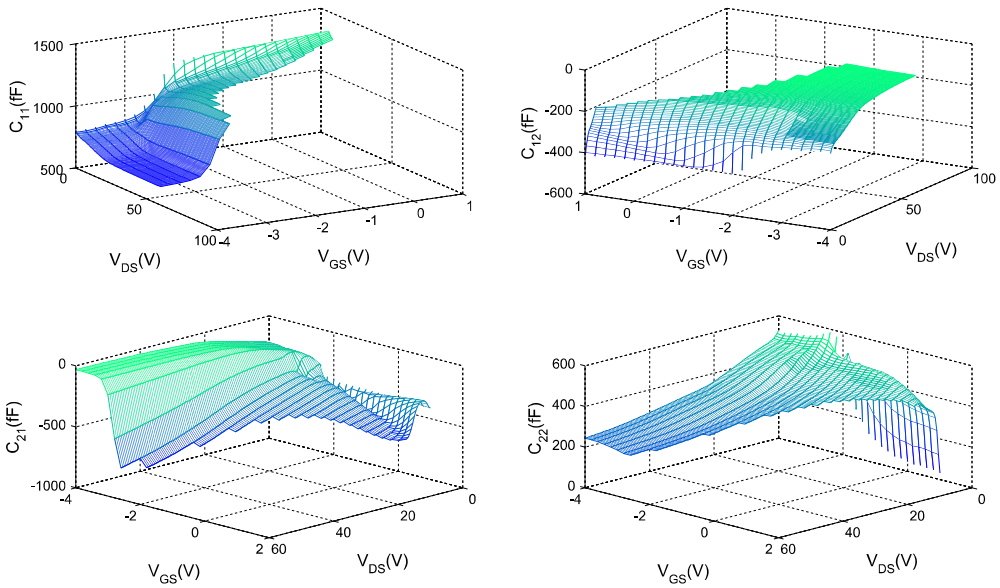



**Fig. 3.2** Intrinsic-capacitance data as a function of the intrinsic voltages identified from intrinsic Y-parameters.

TABLE 3.2. VALUES OF THE PARASITIC ELEMENTS

| *Element* | *Value* |
|---|---|
| $R_G$ | 1.1 Ω |
| $R_D$ | 1.5 Ω |
| $R_S$ | negligible |
| $L_G$ | 147 pH |
| $L_D$ | 125 pH |
| $L_S$ | 10 pH |
| $C_G$ | 36 fF |
| $C_D$ | 37 fF |

After a preliminary DC I/V characterization of the device, its multi-bias S-parameters up to 40 GHz have been measured and de-embedded by the identified parasitic network, in order to shift their reference plane to the intrinsic one. The intrinsic capacitance matrix was then calculated by using multi-bias intrinsic Y-parameters [18], considering a quasi-static approach. The values of $C_{ij}$ ($i,j = 1, 2$) were

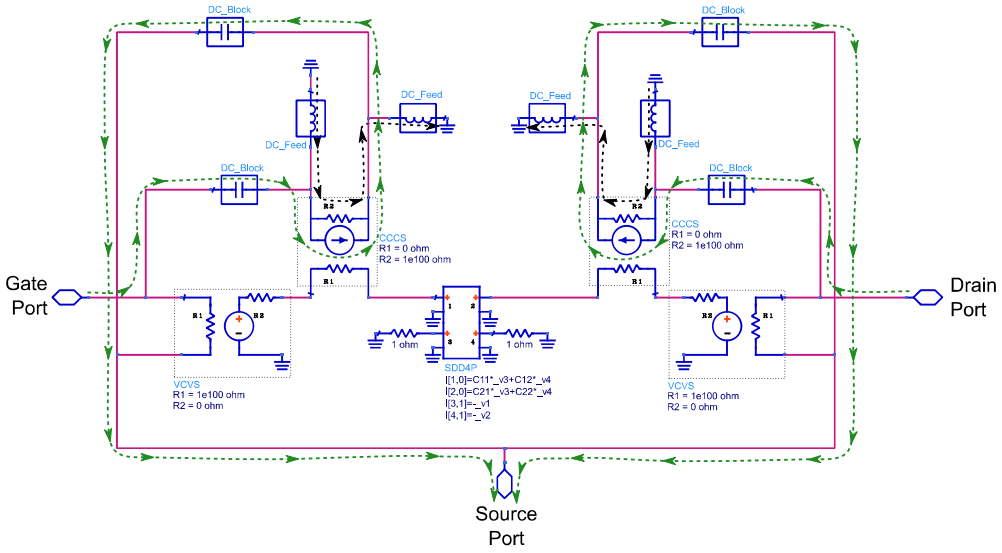



**Fig. 3.3** Schematic for the implementation of the capacitive core of the model. DC and AC components generated by this implementation are separated. DC compoments (black dashed paths) are short-circuited to ground while the AC components (green dashed paths) only reach the external ports.

stored in a LUT as a function of the intrinsic voltages. Results are reported in Fig. 3.2. A symbolically defined device (SDD), which allows to define a nonlinear element by using a time-domain formulation, has been used for implementing the nonlinear capacitances. The corresponding schematic that was exploited is reported in Fig. 3.3. The 4-port SDD is used to implement the following expressions

$$i_{G,C}(t) = C_{11}\frac{dv_{GSi}}{dt} + C_{12}\frac{dv_{DSi}}{dt} \tag{3.5}$$

$$i_{D,C}(t) = C_{21}\frac{dv_{GSi}}{dt} + C_{22}\frac{dv_{DSi}}{dt} \tag{3.6}$$

where $C_{ij}$ ($i,j = 1, 2$) are dynamically read from the LUT according to the instantaneous values of $v_{GSi}$ and $v_{DSi}$, whereas the derivatives are calculated through a dedicated frequency-dependent weighting function (i.e., the multiplication by $j\omega$ of each harmonic component) available for the SDD component.

It is noteworthy that DC and AC current paths have been separated with ideal components (*DC_block* and *DC_Feed*) in order to eliminate the spurious DC compo-

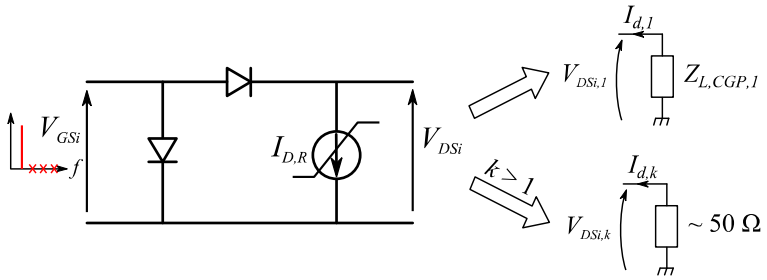



**Fig. 3.4** Approximations related to the resistive-core behavior in the considered operation. $Z_{L,CGP,1}$ is the load at the fundamental frequency.

nent generated by the model, due to the violation of the charge-conservation principle typical of such an implementation of the capacitive core [19-21].

The implementation of the resistive currents, $i_{G,R}$ and $i_{D,R}$, deserves a deeper discussion, bearing in mind the relationship as expressed in (3.4). On the gate side, the current can be described by a conventional formulation of the Schottky junction [22] or by a LUT approach as the one that will be detailed in the following for the drain current. With the aim of preserving a high level of computational efficiency, in this case the first approach was chosen.

On the drain side, the nonlinearity of the current generator produces voltage harmonic components. However, if no harmonic tuning is needed, at microwave frequencies, due to the shorting effect of the capacitances at the harmonic components, the resistive drain current is mainly defined by the load termination at its reference plane at the fundamental frequency. Under this hypothesis, the behavior of the current generator (i.e., the current phasors) can be described, in the space of the load impedances, characterizing the dependence on the voltage phasors only at the fundamental frequency. This greatly simplifies the model identification phase since the harmonic terminations can be set to the system characteristic impedance (i.e., 50 Ω), being the influence of their variation on the transistor response negligible. A schematic representation is shown in Fig. 3.4.

For the implementation of the current-generator model, a LUT approach was adopted. Due to the choices previously discussed, the use of a two-port frequency-domain defined device (FDD) is suitable, and each harmonic current component is defined as the value read from the LUT corresponding to the actual intrinsic voltage

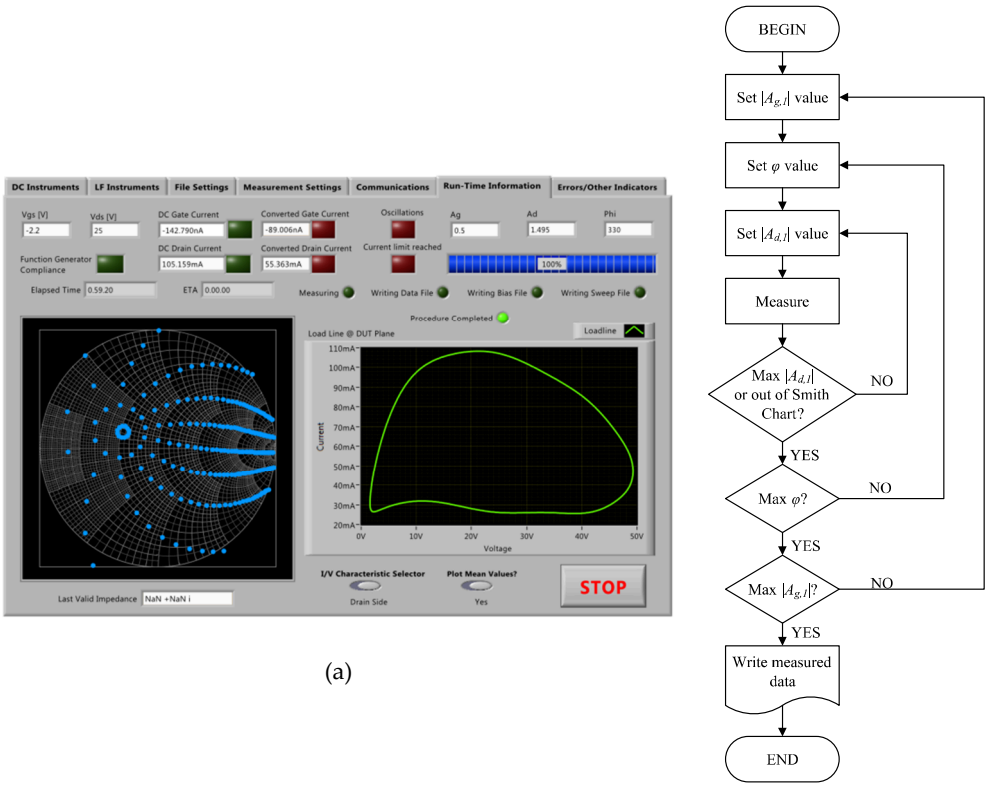
phasors $V_{GSi,1}$ and $V_{DSi,1}$. It is important to point out that the number of the current harmonic components $n$ available in the LUT plays an important role in the FDD definition of the resistive core. Indeed, it is not possible to use the model for harmonic-balance analyses where a number of harmonics greater than $n$ is needed. Anyway, this does not represent a big issue: since the characterization of the current generator is performed with the low-frequency measurement setup, an exhaustive number of current harmonics can be gathered without any additional cost and complexity of the adopted setup.

### 3.3. Measurement procedure and data processing

As previously mentioned, the characterization of the transistor current generator was obtained by means of continuous wave measurements carried out by means of the low-frequency measurement setup described in Chapter 1.

In order to apply the proposed model formulation, the behavior of the current generator has to be characterized for a sufficient number of load conditions and for different input power levels. To this end, a dedicated software to automatize the whole measurement procedure has been developed by using National Instruments LabVIEW. In Fig. 3.5, the flowchart of the developed software is reported as well as its front panel. Basically, for each amplitude value of the gate incident wave, $|A_{G,1}|$, the amplitude $|A_{D,1}|$ and the relative phase φ of the drain incident waveform are swept over a grid of values defined by the user and the corresponding load impedances are synthesized as long as they lie inside the Smith chart. Measured results are stored as vector frequency-domain data for a number of harmonics high enough to minimize the loss of information (in the present case, 11 spectral components were gathered, including the DC).

Each set of measurement data is acquired by keeping the bias point constant, therefore the associated model can be exploited for simulation at this fixed bias point only. If a multi-bias model is needed, the same procedure can be repeated for each bias condition of interest, thus increasing the dimension of the final LUT. Since no additional complexity is introduced from a practical point of view, this eventuality will not be discussed hereafter.




(a) (b)

**Fig. 3.5** Front panel of the developed software for the low-frequency characterization (a) and flow chart (b).

After the low-frequency data related to the current-generator model have been collected, they must be processed to define the model in the CAD environment, i.e., ADS. This data processing is strictly related to the model topology and implementation described in the previous paragraph. In particular, the following two operations are needed:

- Collected data have to be redefined as a function of the gate and drain voltage phasors at the intrinsic plane at the fundamental frequency, i.e., $V_{GSi,1}$ and $V_{DSi,1}$.
- Measurement data have to be extended with respect to the measured domain.

Each of these steps will be described in the following.

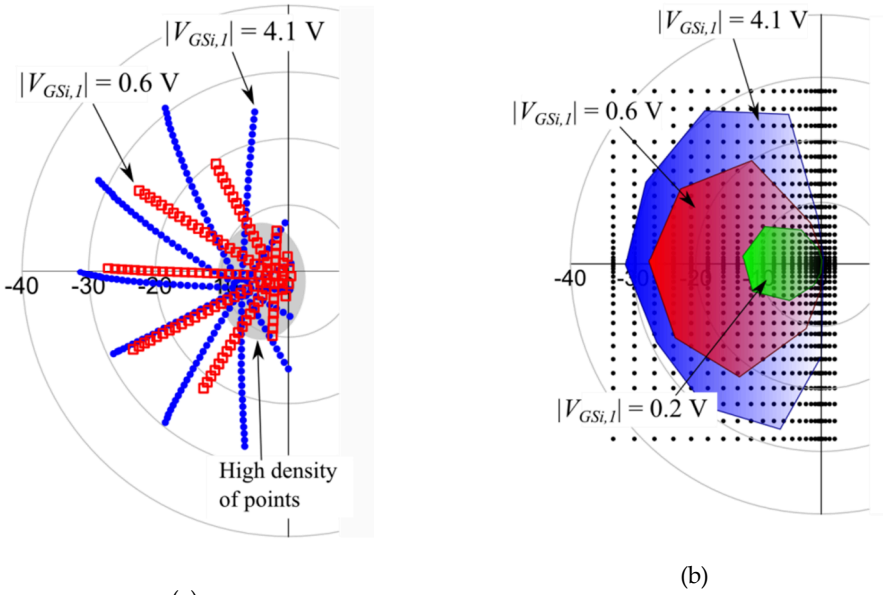



**Fig. 3.6** (a) Measured intrinsic drain voltage phasors at the fundamental frequency and (b) domain for different amplitudes of the gate voltage phasor at the fundamental frequency. The new grid of the drain voltage phasors for interpolation is shown in black dots in (b).

### *3.3.1. Domain redefinition*

According to (3.4), the current-generator model implemented as an FDD needs to be defined with relationships where the voltage phasors at its ports are directly coupled with the corresponding current values. Unfortunately, this is not a straightforward operation because the data acquired with the low-frequency measurements are expressed as dependent on incident wave parameters, i.e. $|A_{G,1}|$, $|A_{D,1}|$, and φ. For such a reason, measured data must be redefined by using the voltage phasors as independent variables. The whole operation is not straightforward since the measured voltage phasors at the fundamental frequency do not constitute a rectangular grid in the complex plane because of the measurement procedure itself. As a matter of fact, while the intrinsic gate voltage phasor remains constant for each input power level (i.e., $|A_{G,1}|$) because, at low-frequency, the gate port of the DUT is equivalent to an open circuit as long as the Schottky junction conduction is prevented, different drain voltage phasors at the fundamental frequency are available because of the different

loads that have been synthesized. In Fig. 3.6, an example for some values of $V_{GSi,1}$ is depicted. It is evident that the measured grids are not suitable for a regular LUT. To solve this problem, an interpolation procedure must be applied. Firstly, the phase of $V_{GSi,1}$ was assumed as reference, thus reducing the information related to $V_{GSi,1}$, which is stored in the LUT as the first independent variable, at just its magnitude. The second independent variable, $V_{DSi,1}$, is a complex number, so it has to be split into its real and imaginary parts. Another solution would be to use its magnitude and phase, but it was intentionally excluded because of the continuity issue that affects, by definition, the argument of a complex number.

According to this choice, a new rectangular grid was defined within the whole measured space. To this end, another detail has to be taken into account. For low values of $|V_{GSi,1}|$, the measured values of $|V_{DSi,1}|$ lie inside a small area of the polar plane, i.e., approximately the gray area reported in Fig. 3.6(a). Thus, a large number of points are *squeezed* inside a small area, resulting very close to each other if compared to the ones obtained for higher values of $|V_{GSi,1}|$. To avoid a loss of information and guarantee robust convergence capability at low levels of input power, the new grid has to be dense in this area. However, keeping such a large density for higher power levels would lead to a huge number of entries in the LUT, which directly affects its dimension. To keep the latter limited, the step of the grid was adjusted along the axes by using a quadratic rule. The resulting grid is reported in Fig. 3.6(b). The interpolation was performed over this grid for each level of $|V_{GSi,1}|$ separately, by using standard procedures (i.e., *triScatteredInterp* [23]) available in the commercial software MATLAB. The result of the interpolation was a regular grid in the new voltage phasor domain. In the extrapolated region, the data need to be further processed according to the following step.

### *3.3.2. Data extension*

The choice of the interpolation grid depicted in Fig. 3.6(b) shows that many points are outside the measured domain, especially for the lowest levels of $|V_{GSi,1}|$. Obviously, the corresponding current phasors cannot be obtained through interpolation, as no measurement is available. Indeed, the interpolator returns an invalid numerical value

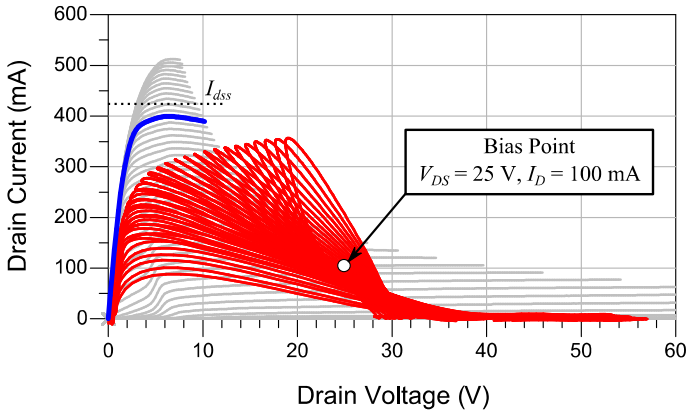



**Fig. 3.7** Example of the load lines synthesized during the low-frequency characterization. The bias point is indicated with a white filled dot, whereas the load lines are shown via the red solid line. In the background, the DC I/V characteristics are depicted and the DC characteristic for $V_{GS}$ = - 0.2 V is highlighted with a thick solid line.

for them, such as NaN (not a number), which is not correctly managed by the simulator. To avoid this problem, an extrapolation procedure has been adopted. For each value of $|V_{GSi,1}|$, the current phasors outside the measured domain were determined by using suitable routines (i.e., the curvefitting function *fit* with biharmonic surface interpolation [24]) available in MATLAB. At the end of this procedure, the LUT is suitable for implementing the model of the current generator in the CAD software.

It is worth noticing that the extrapolation of the measured grid is only functional to the model implementation in a CAD environment and to guarantee convergence for nonlinear simulators. In fact, all the operating conditions of interest for the current generator are defined in the model LUT by measured or interpolated data.

## 3.4. Low-frequency characterization

For the identification of the current-generator model, the DUT has then been characterized at low frequency, i.e., 2 MHz, by exploiting the measurement setup described in Chapter 1 for input power levels corresponding to different values of $|A_{G,1}|$ between 0.05 V and 2.05 V. A constant step of 0.25 V was considered in a first place. However, between $|A_{G,1}|$ = 0.05 V and $|A_{G,1}|$ = 0.3 V, the device behavior changes a lot in terms of output power because of the high low-frequency gain. Thus, for the lower input power levels, a finer step of 0.05 V has been used. Measurement results have

been collected and processed by the MATLAB procedure. The final LUT contains data for 13 input power levels, i.e., 13 levels of $|V_{GSi,1}|$, corresponding to 19x29 points for the real and the imaginary part of $|V_{DSi,1}|$ respectively, and 11 harmonics, including the DC component, for a total dataset size of about 2.1 MB.

Fig. 3.7 shows some synthesized load lines. They were measured for a constant value of both $|A_{G,1}|$ and φ, whereas the amplitude of the drain incident wave has been swept. For each load line, the gate voltage is a sinusoidal wave with an amplitude of 2 V at the DUT plane that reaches, at its maximum, the value of - 0.2 V. By looking at the DC characteristic for $V_{GS}$ = - 0.2 V, the effect of dispersive phenomena related to traps and thermal effects on the dynamic behavior of the device is well evident. This behavior, depending on both the thermal and trap occupation states, is very difficult to accurately describe. Nevertheless, the behavioral nature of the proposed model makes such a description simple since it is implemented by directly using the gathered measurements.

### 3.5. Model robustness in nonlinear simulators

As well known, the main problems for a LUT-based model in nonlinear analysis are convergence robustness and simulation time. To verify the robustness of the model in a nonlinear simulation environment, a large number of operating conditions should be considered. In this case, load–pull simulations were chosen. The model has been tested in a simulation bench created by using Agilent ADS 2008 Update 2. The source impedance was kept constant to 50 Ω, whereas the fundamental load impedance was swept over a grid of 227 values, covering an area of the Smith chart of radius 0.8. Simulations were performed for different operating frequencies from 2 to 12 GHz and no convergence issue has been observed.

Simulation data were analyzed and processed in order to obtain load–pull contours. In Fig. 3.8, constant output power contours are shown for 2 dB of gain compression for each operating frequency. Their regular shape suggests the model does not produce any discontinuity or numerical problem for the simulator that could be induced by the interpolation over the LUT data.

The optimum impedance predicted by the model moves on the Smith chart as a function of frequency following a typical trajectory (see Fig. 3.8). In the figure, the impedance corresponding to the maximum output power at LF (i.e., 2 MHz) for 2 dB of gain compression is also reported for comparison. As expected [13], it lies on the real axis of the Smith chart, which corresponds to a pure resistive impedance.

Regarding the simulation time, it was pretty limited. As an example, at the fundamental frequency of 4 GHz and considering an input power swept between 0–18 dBm with a step of 1 dB, the simulation lasted approximately 140 s on a PC equipped with an Intel Core i7-3770K microprocessor with a 3.5-GHz clock frequency and 8 GB of DDR3 RAM. This simulation time is strongly affected by the LUT implementation of the capacitive core. In practice, for the simulation of the resistive core only, over the same grid of load impedances and for the same number of input power levels, a simulation time of just 16 s was needed.

### 3.6. High-frequency validation

The model has been validated by exploiting high-frequency measurements performed with a large-signal network analyzer (LSNA) with a total bandwidth of 50 GHz. The device was measured at 4 GHz, and under the same bias condition for which the model was extracted, different load conditions were synthesized at the fundamental frequency by using a mechanical tuner. Impedances at the harmonic frequencies were not controlled with the aim of validating the proposed approach in the selected operation (i.e., no tuning at harmonics is performed). It is important to observe that the selected operating frequency is relatively low in order to test the model in an unfavorable condition for the shorting effect of the intrinsic nonlinear capacitances at the harmonic frequencies. Indeed, being the selected technology oriented to X-band power amplifier design, up to 12 GHz the shorting effect is not yet strongly pronounced.

In Figs. 3.9 and 3.10, comparisons between model predictions and measurement results are shown. The load impedances cover a set of pretty different values from conditions close to the power matching to strongly mismatched ones. In any case, the model provides a very good fit of the device behavior, in some conditions up to a gain

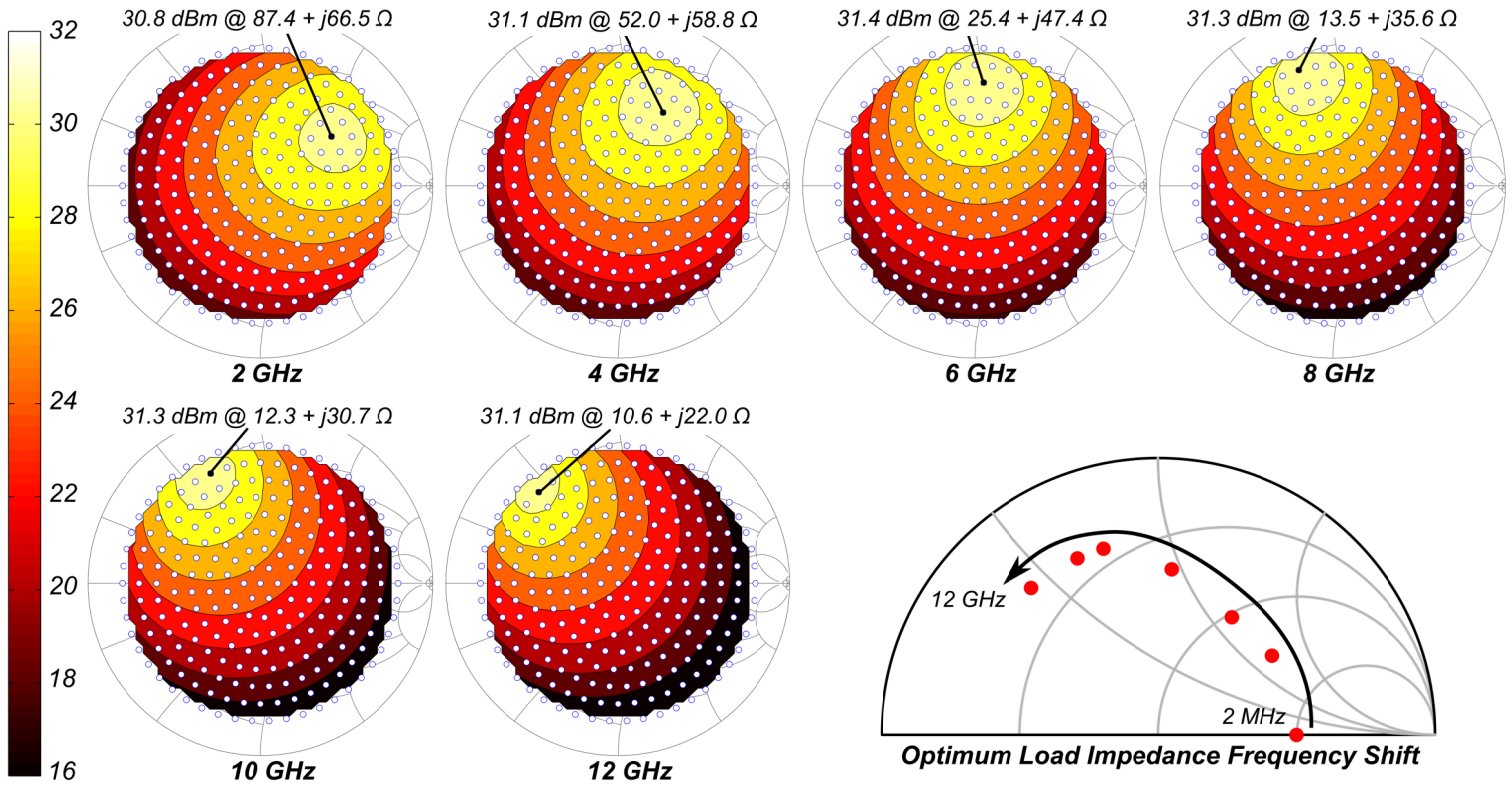



**Fig. 3.8** Simulated output power load–pull contours for 2 dB of gain compression at different frequencies within 2 and 12 GHz. The power difference between the contour curves is 2 dB. The shift of the predicted optimum impedance versus frequency is pointed out. The optimum impedance obtained at low frequency (i.e., 2 MHz) is also shown.

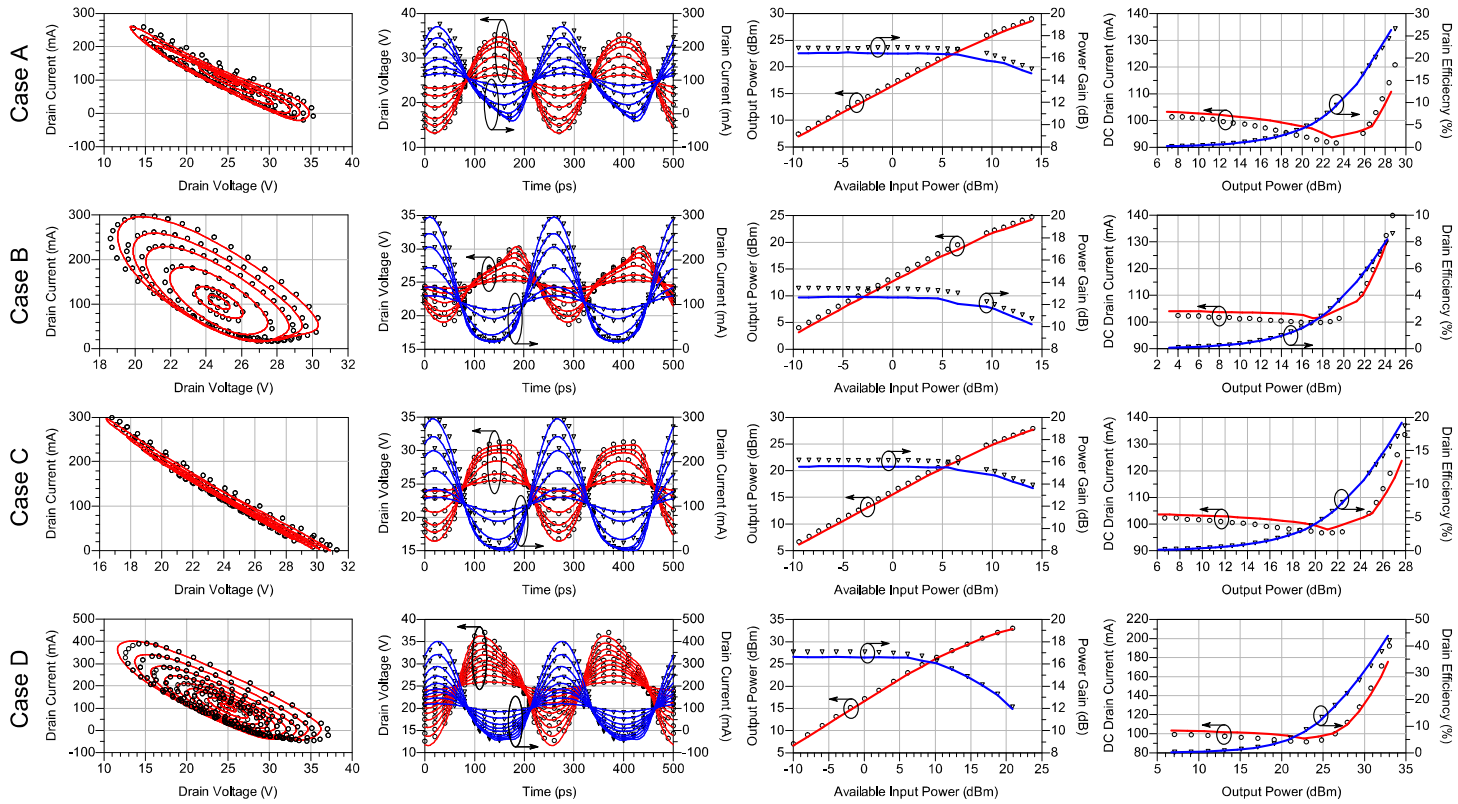



**Fig. 3.9** Comparisons between measurement (symbols) and simulation (solid lines) under large-signal operation at 4 GHz. The bias point is $V_{DS}$ = 25 V and $I_D$ = 100 mA. Fundamental load impedances are: 81.2 + j19.6 Ω (case A), 25.2 – j24.1 Ω (case B), 50.0 + j0.0 Ω (case C), 46.9 + j27.2 Ω (case D).

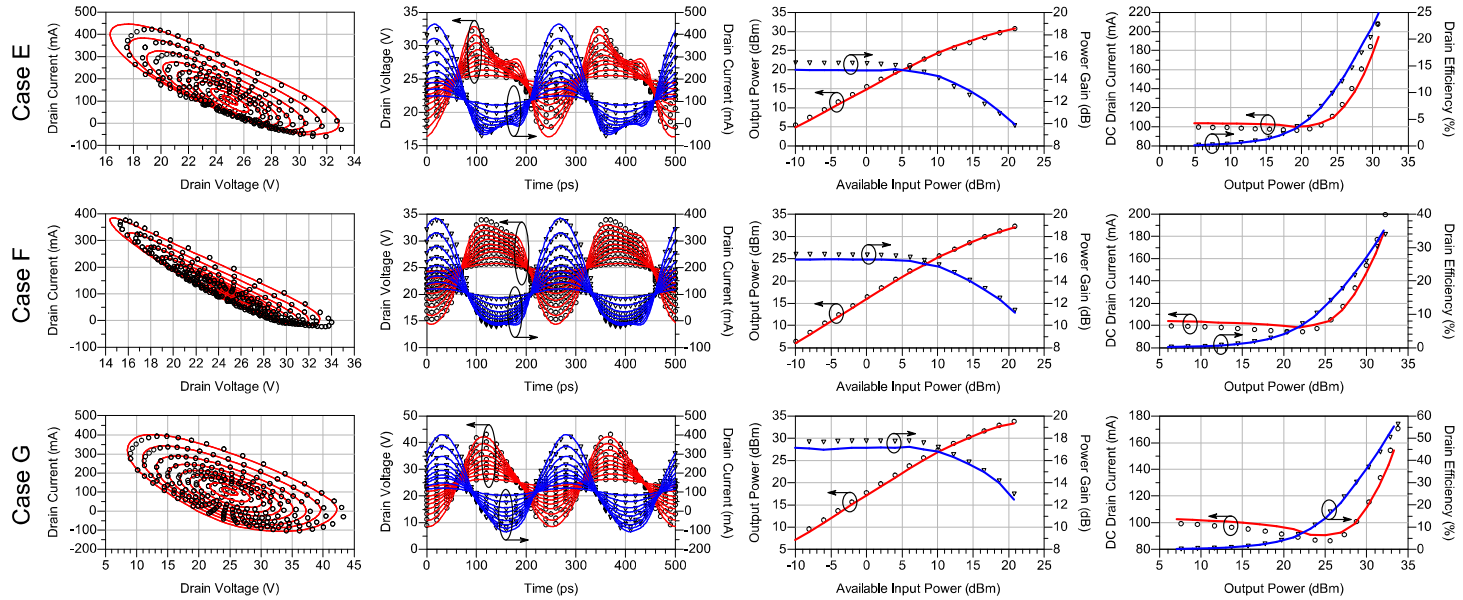



**Fig. 3.10** Comparisons between measurement (symbols) and simulation (solid lines) under large-signal operation at 4 GHz. The bias point is $V_{DS}$ = 25 V and $I_D$ = 100 mA. Fundamental load impedances are: 24.3 + j15.3 Ω (case E), 35.0 + j15.6 Ω (case F), and 46.8 + j48.8 Ω (case G).

compression level higher than 4 dB.

There is a small difference (fraction of a decibel) between the simulated and measured small-signal gain, whose entity depends on the load impedance value. These discrepancies can be equally attributed to the inaccuracy of the model of the intrinsic nonlinear capacitances (extracted from multi-bias S-parameters) and residual uncertainty of the LSNA. As the input power increases, the fitting of the model gets better, overlapping measured data.

The last column in Figs. 3.9 and 3.10 shows the most interesting results since all the quantities involved (i.e., average value of the drain current, output power, and efficiency) are strictly related to the current-generator model. As can be seen, the agreement is excellent. It is important to point out how the shape of the average drain current is well reproduced by the model, including the initial typical drop ascribed in [10] to fast trapping phenomena.

## 3.7. Observation on small-signal validation

The developed model does not allow for a direct validation of the small-signal parameters, i.e., S parameters, since only nonlinear simulations can be performed. However, a comparison can be done by considering a harmonic balance simulation performed by using 50-Ω terminations at both the ports of the device and an input power low-enough so that the intrinsic gate voltage corresponds to the lowest value stored in the LUT to guarantee a linear operating condition. Obviously, the comparison is meaningful for the selected bias condition only.

The result is reported in Fig. 3.11. As expected, the model shows an accurate prediction capability. Indeed, such a consideration could be retrived also by looking at the results reported in Figs. 3.9 and 3.10 for the lowest levels of input power.

## 3.8. Conclusion

In this Chapter, an original approach to behavioral modeling formulation for transistors has been discussed and applied to a GaN FET. It exploits the advantages of both compact and behavioral modeling techniques. The first approach has been applied for the identification of the capacitive core and the parasitic network by using a conven-

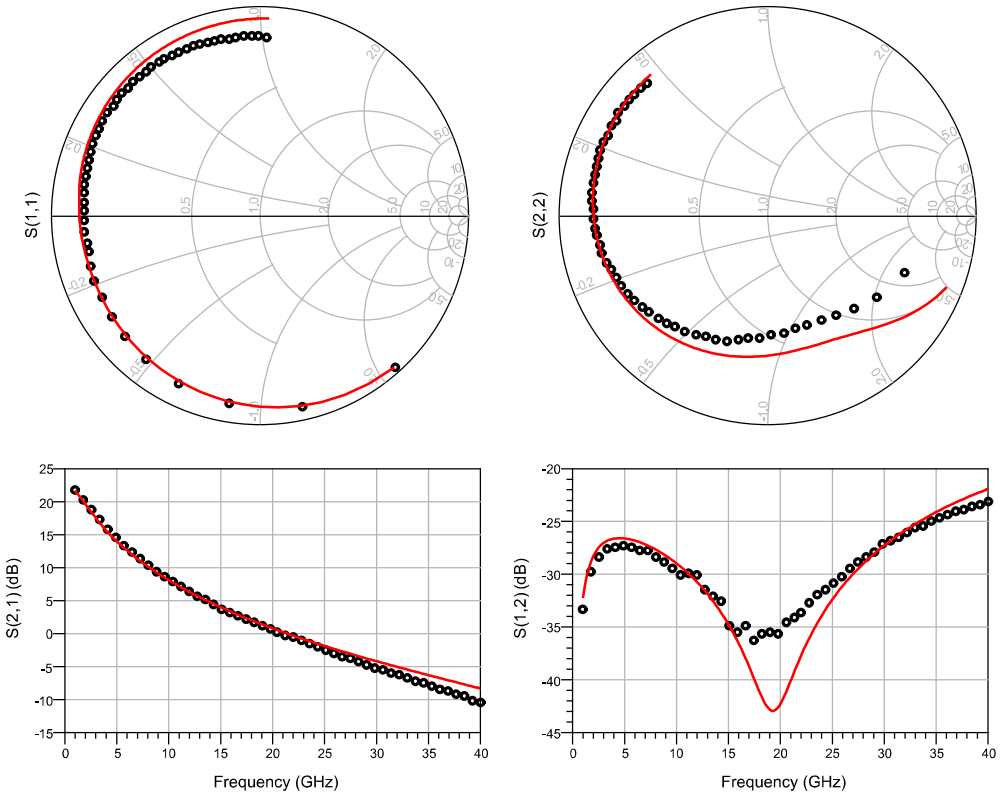



**Fig. 3.11** Model predictions (continuous line) and S-parameter measurements (circles) in $V_{DS}$ = 25 V, $I_D$ = 100 mA.

tional equivalent circuit description. The behavioral approach is devoted to the model implementation of the resistive core, and, more precisely, its current generator, characterized by means of low-frequency measurements. They allow to gather both thermal and trapping effects causing low-frequency dispersion, which will be intrinsically included in the model description. Moreover, the advantages of exploiting low-frequency measurements in terms of frequency and power limitations with respect to high-frequency setups have been pointed out.

The developed model is robust for nonlinear simulations, which are not sensibly affected in terms of simulation time by the LUT structure of the current-generator model implementation.

Furthermore, since the behavioral approach is applied to the resistive core only, intrinsic sections remain accessible, which constitutes a great advantage for circuit design purposes, as will be clearly explained in the following chapter.

The validation through time-domain high-frequency measurements showed excellent prediction capabilities, in particular for the results directly related to the current-generator behavior. Effects as fast-trapping phenomena are perfectly reproduced without the need of a dedicated modeling solution.

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*Chapter 4*

# DESIGN METHODOLOGY FOR HIGH-EFFICIENCY POWER AMPLIFIERS

In the most general case, a microwave power amplifiers is a complex circuit made of several active devices (i.e., transistors), organized in one or more stages connected to each other by passive networks to distribute power and maximize the overall performance. Each part must be properly designed according to the specifications. This is a very complex procedure and it is subject to the choices of the designer, who often has different degrees of freedom also related to his own experience.

Whatever the design choices could be, some basic information does exist the designer need to know. The most important one is the knowledge of the device performance as a function of some fundamental parameters, as the bias point and its source and load impedances [1, 2].

This chapter focuses on this particular topic. Firstly, a brief introduction on microwave power-amplifier topology will be given by considering the analysis of a single transistor amplifier. Then an example of high-efficiency class of operation, i.e., class-F amplifier, will be discussed. This will clarify how the selection of the proper terminations affects the device performance and the feasibility of the theoretical prescriptions on actual devices will be discussed.

Successively, the load-pull technique will be briefly reviewed as an important tool for designers to identify the optimum operating condition, although load-pull use can be limited by power and frequency constraints.

Later on, a design methodology based on large-signal low-frequency measurements will be described, highlighting the features that make it an interesting alterna-

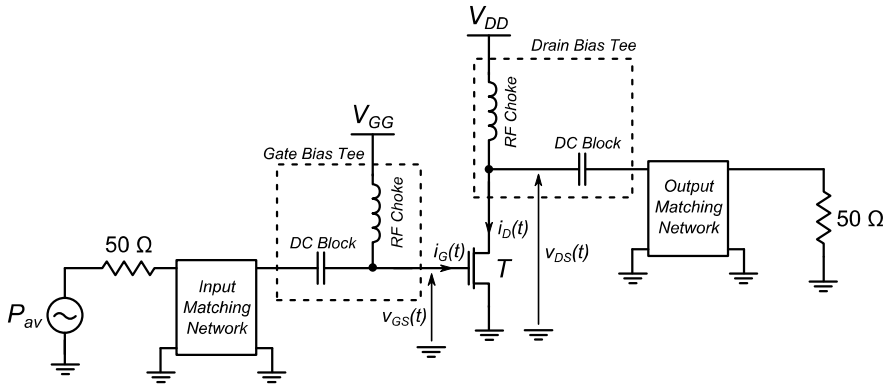



**Fig. 4.1** Simplified topology of a power amplifier based on an FET device.

tive to load-pull-based techniques. To clarify this aspect, a first example of application will be discussed, with the aim of describing how it is possible to identify the optimum condition at microwave frequency for an electron device starting from a small set of large-signal low-frequency measurements and conventional frequency-dependent S-parameter measurements.

Finally, the design methodology will be applied to obtain high-frequency load-pull data [3]. In particular, a class-F operation will be considered as an example.

## 4.1. Design of a high-efficiency power amplifier

As mentioned in the introduction, this paragraph focuses on the identification of the optimum operating condition at microwave frequencies for a single active device. For this analysis, a simplified single-stage power amplifier topology can be considered, as shown in Fig. 4.1. The bias-tees, realized in principle with a capacitor (*DC block*) and an inductor (*RF choke*), separate the signal paths from the DC paths. The *matching networks* are two passive circuits designed to provide the proper impedances at their input and output ports for optimal amplifier performance.

The operating condition of the transistor is mainly determined by three factors: its bias point and the source and load impedances. Typical design techniques are based on the analysis of how these elements affect amplifier performance by determining the transistor load line [1,2].

The *waveform engineering* [4] approach is one of the state-of-art techniques. It is based on the possibility of shaping (*engineering*) voltage and current waveforms at the active device port in order to obtain optimal performance, in particular in terms of efficiency. For this purpose, it is convenient to discuss here a specific example of operating class where waveform engineering concepts are exploited to increase power amplifier efficiency.

### *4.1.1. An example of high-efficiency operating condition: the class-F amplifier*

The class-F operating condition [1, 2] for a power amplifier guarantees the minimum amount of dissipated power on the active device and, at the same time the concentration of the output power on the fundamental harmonic only.

In general, the performance of a transistor can be defined by the *load-line* the device follows under dynamic operation according to its I/V characteristics; the load-line is determined by the shape of the drain voltage waveform, $v_{DS}(t)$, and the drain current one, $i_D(t)$. Due to the device nonlinearities, they can be expressed in the frequency domain as:

$$v_{DS}(t) = V_{DS} - \sum_{k=1}^{+\infty} V_{DS,k} \cos\left(k\omega_0 t + \phi_k\right) \tag{4.1}$$

$$i_{DS}(t) = I_D + \sum_{k=1}^{+\infty} I_{D,k} \cos\left(k\omega_0 t + \xi_k\right) \tag{4.2}$$

where $V_{DS,k}$ and $I_{D,k}$ are the amplitudes of the $k$-th harmonic components of $v_{DS}(t)$ and $i_D(t)$, $V_{DS}$ and $I_D$ are their average values, $\phi_k$ and $\xi_k$ are the corresponding phases and $\omega_0 = 2\pi f_0$, $f_0$ being the fundamental frequency.

Starting from equations (4.1) and (4.2), it is possible to derive the general expressions of the DC supplied power, $P_{DC}$, and RF power provided to the load, $P_{RF}$, at the device reference plane:

$$P_{DC} = V_{DS} I_D \tag{4.3}$$

$$P_{RF} = \frac{1}{2} \sum_{k=1}^{+\infty} V_{DS,k} I_{D,k} \cos\left(\phi_k - \xi_k\right) = \sum_{k=1}^{+\infty} P_{RF,k} \tag{4.4}$$

where $P_{RF,k}$ is the active power provided at the $k$-th harmonic. If the input power can be considered negligible[**], the power dissipated on the transistor will be the average value of the instantaneous power on the transistor itself or, in other words, the difference between DC supplied power and the total RF output power, so that:

$$P_{diss} = \frac{1}{T}\int_0^T v_{DS}(t) i_D(t) dt = P_{DC} - P_{RF} \tag{4.5}$$

$T = 1/f_0$ being the period of the fundamental signal.

In power amplifier design, the only RF power component of interest is the one at the fundamental frequency, i.e., $P_{RF,1}$. For such a reason, the efficiency of the amplifier can be expressed as:

$$\eta = \frac{P_{RF,1}}{P_{DC}} = \frac{P_{RF,1}}{P_{diss} + P_{RF,1} + \sum_{k\geq 2} P_{RF,k}} \tag{4.6}$$

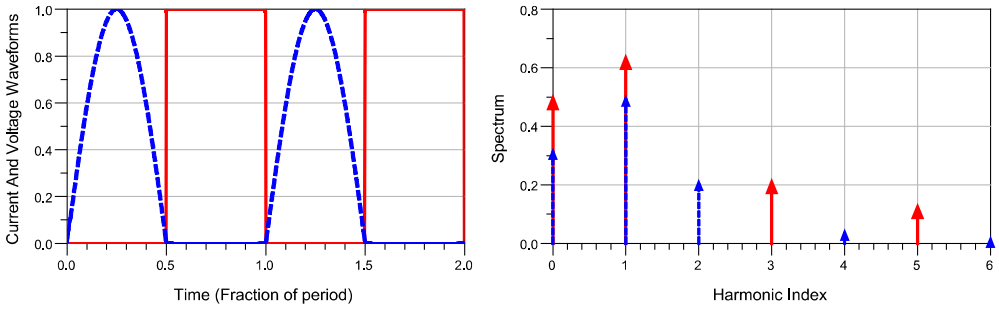
Therefore, to maximize the efficiency the following two conditions must be satisfied:

- *Zero dissipated power on the active device*. According to equation (4.5), it means that $v_{DS}(t)$ and $i_D(t)$ waveforms must not overlap.
- *No active power at harmonics*. Considering (4.6) this can be obtained in two different ways: (i) by forcing a relative phase of ± 90° between current and voltage harmonic components (i.e., pure reactive impedances at harmonics); (ii) by forcing at least one between current and voltage harmonic components to have a magnitude equal to zero.

The class-F amplifier fulfills both these requirements by considering a square waveform for $v_{DS}(t)$ and a half-rectified sine wave for $i_D(t)$[††]. As depicted in Fig. 4.2, there is not any superposition between the two waveforms. Moreover, by looking at their spectra, the current has only even harmonics (except for the fundamental) whereas

[**] In an actual device, this hypothesis is reasonable for high levels of power gain or for operating frequency low enough to consider the reactive phenomena negligible.

[††] The second condition could be also fulfilled by using pure reactive harmonic terminations, providing a relative phase of ±90° between current and voltage harmonic components. However, this choice would not satisfy the non-overlapping requirement, unless the active device were driven as a switch. This operating class, typically referred to as class-E amplifier [5] will be not dealt with here.




(a) (b)

**Fig. 4.2** Drain current and voltage waveforms (a) and corresponding spectra (b) for class F. Waveforms have been normalized with respect to their maximum value.

the voltage has only odd harmonics. This implies no active power at harmonics, fulfilling the second condition for maximum efficiency.

The spectral content of the *engineered* current and voltage waveforms can be obtained by using a class-AB bias for the device and a load impedance defined as follows.

$$Z_L = \begin{cases} Z_{OPT} & f = f_0 \\ 0\ \Omega & f = kf_0,\ k \text{ even} \\ +\infty & f = kf_0,\ k \text{ odd} \end{cases} \tag{4.7}$$

where $Z_{OPT}$ is the impedance that optimizes the device performance, according to specifications.

### *4.1.2. Observations on class-F amplifier implementation*

In the previous paragraph, the analysis of the class-F amplifier has been reviewed. As reported, such an amplifier can be designed by using a specific set of load impedances at fundamental and harmonics to *shape* voltage and current waveforms at the output port of the active device. However, what is defined by the theory could lack of practical feasibility.

First of all, the analysis of a class-F amplifier is related to the operating regime of the active device at its current-generator plane by considering its I/V characteristics. Considering a typical microwave application, the operating frequency is high enough to make it impossible to directly control the harmonic terminations at the current-generator reference plane, since the contributions of displacement currents due to in-

trinsic capacitances and parasitic structures are not negligible. This operation can be done only by exploiting computer-aided design (CAD) with a model of the electron device that allows to access the intrinsic sections. Unfortunately, foundries do not always provide this capability for their own models.

Another aspect that has to be considered comes from equation (4.6). It defines the load impedances that have to be synthesized up to an infinite frequency, which is obviously not feasible. For instance, the synthesis of an open circuit becomes nearly impossible as the frequency increases, since the intrinsic capacitances will tend to short-circuit the intrinsic terminals, showing a low impedance at the current-generator plane whatever the extrinsic load impedance would be.

Moreover, synthesizing terminations for a large number of harmonic components requires matching networks with high frequency selectivity, reducing the bandwidth of the power amplifier.

For these reasons, a maximum of three harmonics is typically considered for the load termination, which will only approximate the ideal behavior of the class-F amplifier, thus reducing, with respect to theory, its final performance, i.e., the maximum theoretical efficiency drops to 88% [2].

Finally, it is noteworthy that the actual power amplifier performance depends on dynamic I/V characteristics of the active device, thus low-frequency dispersion could produce a severe degradation [6]. As an example, a greater knee voltage with respect to DC I/V characteristics could provide a reduction of the efficiency of several percentage points with respect to the expected one.

## 4.2. Load-pull techniques

Load-pull measurements [2, 7-9] are a useful tool for microwave circuit designers, since they provide a lot of information directly exploitable for power amplifier design. In Fig. 4.3 a typical load-pull setup is depicted. The device under test (DUT) is connected at two mechanical tuners. Their role is to change load and source terminations with respect to the system impedance (i.e., 50 Ω). An RF source provides the input power while a two-channel power meter is devoted to the acquisition of the input and output power levels. The available input power is typically acquired through a

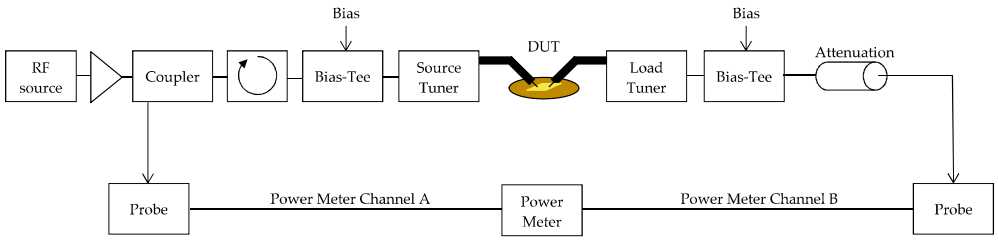



**Fig. 4.3** Block diagram of a typical passive load-pull system.

coupler and a circulator can be inserted on the input-signal path to provide a better 50-Ω source termination to the system. On the output path, an attenuator can also be added to protect the power-meter probe from high-power levels. Bias voltages and currents at the DUT can be imposed and monitored through a DC source.

The purpose of this setup is to experimentally analyze the performance of the device for different load and source terminations in order to determine its optimum operation. An example of the typical measurement procedure consists in performing an input power sweep for a set of load impedances defining a grid on the Smith chart. For each power level different data can be measured, like the output power, power gain and efficiency. The results are typically shown on a Smith chart, as reported in Fig. 4.4. Here, the *load-pull contours* represent the loci of the load impedances providing the same amount of output power for a constant level of input power. The center of the contours represents the optimum load impedance, i.e., the one that guarantees the maximum output power for the selected condition. It is worth noting that the optimum impedance is not unique: different parameters (e.g., output power, efficiency, gain) can have different optimum impedances. Load-pull contours can be a useful tool if a trade-off is needed.

If a source tuner is available in the system, *source-pull* can be exploited to find the best input termination to maximize the device power gain. In the most general case, changing the source termination influences the output condition and vice versa, thus source pull and load pull are often iterated until design specifics are fulfilled.

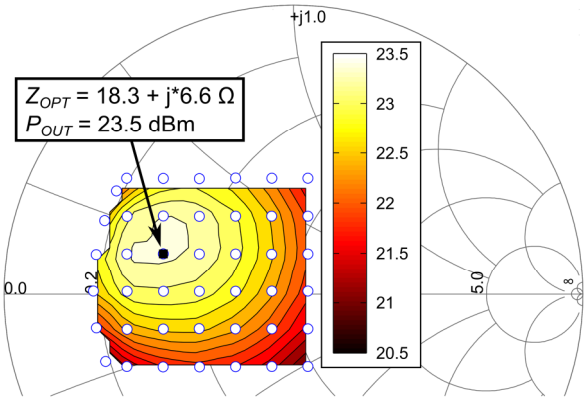



**Fig. 4.4** Constant output power load-pull contours for a constant level of input power of 11 dBm measured on a 0.15x600 μm² GaAs pHEMT biased in $V_{DS}$ = 6 V, $I_{DS}$ = 74 mA at 20 GHz.

The load-pull technique that has been described so far is often referred to as *passive* load pull, since it exploits passive elements (i.e., the tuners) to synthesize the desired impedances. This is typically done at the fundamental frequency. However, the use of multiharmonic tuners is more and more diffused to implement high-efficiency operating classes, which need a tuning of the load termination at harmonics as well.

The main limitation of passive load-pull techniques is related to the infeasibility of synthesizing impedances close to the boundaries of the Smith chart. This is a consequence of the unavoidable losses of both the signal paths and the setup components which become more and more critical as the frequency increases.

An alternative to passive load-pull systems consists in the *active* synthesis of impedances, i.e., the *active load-pull* [8]. In this case, the output tuner is replaced with a second RF signal generator, and the load impedance can be determined by tuning the magnitude and phase of the generated incident wave with respect to the reflected one provided by the active device. This would require a second RF generator or alternatively the use of part of the input power to generate the output incident wave properly amplified and phase shifted. The second source can be obtained also by drawing part of the output signal provided by the device itself and inject it after having adjusted its magnitude and phase. This solution, called *active loop* [10], is more critical since it implies a feedback path in the output section of the setup that can cause oscillations, which must be properly prevented.

With an active technique the synthesis of every impedance in the Smith chart is possible, because the losses produced by components and measurement instruments are compensated by properly tuning the amplitude of the output incident wave.

An important limitation that affects every load-pull system concerns the amount of power that can be safely managed. Operating at microwave frequency, this can be a critical aspect, in particular when new technologies, providing high-power densities have to be characterized.

The typical load-pull systems provide scalar measurement data. Time-domain waveforms could be gathered if a set of additional instruments is included in the system, transforming it in a *large-signal network analyzer* (LSNA). This setup can provide a full characterization of the device in actual operating conditions, although with a significant increase of its cost and the complexity of the calibration procedure. Moreover, large-signal time-domain setups suffer from frequency limitations. As an example, the state of art shows a total bandwidth of 67 GHz for such systems that could be very restrictive when the device has to be characterized for high-efficiency operation since it requires the acquisition of waveforms up to several harmonic components.

A final consideration must be done related to the importance of load-pull systems for design purposes. Since the operating frequency is in the microwave band, no information is directly retrievable at the current-generator plane. Therefore, it is not possible to properly verify the class of operation of an active device with sufficient accuracy by looking at only scalar results or time-domain extrinsic waveforms.

The availability of vector measurements has actually an important advantage. As a matter of fact, there exist some procedures, called *nonlinear de-embedding techniques* [11-13], which allow deriving the current-generator waveforms for a measured operating condition starting from the extrinsic current and voltage waveforms. These techniques require the availability of a model of both the parasitic network and the capacitive core, in order to calculate their contributions and remove them from the high-frequency measured data. Such a procedure, which is theoretically feasible, suffers from some limitations, related to the required measurement system (i.e., LSNA) as previously mentioned, and to the model accuracy.

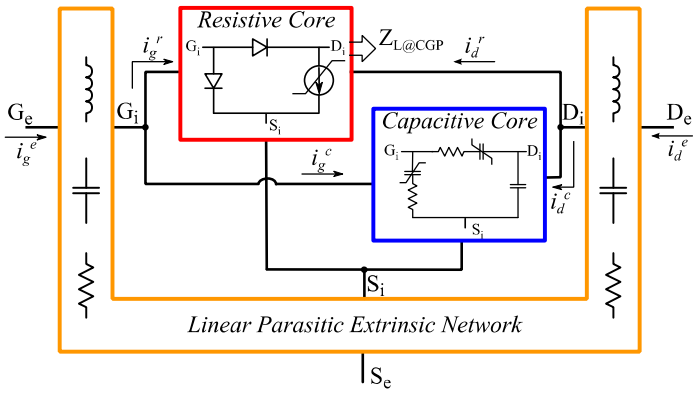



**Fig. 4.5** General topology of a nonlinear model of FET devices.

## 4.3. Nonlinear embedding as a design methodology

An alternative methodology to load-pull techniques for the design of power amplifiers is based on the *nonlinear embedding* technique [14]. Considering the topology of a nonlinear model of a FET device introduced in Chapter 1 and reported in Fig. 4.5 for convenience, this approach consists in fixing the operating condition at the current-generator plane, and then identifying the corresponding condition at the extrinsic plane by exploiting a model of both the capacitive core and the parasitic network. This procedure has been presented and applied in different works [5, 15-21], and it is here briefly summarized.

As mentioned, according to the theory on power amplifier design, the operating condition is defined at the current-generator plane. Therefore, the design methodology starts with its direct identification on the actual device that will be exploited for the design. Since it is necessary to isolate the current-generator contribution, measurements at design frequency must be avoided[‡‡]. DC measurements could be used as a first estimate, but the results would not include the low-frequency dispersion, which could produce severe degradation of the device performance and then of the design methodology prediction. To overcome this issue, the low-frequency setup described

‡‡ High-frequency measurements could be used if associated to a nonlinear de-embedding procedure to shift measured data at the intrinsic plane. However, this faces measurement setup limitations and the possible lack of accuracy of the model of both the capacitive core and the parasitic network needed for the de-embedding technique.

in Chapter 1 can be exploited, since it allows a direct measurement of the resistive core under any load condition. Once the latter has been selected and measured, the result is a set of voltage phasors at the intrinsic plane $[V(k\omega_{LF})]^i$ and a set of current phasors at the current-generator plane $[I(k\omega_{LF})]^R$, being $k$ the frequency index. Above the cut-off of the dispersive effects [22, 23], the dynamic I/V behavior of the device (i.e., the resistive core) is actually frequency independent, which means that, for each RF frequency, there is an operating condition at the extrinsic plane such that the behavior of the resistive core is exactly equal (i.e., identical load line) to the one measured at low frequency. In other words, the RF phasors will be the same as the low-frequency measured ones just shifted at the frequency $\omega_{RF}$, i.e,

$$\begin{cases}[V(k\omega_{LF})]^i \\ [I(k\omega_{LF})]^R\end{cases} \xrightarrow{\text{Frequency Shift at } \omega_{RF}} \begin{cases}[V(k\omega_{RF})]^i \\ [I(k\omega_{RF})]^R\end{cases} \tag{4.8}$$

At this stage, the high-frequency condition that guarantees the same waveforms measured at low-frequency at the current generator plane can be assessed by combining the measured data with the contributions of both the capacitive core and the parasitic network, at the selected RF frequency. To this purpose, a model of these elements is necessary.

Displacement currents $[I(k\omega_{RF})]^C$ can be calculated by applying the frequency-shifted voltage phasors $[V(k\omega_{RF})]^i$ to a model of the capacitive core. Then, it is possible to calculate the total intrinsic current phasors as:

$$[I(k\omega_{RF})]^i = [I(k\omega_{RF})]^R + [I(k\omega_{RF})]^C \tag{4.9}$$

Now, every electrical value at the intrinsic plane is known at the design frequency. To shift these data at the extrinsic plane, i.e., $[V(k\omega_{RF})]^e$ and $[I(k\omega_{RF})]^e$, the parasitic network effects have to be included. This can be done by using a proper description of them, like a 4x4 hybrid matrix **H**, and exploiting the following relationship:

$$\begin{bmatrix}[V(k\omega_{RF})]^e \\ [I(k\omega_{RF})]^e\end{bmatrix} = \mathbf{H}(k\omega_{RF}) \cdot \begin{bmatrix}[V(k\omega_{RF})]^i \\ [I(k\omega_{RF})]^i\end{bmatrix} \tag{4.10}$$

The knowledge of $[V(k\omega_{RF})]^e$ and $[I(k\omega_{RF})]^e$ allows determining the RF terminations at the extrinsic planes in terms of load and source impedances to guarantee the same operating condition measured at the current generator plane at low frequency.

Two aspects related to this methodology must be pointed out. First of all, the initial requirement for its application is the availability of a model of the device capacitive core ant its parasitic network. Therefore, one can object that a full model could be exploited, by using the current-generator model in place of the low-frequency measurements. Although there is no difference from a procedural point of view, exploiting measurements directly performed on the actual device makes it possible to fully gather the effects of low-frequency dispersion, with the only inaccuracies of the measurement system. The same level of accuracy is hardly reproduced by a model of the current generator, leading to errors in the expected performance.

Secondly, it is important to note that the design frequency can be chosen independently from the low-frequency measurement set. As a matter of fact, the same set can be used to predict the device performance at every microwave frequency, since the behavior of the current generator does not change by definition. The only elements to be determined are the displacement currents and the parasitic network effects. The only limitation is related to the maximum frequency for which their models provide accurate results.

The described methodology has been successfully applied to several power amplifier designs [5, 15-21], confirming its robustness.

To better understand the design methodology flow, an example of its application is reported in the following paragraph.

## 4.4. Identification of the optimum operation for a GaN HEMT in high-power amplifiers

In this example [24], the design methodology is applied to a 0.5x8x250-$\mu m^2$ GaN HEMT to predict its optimum performance operation. A class AB operation is considered with no harmonic tuning at the design frequency of 5.5 GHz.

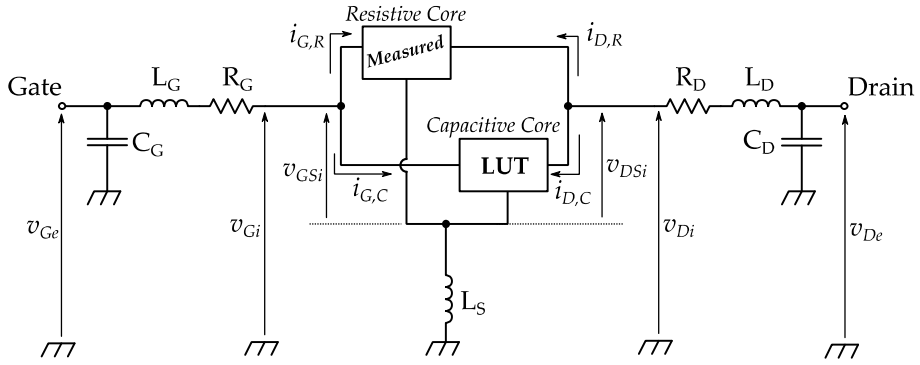



**Fig. 4.6** Equivalent model adopted for the GaN HEMT for the application of the design methodology. The values of the parasitic elements are: $L_G$ = 87.6 pH, $L_D$ = 65.8 pH, $L_S$ = 4.15 pH, $R_G$ = 0.939 Ω, $R_D$ = 0.784 Ω, $C_G$ = 50.2 fF, and $C_D$ = 8.99 fF.

### *4.4.1. Identification of the parasitic network and the capacitive core*

The first step consists in the identification of the capacitive core and the parasitic network of the device. To this end, multi-bias small-signal parameters (e.g., S-parameters) measured over a suitable range of frequencies have been used. The parasitic network was determined through cold-FET S-parameters [25, 26] according to the topology reported in Fig. 4.6, whereas the imaginary part of the intrinsic Y-parameters, obtained by de-embedding the parasitic elements from the measured S-parameters, was used to calculate the capacitive core, following a quasi-static approach.

Capacitance values were stored in a LUT but this is not the only possible choice, since any modelling approach can be used. In this case study, the LUT approach has been considered because of its high-level of accuracy (data are directly derived from measurements). A nonquasi-static model can also be used if the design frequency is closer to the maximum allowed for the device.

### *4.4.2. Low-frequency characterization*

In this example, the optimum operation for the selected device has to be determined. As mentioned, output power and efficiency are mainly defined by the I/V waveforms (or load conditions) at the current-generator plane. Indeed, because of its nature, the optimum performance is achieved with a pure resistive load-line [1, 2]. Therefore, a

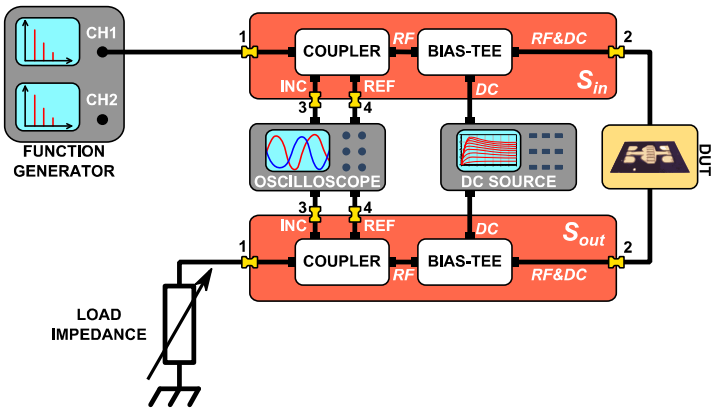



**Fig. 4.7** Low-frequency measurement setup with variable passive load termination.

low-frequency characterization based on the synthesis of resistive impedances at the current-generator plane can be considered sufficient for the aim of this case study.

According to this consideration, the low-frequency setup has been slightly modified, as reported in Fig. 4.7. A set of good-quality high-power resistors were connected in place of the function-generator channel devoted to the drain path. They allow to dissipate an output power up to 50 W and to speed up the measuring process since no tune of the drain incident-wave parameters must be done. This is an example of how the setup can be easily adapted to different conditions without altering its operation.

Low-frequency measurements were performed at 2 MHz considering load values ranging from 49 Ω to 134 Ω. The achieved data can be directly used to assess the optimum performance condition. In particular, the output power has been maximized under the constraint of a sufficiently high efficiency. According to Fig. 4.8, the optimum trade-off is guaranteed by a load impedance of 100 Ω at the current-generator plane, providing 38.7 dBm output power with 66.5% efficiency.

For each impedance, the measured intrinsic voltage phasors are available for the next step of the methodology.

### *4.4.3. Shift of low-frequency data at the design frequency*

Since the capacitive core is assumed strictly in parallel with the resistive core, they are subject to the same voltage phasors (in terms of magnitude and phase) measured at

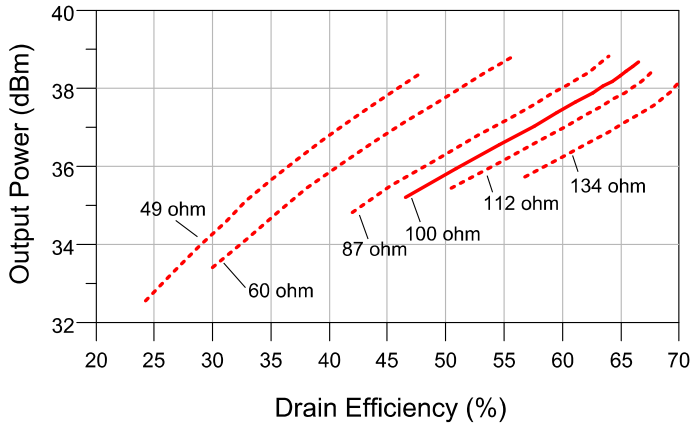



**Fig. 4.8** Output power as function of drain efficiency for different load conditions at the current-generator plane (frequency 2 MHz).

low frequency. Therefore, the voltage phasors, shifted at the design frequency of 5.5 GHz, have been applied to the capacitive core to calculate the displacement currents through the following expressions:

$$i_{G,C} = C_{11}\frac{dv_{GSi}}{dt} + C_{12}\frac{dv_{DSi}}{dt} \tag{4.11}$$

$$i_{D,C} = C_{21}\frac{dv_{GSi}}{dt} + C_{22}\frac{dv_{DSi}}{dt} \tag{4.12}$$

$[C_{ij}]_{i,j=1,2}$ being the matrix of the intrinsic nonlinear capacitances and $v_{GSi}$ and $v_{DSi}$ the time-domain intrinsic voltages measured at low-frequency and shifted at high frequency. In this particular case, equations (4.11) and (4.12) have been solved by using a nonlinear circuit simulator, although other approaches can be adopted (e.g., numerical computing software).

Results have been summed up with the resistive currents (shifted at 5.5 GHz as well considering their frequency independence) to obtain the total intrinsic currents ($i_{Gi}$ and $i_{Di}$) and then, by exploiting the equivalent-circuit description of the parasitic network, the extrinsic voltage and current phasors have been determined. In particular, the first step was the determination of the intrinsic voltages $v_{Gi}$ and $v_{Di}$ (see Fig. 4.6) through their phasors as:

$$V_{Gi}(k\omega_{RF}) = V_{GSi}(k\omega_{RF}) + jk\omega_{RF}L_S \cdot \left[I_{Gi}(k\omega_{RF}) + I_{Di}(k\omega_{RF})\right] \tag{4.13}$$

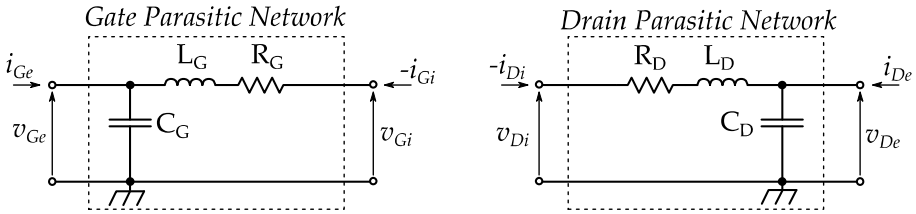



**Fig. 4.9** Parasitic networks as 2-port networks to be embedded.

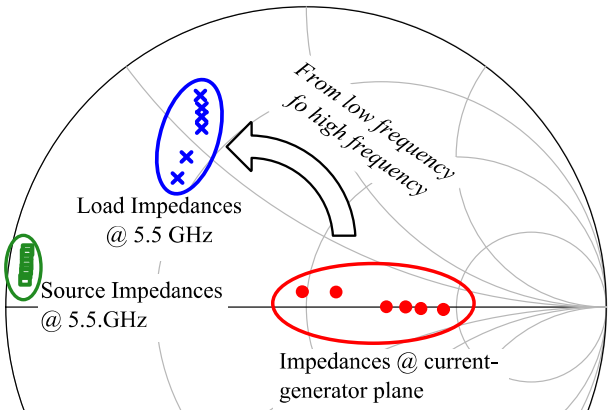



**Fig. 4.10** Impedances synthesized at low frequency at the current-generator plane (red dots), corresponding load (blue crosses) and source (green squares) impedances at the extrinsic plane for a fundamental frequency of 5.5 GHz.

$$V_{Di}(k\omega_{RF}) = V_{DSi}(k\omega_{RF}) + jk\omega_{RF}L_S \cdot \left[I_{Gi}(k\omega_{RF}) + I_{Di}(k\omega_{RF})\right] \tag{4.14}$$

The remaining part of the parasitic network can be represented as two 2-ports, as reported in Fig. 4.9, thus, by using their Y-parameters the extrinsic voltages ($v_{Ge}$ and $v_{De}$) and currents ($i_{Ge}$ and $i_{De}$) can be determined.

Finally, extrinsic source and load impedances corresponding to the current-generator operating conditions measured at low frequency can be calculated. In Fig. 4.10, the results are reported. The source impedances indicated in the plot guarantee large-signal conjugate matching at the device input port. In Table 4.1 the load conditions measured at the low-frequency plane and the predicted ones at RF are shown. The optimum impedance corresponding to 100 Ω at the current-generator plane becomes $Z_L$ = 10.8 + j28.6 Ω at the extrinsic plane at 5.5 GHz. In this case, the predicted maximum output power is 38.4 dBm with a drain efficiency of 62%.

TABLE 4.1. CORRESPONDENCE BETWEEN LOAD IMPEDANCES AT THE CURRENT GENERATOR PLANE AND AT THE EXTRINSIC PLANE

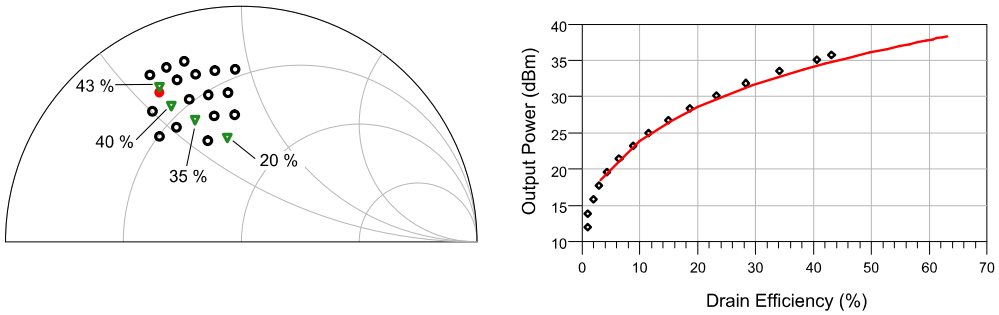
| *$Z_L$ at the current generator plane* | *$Z_L$ at the extrinsic plane* |
|---|---|
| 48 Ω | 14.2 + j19.3 Ω |
| 60 Ω | 13.4 + j22.6 Ω |
| 87 Ω | 12.1 + j27.4 Ω |
| 100 Ω | 10.8 + j28.6 Ω |
| 112 Ω | 9.75 + j29.4 Ω |
| 134 Ω | 8.16 + j30.3 Ω |

TABLE 4.2 HIGH-FREQUENCY LOAD-PULL RESULTS @ 5.5 GHZ

| *Drain efficiency* | *Load impedance* | *Output power* |
|---|---|---|
| 20% | 30.5 + j33.4 Ω | 31.1 dBm |
| 35% | 20.5 + j30.4 Ω | 35.0 dBm |
| 40% | 14.4 + j28.6 Ω | 35.6 dBm |
| 43% | 10.0 + j29.2 Ω | 35.7 dBm |

### *4.4.4. Validation of the high-frequency results*

To validate the design procedure, load-pull measurements have been carried out on the device over a proper grid of load impedances. To compare the results, measurement data have been analyzed to assess the optimum impedance in terms of maximum output power for constant levels of drain efficiency. As shown in Fig. 4.11a, as the output power increases, the optimum impedance moves toward the one predicted by the proposed methodology. In Table 4.2, output power and load impedance for each efficiency level are indicated. It is noteworthy that the high-frequency measured output power reaches lower levels than the ones expected from this technology, i.e., 5 W/mm. Indeed, such power levels are consistent with the results of our methodology. This discrepancy is due to the power limitation of the exploited high-frequency load-pull measurement setup, where the RF source is not able to provide enough input power to the DUT to reach output-power levels close to saturation. On the contrary,




(a) (b)

**Fig. 4.11** (a) Comparison between high-frequency load-pull data and methodology results. Green triangles represent the optimum power impedances for the indicated drain efficiency levels. The red filled dot is the optimum impedance obtained through the presented methodology. Empty dots represent the other impedances included in the high-frequency load-pull measured grid. (b) Output power vs drain efficiency at 5.5 GHz. High-frequency measurement (symbols) and methodology prediction (solid line) are reported for the optimum impedance.

this is not a big issue for the low-frequency measurement setup, where just a low-cost function generator is sufficient to impose the desired voltage waveform at the intrinsic gate-source port, being the input port of the DUT an open circuit. In any case, RF measurements are in good agreement with the results of the methodology; this can be appreciated in Fig. 4.11b, where the good coherence between RF measurements and predicted results is shown.

## 4.5. Multiharmonic characterization – Class-F load-pull contours

As mentioned in Paragraph 4.3, the nonlinear embedding methodology can be iterated over a large number of operating conditions measured at low-frequency. Following this procedure, it is possible to obtain load-pull data at microwave frequencies simultaneously guaranteeing the required current-generator behavior. In the following example [3], this potentiality is described by obtaining load-pull data for a device under class-F operation correctly synthesized at the current-generator plane. It is important to remark that this condition is not directly achievable with a high-frequency measurement setup.

For this application a 1.25-mm periphery 0.25-μm GaN-on-SiC HEMT has been chosen at a design frequency of 2.4 GHz. Its technology specifications are summarized in Table 4.3. The design frequency will be 2.4 GHz, which can be considered suf-

TABLE 4.3. 0.25-μm GAN HEMT TECHNOLOGY SPECIFICATIONS

| *Quantity* | *Value* |
|---|---|
| *Breakdown Voltage* | -70 V |
| *Pinch-off Voltage* | -4 V |
| $I_{DSS}$ | 1 A/mm |
| *Saturated Output Power* | 5 W/mm |

ficiently high for such a device. To validate the results, a prototype of a class-F amplifier operating within [2.3-2.5] GHz was realized by using the methodology predictions.

### *4.5.1. Multiharmonic low-frequency characterization*

The GaN HEMT was biased under class-AB condition ($V_{DS}$ = 32 V, $I_D$ = 10 mA). A low-frequency load-pull characterization of the device intrinsic resistive core was carried out by exploiting the active load-pull setup described in Chapter 1 with the control of the drain terminations up to the third harmonic component. The impedances synthesized at the fundamental frequency (i.e., 2 MHz) are shown in Fig. 4.12, whereas, for each one of them, the second harmonic impedance was settled to be a short circuit and the third one to be a high-impedance termination[§§] [1, 2].

Once the low-frequency characterization was concluded, several data as the output power and the drain efficiency are available and low-frequency load-pull contours can be drawn to evaluate the device performance. For this activity, the target was to optimize the output power close to the maximum theoretical value for this technology (i.e., 5 W/mm) with the maximum efficiency. For the output power, a value of 5 W (~ 37 dBm) has been considered a reasonable target. Nevertheless, not every measured impedance satisfies this requirement. In Fig. 4.12 it is pointed out that only

[§§] According to class-F theory, an open circuit should be synthesized at the third harmonic. However, from a practical point of view, an impedance sufficiently high with respect to the fundamental one is sufficient. As a matter of fact, the role of the third-harmonic termination is to minimize its correspondent current phasors with respect to the second-harmonic one.

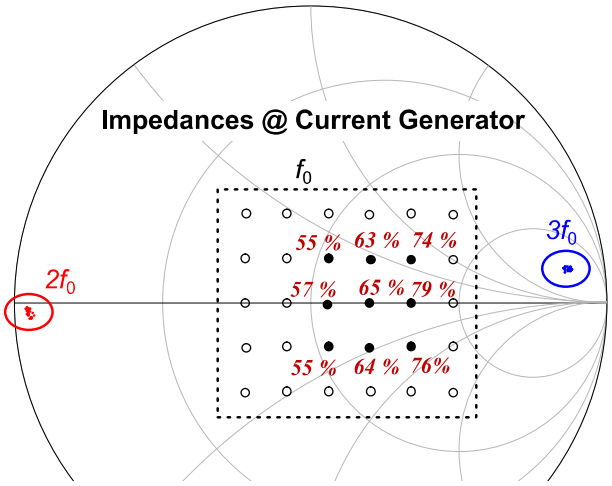
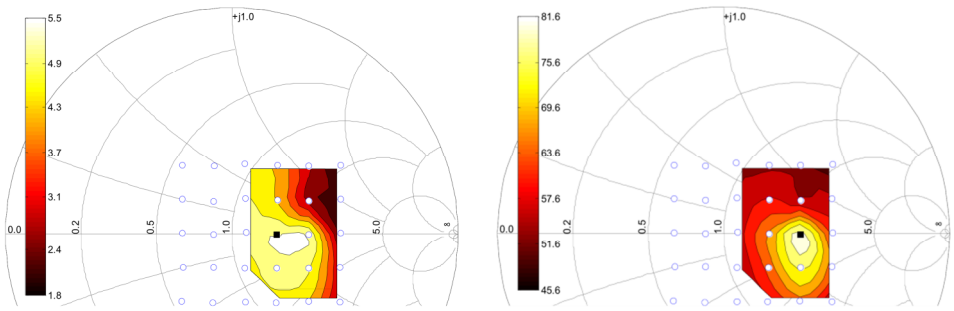



**Fig. 4.12** Grid of impedances measured at the fundamental frequency of 2 MHz (circles) for the 1.25-mm periphery 0.25-μm GaN HEMT biased at $V_{DS}$ = 32 V, $I_D$ = 10 mA. Impedances corresponding to an output-power level of at least 5 W and their corresponding efficiency values are shown with filled circles. The impedances synthesized at the 2nd and 3rd harmonics are also depicted.

nine impedances get the target and for each one the corresponding efficiency is indicated. The reason of this limitation is essentially related to reliability constraints since, for the remaining impedances, the compliances related to the maximum gate-source or gate-drain voltages are reached. In order to clarify this important aspect, Fig. 4.13 shows the output power and efficiency contours for a constant minimum value of the dynamic gate-drain voltage, i.e., $v_{GD,min}$ = -69 V, which is close to the breakdown voltage as reported in Table 4.3. In Fig. 4.13a it can be noticed that the maximum 5.5-W output power, corresponding to a 68.4% drain efficiency, is achieved at $Z^P_{L,CGP}$ = 75 Ω, whereas from Fig. 4.13b the optimal efficiency condition (81.6 %) is found at $Z^E_{L,CGP}$ = 103 Ω which corresponds to a 5.4-W output power. Since the target is to maximize the efficiency, obtaining as much power as possible, $Z^E_{L,CGP}$ can be considered the optimum condition. The optimum impedances at the fundamental and harmonics are reported in Table 4.4. As it can be seen, short and open circuits are synthesized at the second and third harmonic respectively.




(a) (b)

**Fig. 4.13** Constant output power (a) and drain efficiency (b) contours at constant $v_{GD,min}$ = -69 V. Measurements carried out at 2 MHz for a 1.25-mm periphery 0.25-μm GaN HEMT biased at $V_{DS}$ = 32 V, $I_D$ = 10 mA.

TABLE 4.4. MEASURED LOW-FREQUENCY DRAIN IMPEDANCES

| *Frequency* | *Impedances at the current generator plane* |
|---|---|
| *2 MHz* | 103 Ω |
| *4 MHz* | 0.3 + j0.1 Ω |
| *6 MHz* | 344 + j515 Ω |

Figure 4.14 shows the trajectories of the load-line synthesized at the electron-device intrinsic resistive core as a function of the input-power sweep. The measured load line for the highest input power value is compared with the one obtained by exploiting the foundry model, which predicts 6.9 W output power with 90% drain efficiency (dotted line in Fig. 4.14). This simulation was performed under the same condition of the low-frequency measurements. It is well evident the poor predictive capability of the foundry resistive-core model due to the lack of an accurate description of thermal and trapping phenomena [27-30].

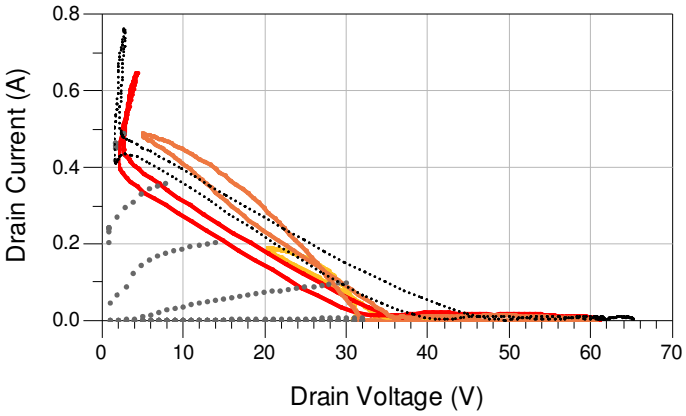



**Fig. 4.14** LF measurements (solid lines) for the load impedance $Z^{E}_{L,CGP}$ = 103 Ω as a function of increasing input power under class-F operation performed on a 1.25-mm periphery 0.25-μm GaN HEMT biased at $V_{DS}$ = 32 V, $I_D$ = 10 mA. The load-lines are superimposed to DC characteristics ($V_{GS}$ swept from -5 V to 0 V, step 0.5 V). The simulated load-line provided by the foundry model, which overestimates device performance, is also drawn (dotted line).

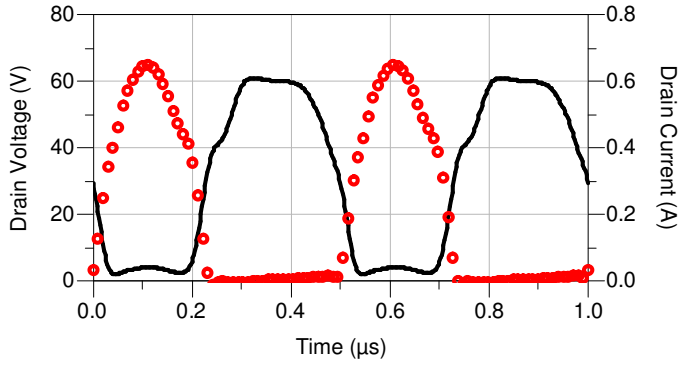
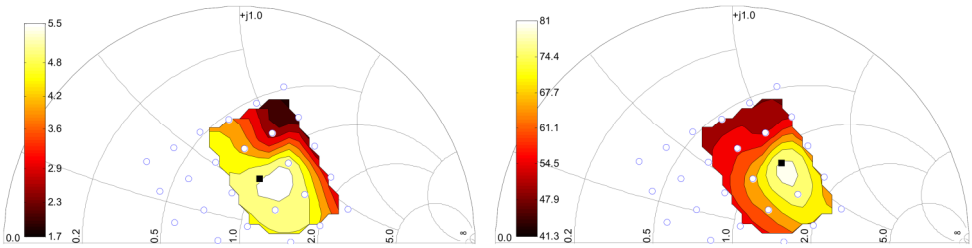



**Fig. 4.15** Low-frequency time-domain voltage (solid line) and current (symbols) waveforms at the device current-generator plane for the highest value of input power, corresponding to the synthesized class-F operating mode (loading condition of Table 4.4) performed on a 1.25-mm periphery 0.25-μm GaN HEMT biased at $V_{DS}$ = 32 V, $I_D$ = 10 mA.

Figure 4.15 shows the measured low-frequency time-domain voltage and current waveforms referred to the current-generator plane: it is well evident that such electrical variables satisfy the minimal-overlapping condition imposed by class-F operation.

### *4.5.2. From low-frequency to high-frequency*

According to the design methodology, the obtained low-frequency electrical variables corresponding to each termination of the grid in Fig. 4.12 can be elaborated in order to obtain the behavior of the selected class-F operating mode at the design fre-




(a) (b)

**Fig. 4.16** Grid of impedances at the fundamental frequency of 2.4 GHz obtained from the measurement grid in Fig. 4.12 for a 1.25-mm periphery 0.25-μm GaN HEMT (circles) biased at $V_{DS}$ = 32 V, $I_D$ = 10 mA. (a) Constant output-power contours and (b) constant efficiency contours for $v_{GD,min}$ = -69 V.

quency of 2.4 GHz. In this case, the foundry model (EE_FET3 [31]) has been exploited for both the capacitive-core and the linear-extrinsic-parasitic-network behavior.

Figure 4.16 shows the grid of impedances at the fundamental frequency of 2.4 GHz, resulting from the computation of the low-frequency grid reported in Fig. 4.12.

At this point, all the information in terms of output power, efficiency, PAE, gain, etc., is available at the design frequency of 2.4 GHz and can be conveniently exploited to find the optimal impedance.

As shown for the low-frequency measurements ($f$ = 2 MHz), Fig. 4.16 reports the output power and drain efficiency contours for constant $v_{GD,min}$ = -69 V[***]. In Fig. 4.16a, a maximum output power of 5.5 W and a corresponding 68 % drain efficiency are achieved at $Z^P_{L,EP}$ = 50.6 + j29.9 Ω, whereas from Fig. 4.16b the optimal efficiency condition is found at $Z^E_{L,EP}$ =57 + j45.4 Ω, which corresponds to 81% drain efficiency and 5.4-W output power. It is evident that the impedance providing the best efficiency for this application is represented by $Z^E_{L,EP}$, which corresponds to the impedance $Z^E_{L,CGP}$ at the current-generator plane.

Table 4.5 shows the optimum extrinsic load terminations at the frequency of 2.4 GHz compared to the ones at the current-generator plane. It must be outlined that the latters are not directly deducible from the extrinsic data. As an example, the ob-

[***] It is worth noticing that this value is referred to the intrinsic voltages. This kind of information cannot be directly evaluated from high-frequency measurements.

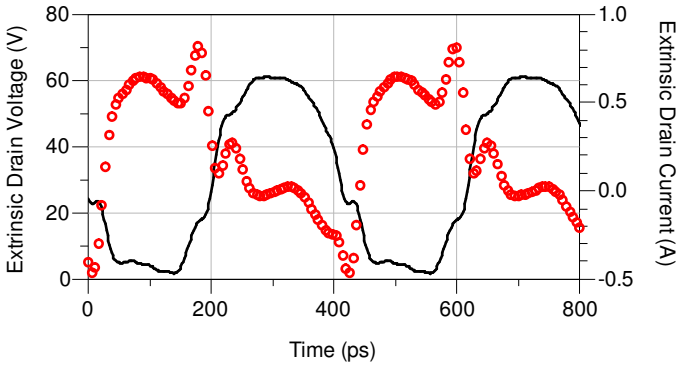


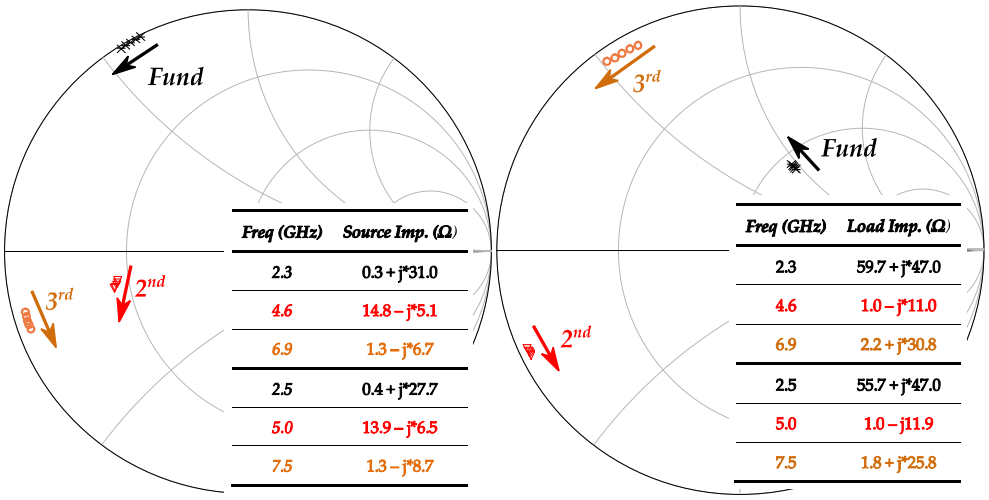

**Fig. 4.17** Extrinsic time-domain voltage (continuous line) and current (circles) waveforms at the device drain extrinsic terminal for the highest input power value, at the design frequency of 2.4 GHz (loading condition of Table 4.5) obtained for a 1.25-mm periphery 0.25-μm GaN HEMT biased at $V_{DS}$ = 32 V, $I_D$ = 10 mA.

TABLE 4.5. COMPARISON BETWEEN THE SELECTED CURRENT GENERATOR LOAD IMPEDANCEAND THE EXTRINSIC ONE AS A FUNCTION OF FREQUENCY

| *Impedances at the current generator plane* | *Frequency* | *Impedances at the extrinsic plane* |
|---|---|---|
| 103 Ω | *2.4 GHz* | 57 + j 45.4 Ω |
| 0.3 + j0.1 Ω | *4.8 GHz* | 1.4 – j 11 Ω |
| 344 + j515 Ω | *7.2 Ghz* | 2.3 + j 29.7 Ω |

tained third-harmonic high-impedance condition at the intrinsic device, typical of class-F operating mode, is not easily deducible from its extrinsic value. This is the reason why large-signal measurements carried out at the design frequency cannot give useful information at the current-generator plane, unless a rigorous nonlinear de-embedding procedure is adopted [11-13].

Moreover, as clearly shown in Fig. 4.17 where the extrinsic voltage and current time-domain waveforms at the design frequency of 2.4 GHz are depicted, it is very difficult to assert that the GaN HEMT is working in class-F operation, whereas this is well evidenced by looking at the same electrical variables referred to the current generator plane (Fig. 4.15).




(a) (b)

**Fig. 4.18** Source (a) and load (b) impedances evaluated in the frequency range 2.3 – 2.5 GHz: fundamental (stars), second (triangles) and third (circles) harmonic termination trajectories for a 1.25-mm periphery 0.25-µm GaN HEMT biased at $V_{DS}$ = 32 V, $I_{DS}$ = 10 mA.

### *4.5.3. Design of the class-F power amplifier*

The data collected at low frequency can be exploited to obtain information at whatever frequency is needed, since it is sufficient to iterate the methodology for each value of interest, starting from the same set of low-frequency measurements.

To validate the results, a prototype of a class-F power amplifier has been realized within the bandwidth [2.3 - 2.5] GHz. Extrinsic variables have been computed in this frequency range and the trajectories of the fundamental-, second- and third-harmonic input and output impedances are depicted in Fig. 4.18 where their values at the extremes of the considered bandwidth are also reported in the insets. The source impedance has been chosen equal to the conjugate of the large-signal electron-device input impedance, over the whole bandwidth. This is a straightforward operation since the methodology provides the current and voltage waveforms at the extrinsic plane for each power level.

The designed class-F GaN PA was manufactured on a high-frequency laminate. Fundamental and harmonic target impedances have been synthesized in the frequen-

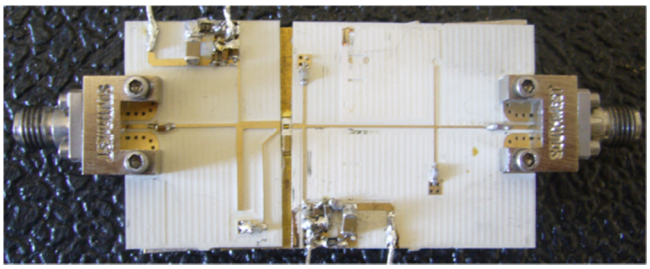


**Fig. 4.19** Realized GaN class-F hybrid power amplifier.

cy range 2.3 – 2.5 GHz by means of simple topologies for both the input and output matching network. It must be observed that, once the trajectories over the frequency of fundamental and harmonic impedances have been computed, an arbitrarily large bandwidth could be obtained by increasing the topological complexity of the matching networks. However, for the aim of this prototype, such a solution is unnecessary.

A photograph of the realized class-F power amplifier is shown in Fig. 4.19. It delivers an output power greater than 36 dBm (~ 4 W) with a drain efficiency greater than 55% over the frequency range of 2.3 – 2.5 GHz, with 4.9 W (36.9 dBm) maximum power and 74% efficiency at 2.45 GHz. Moreover, if the power amplifier bandwidth is considered in the frequency range 2.375 – 2.475 GHz, the measured efficiency is always greater than 70 %, while the output power is never lower than 4.9 W (36.9 dBm).

With the aim of comparing the experimental performance of the power amplifier with the predicted one, which is referred to the device ports, both measured output power and drain efficiency were de-embedded from the losses of the output matching network. Figure 4.20 shows the comparison between the performance of the power amplifier with and without considering the matching networks. As a matter of fact, an output power greater than 4.4 W (36.4 dBm) with a drain efficiency greater than 61% are registered over the band [2.3 – 2.5] GHz at the power-amplifier plane. On the other hand, the peak value of the output power and drain efficiency at electron device plane are, in this case, 5.5 W (37.4 dBm) and 84% respectively. Besides, in the range of frequencies [2.375 -2.475] GHz, efficiency is always greater than 80% and the output power is never smaller than 5.4 W (37.3 dBm). Experimental performance at the elec-

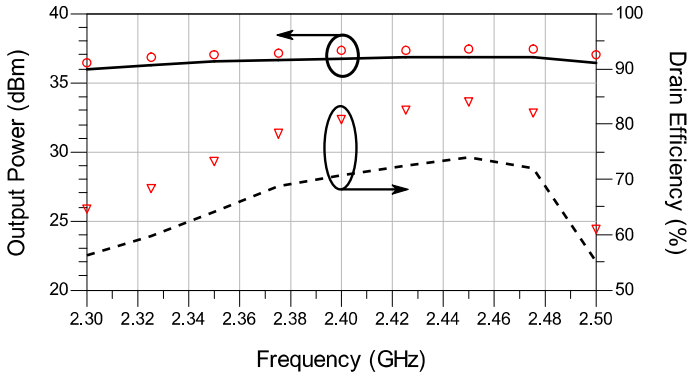



**Fig. 4.20** Measured output power and drain efficiency of the realized class-F power amplifier across the bandwidth [2.3 – 2.5] GHz at the power-amplifier reference plane (bold and dotted lines respectively) and electron device plane (circles and triangles respectively).

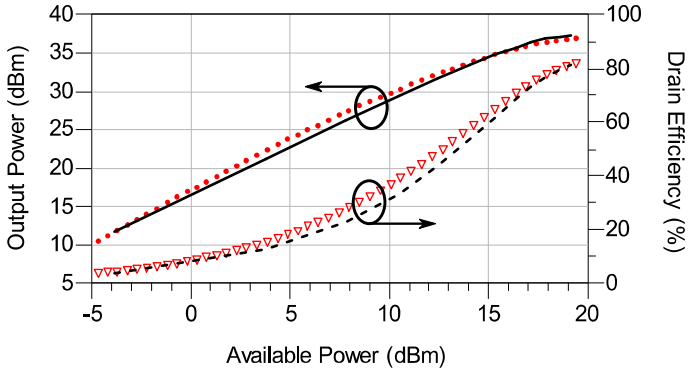



**Fig. 4.21** Measured output power and drain efficiency of the realized class-F power amplifier at electron device plane (dots and triangles respectively) compared to the ones predicted by the design methodology (solid line and dashed line respectively).

tron-device reference plane is in very good agreement with the predicted one (37.3 dBm and 81%), based on the low-frequency load-line characterization.

Figure 4.21 shows the comparison between measured and predicted output power and drain efficiency sweeps at 2.45 GHz; at this frequency the impedance values reported in Fig. 4.18 have been more accurately synthesized. The excellent agreement confirms the validity of the proposed design technique.

## 4.6. Conclusion

In this Chapter the problem of determining the optimum electron device operating condition for power amplifier design has been discussed. The high-efficiency

class-F power amplifier has been reviewed as an example of a theoretical approach, highlighting some problems of practical feasibility.

The conventional design approach based on load-pull measurements at microwave frequency has been described, pointing out the limitations of the setups. In particular, apart for power and frequency constraints, the problem of assessing information at the current-generator plane for determining the actual operating condition of the device under test has been identified as a critical aspect since it is the reference plane the design theories are referred to.

An alternative design approach based on the nonlinear embedding technique has been considered. Starting from low-frequency measurements, it is possible to estimate the high-frequency device performance by exploiting a model of its intrinsic capacitances and parasitic network and calculating the corresponding extrinsic conditions to be synthesized.

As an example, this technique has been successfully applied for the prediction of the optimum performance operation for a 0.5-8x250-$\mu m^2$ GaN HEMT device for which a small set of low-frequency measurements turned out to be sufficient to assess the optimum load condition at the current-generator plane. The technique has been validated for a design frequency of 5.5 GHz by using conventional load-pull measurements.

Finally, the methodology has been exploited, for the first time, to estimate the performance of a 1.25-mm periphery 0.25-μm GaN-on-SiC HEMT under a high-efficiency condition (i.e., class-F) at the design frequency of 2.4 GHz. The low-frequency setup has been used to perform measurements at 2 MHz at the current-generator plane imposing the load terminations defined by the theory. Then, the high-frequency behavior at 2.4 GHz corresponding to the low-frequency measured load lines has been assessed through the model of both the capacitive core and the parasitic network of the device, obtaining load-pull contours under class-F operating condition.

The optimum case in terms of efficiency has been identified, and to validate the whole procedure, a prototype of a power amplifier has been realized by exploiting the design methodology predictions. Measured data on the power amplifier were in

excellent agreement with the expected ones, confirming the validity of the adopted approach.

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[1] **G. Bosi**, E. Cipriani, P. Colantonio, F. Giannini, A. Raffo, and G. Vannini, "Gate waveform effects on high-efficiency PA design: an experimental validation," *9th European Microwave Integrated Circuits Conference (EuMIC)*, Rome, Italy, Oct. 2014.

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