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A Thorough Evaluation of GaN HEMT Degradation under Realistic Power Amplifier Operation

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Abstract: In this paper, we experimentally investigate the effects of degradation observed on 0.15-µm GaN HEMT devices when operating under realistic power amplifier conditions. The latter will be applied to the devices under test (DUT) by exploiting a low-frequency load-pull characterization technique that provides information consistent with RF operation, with the advantage of revealing electrical quantities not directly detectable at high frequency. Quantities such as the resistive gate current, play a fundamental role in the analysis of technology reliability. The experiments will be carried out on DUTs of the same periphery considering two different power amplifier operations: a saturated class-AB condition, that emphasizes the degradation effects produced by high temperatures due to power dissipation, and a class-E condition, that enhances the effects of high electric fields. The experiments will be carried out at 30 °C and 100 °C, and the results will be compared to evaluate how a specific RF condition can impact on the device degradation. Such a kind of comparison, to the authors' knowledge, has never been carried out and represents the main novelty of the present study.

Keywords: device degradation; gallium nitride; HEMT; load-pull measurements; microwave frequency; power amplifier; reliability; stress measurements

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1. Introduction

The unique properties of Gallium Nitride (GaN) technology make it one of the enabling factors pushing forward the development of microwave electronics, ranging from mobile communication and radar systems to satellite communications [1–7]. The success of this technology lies in the physical properties of GaN [8,9], such as its high electron mobility and the wide bandgap. These allow high-frequency operation, high power density, and the ability to sustain high electric fields, providing intrinsic robustness to the devices [10].

In this context, the analysis of the technology reliability plays a fundamental role to identify and understand the mechanisms of degradation of the electron devices that can lead to a limited performance or even to a premature failure, especially when the technology is pushed towards its limits to fulfill the challenging specifications of the demanding emerging applications.

DC stress tests are a well-established technique adopted for investigating technology reliability [11–15]. In these tests, a high-voltage bias point is applied to the device, sometimes gradually, to activate specific degradation mechanisms, such as hot-electrons (i.e., carriers with a mean kinetic energy greater than the lattice thermal energy [16]), a typical issue in GaN devices [17,18], especially under large-signal dynamic operation, when the transistor continuously switches between the on and the off state [19]. This type of experiment is easy to implement since it requires simple instrumentation and provides

accurate results. Nevertheless, if we consider the typical applications of microwave devices, DC operation is far from being a realistic condition, and RF stress tests are usually required [20–23]. It has been demonstrated that the application of a realistic stress condition can lead to very different results with respect to DC stress tests because of the degradation mechanisms that can be triggered or accelerated by RF signals [24,25]. Although RF tests provide a better understanding of the device reliability issues, the setups required for this characterization present some limitations. First, their complexity is higher than that of DC setups, which directly impacts the accuracy of the measurements [26–28]. Indeed, proper calibration procedures are required at RF [28–30], and they need to remain valid for the entire duration of the stress tests, which can reach hundreds or even thousands of hours. Second, the need of RF instrumentation increases the overall costs of the experiments, considering that such long-lasting measurements require dedicated setups, which become unavailable for other activities when stress tests are ongoing. Another limitation is related to the levels of power manageable at RF. In fact, if dealing with complete circuits, e.g., power amplifiers, could be relatively easy at high frequencies, the investigation of the technology's reliability issues needs to be performed at the transistor level, which can pose significant challenges when large peripheries need to be characterized, in terms of both power management and stability [27,29].

In this paper, we propose a characterization technique for reliability investigation that tries to overcome the aforementioned limitations, whilst, nevertheless, providing accurate and consistent results directly comparable with RF stress results. It is based on a time-domain load-pull setup [31] operating at a few megahertz, that mixes the advantages of low-frequency measurements and the possibility of stressing the device under test setting realistic operating conditions, thereby enabling access to data not directly available at microwaves [32,33]. We will prove the effectiveness of the characterization technique by showing the results of two stress experiments carried out using samples from a 0.15-µm GaN HEMT technology, where devices with the same periphery are tested under different realistic operating conditions, i.e., a class-AB operation and a class-E operation, with the aim of highlighting their different impact from a degradation perspective.

The paper is organized as follows. Section 2 exhaustively describes the characterization technique, focusing on the capabilities of the adopted setup and its advantages when compared with other characterization techniques. Section 3 describes the general implementation of the stress measurement, whereas the details on the experiments carried out with this technique will be given in Section 4. In Section 5, the measurement results will be presented, whereas conclusions will be drawn in Section 6.

2. Characterization Technique

The proposed technique for evaluating the degradation effects on microwave transistors is based on the exploitation of low-frequency time-domain load-pull measurements. The term "low frequency" as defined herein refers to an operating frequency in the megahertz range, at which the microwave device behaves approximately as a "resistive" component, since the reactive effects associated with the parasitic elements and the intrinsic nonlinear capacitances produce negligible effects (Figure 1) [33]. This enables the access to electrical quantities that cannot be directly monitored under a microwave regime, such as the resistive gate current, i.e., the current flowing through the gate Schottky junction in a HEMT when excited under forward and/or reverse conduction. This quantity is usually hidden at microwave frequencies due to contributions of the reactive currents, which are orders of magnitude higher, leaving the average gate current as the only indicator related to the Schottky junction conduction regime. Nevertheless, this might lead to misleading information. As an illustrative example, Figure 2 shows two different gate current waveforms having the same average value but representing very different conditions. The blue waveform shows only the forward conduction of the Schottky junction (i.e., the positive current), whereas the red one also exhibits the reverse conduction, with a consequent increase of the forward current to keep the average value constant. Clearly, the latter is

a more critical condition for the device, but it is impossible to infer only based on the average current.

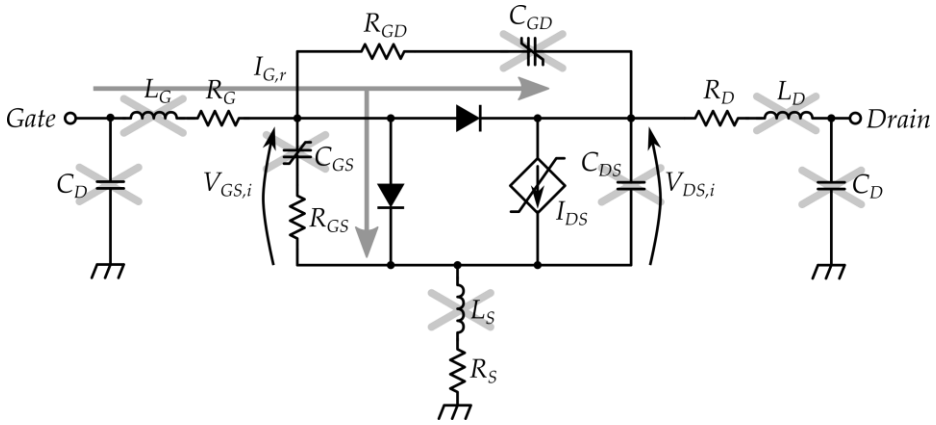

Figure 1. Equivalent-circuit model of a microwave field-effect transistor operating at a low frequency.

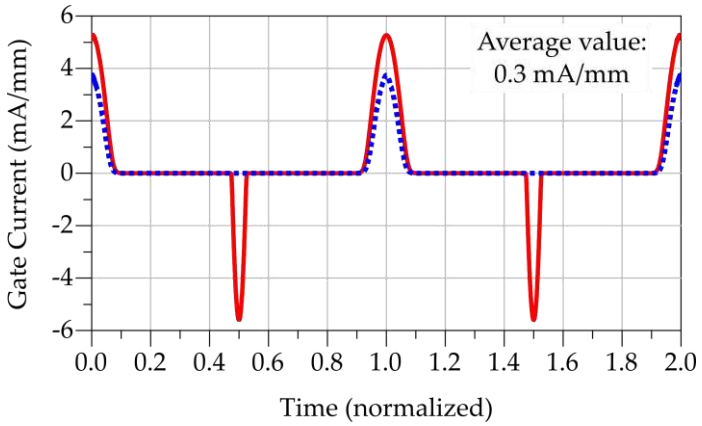

Figure 2. Examples of gate current waveforms having the same average value but representing very different conditions: forward and reverse conduction (red line), and only forward conduction (blue line).

Operating at a low frequency also enables the direct access to the so-called current-generator plane of the transistor, i.e., the intrinsic active part of the device. Power amplifier design techniques are generally related to this reference plane, defining the waveforms and/or the load terminations that the transistor current generator must experience to implement a specific class of operation [34,35]. The direct access to this plane enables the possibility of accurately controlling and monitoring the operating condition of the device by properly setting the input signals and the load conditions.

The choice of an operating frequency in the megahertz range for the characterization of microwave devices also allows one to account for the so-called low-frequency dispersion phenomena, i.e., the effects of thermal and trapping phenomena, which influence the electrical characteristics of the transistor [36–40]. Thermal effects depend on the junction temperature, i.e., the temperature that the device channel reaches during operation because of the power dissipation. Trapping phenomena are related to the presence of electron traps into the layers of material composing the transistor and consisting of energy levels that the carriers can occupy, being subtracted from conduction. These phenomena depend on the electric fields applied to the device, which are strictly related to the operating condition, especially in GaN devices where fast-trapping is an unavoidable issue connected to the maximum field instantaneously applied to the transistor [41]. Thermal and trapping effects are intrinsically intertwined [39,42,43] and are characterized by time constants relatively

low when compared to the timing of a microwave signal [33,36,39,40], as well as that of the low-frequency characterization. Therefore, the data gathered from the low-frequency measurements are consistent with the microwave behavior of the device, being the cut-off frequency of these effects below a few megahertz.

The schematic of the setup that implements the measurement technique is reported in Figure 3. The device under test (DUT) is biased by a DC source measure unit (SMU, HP 4155B) with a high resolution (4 μV; 20 fA) and accuracy (V: 0.05%, I: 0.2%). On the input side, a commercial bias tee is used (Minicircuit ZX85-12G-S+, frequency range: 200 kHz–12 GHz), whereas on the output side a dedicated bias tee has been designed to support high-power levels (frequency range: 200 kHz–200 MHz, maximum voltage: 100 V, maximum current: 2 A, and power handling: 30 W). They provide DC-to-AC isolation and prevent low-frequency instabilities. Incident and reflected waves at the DUT ports are separated by two dual-directional couplers (frequency range: 10 kHz–400 MHz) and sent to a 12-bit 350-MHz 4-channel oscilloscope (Tektronix MSO54) for the acquisition. The input signal is provided by an arbitrary function generator (Tektronix AFG 3252). Regarding the load condition, it is important to stress that, by operating at a few megahertz, we can directly control the current-generator load. Therefore, once the class of operation to be investigated is defined, we can know and synthesize the corresponding load condition at the fundamental and harmonic frequencies. To this purpose, we designed and produced an electronically controllable tuner coupled with a frequency multiplexer, which controls the load impedance up to the third harmonic, allowing the synthesis of both conventional and high-efficiency classes of operation that require a harmonic manipulation of the load (e.g., class-F conditions). In case this is not sufficient, we can easily design a customized board that also implements the terminations required for the characterization at higher harmonics (if required) which can also be dimensioned to sustain high power levels, thus enabling the possibility of characterizing devices with very large peripheries.

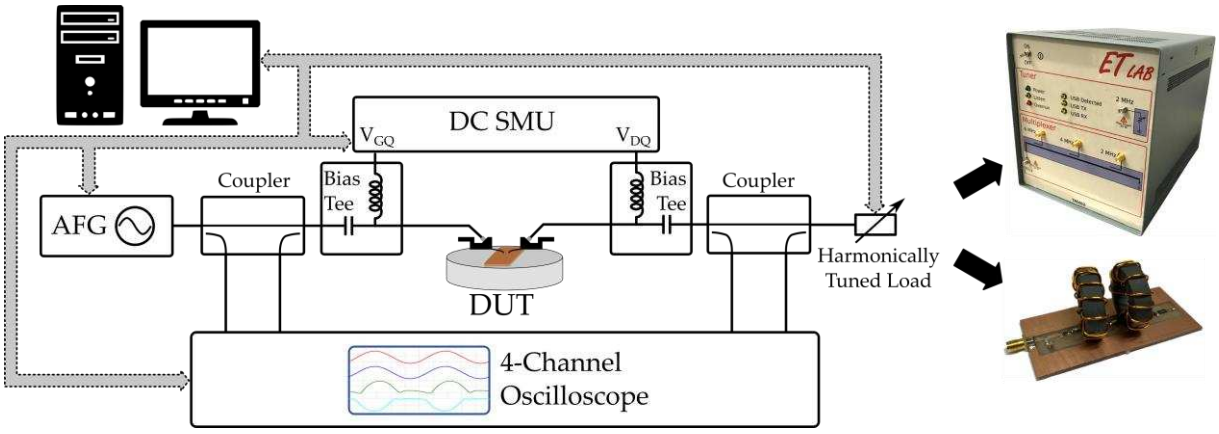

Figure 3. Block diagram of the low-frequency time-domain load-pull setup used for the characterization of microwave devices.

The setup is fully controlled by an internally developed software, that includes the possibility of implementing a stress-measurement routine to evaluate the degradation effects of the specific operating condition applied to the DUT. In this context, an important role is played by the calibration, which must be stable over time. This is easily achieved at megahertz frequencies, where the time-varying characteristics of instruments and components have negligible effects and provide a stable system for long periods of time.

3. Implementation and Definition of the Stress Measurement

The software controlling the measurement setup allows the user to organize a set of automatic measurements that will be carried out sequentially on the DUT. The user can choose between *stress measurements* and *control measurements*. In the first case, a defined

operating condition is applied to the DUT for a certain period of time, during which the main electrical quantities of interest are periodically monitored and sampled. The control measurements, instead, are thought to be carried out in between stress sessions to check the status of the DUT under operating conditions different from the one selected for the stress. Stress measurements can be chosen among:

- DC stress: a bias point is applied to the DUT for a time T_{stress}, during which the DC currents and voltages are periodically measured with a sampling time $T_{s,DC}$. In this case, no signal is applied to the DUT.
- Low-frequency stress: a large-signal operating condition at a low frequency is applied to the DUT for a time T_{stress}, during which both average currents and voltages as well as the incident and reflected waveforms are periodically measured. The sampling time for the DC quantities ($T_{s,DC}$) and for the waveforms ($T_{s,AC}$) can be different.

The available control measurements are:

- DC measurements: DC I/V characteristics are measured over a grid of bias points defined by the user.
- Low-frequency measurements: a large-signal low-frequency characterization is carried out on the DUT. The investigated condition can be different with respect to the one used for the stress measurement and the user can choose among a single load line, a power sweep, a load sweep or both.

Although the software provides great flexibility in the definition of the measurement sequence, the typical choice, which has been used also for the characterization presented in this paper, is schematically depicted in Figure 4. A preliminary set of control measurements is carried out on the DUT to obtain its initial state. Then, the total stress time is divided into several stress sessions followed by intermediate control measurements to evaluate the degradation of the DUT under different conditions and to monitor the evolution of its state. Eventually, a final set of control measurements is carried out to characterize the final state of the DUT.

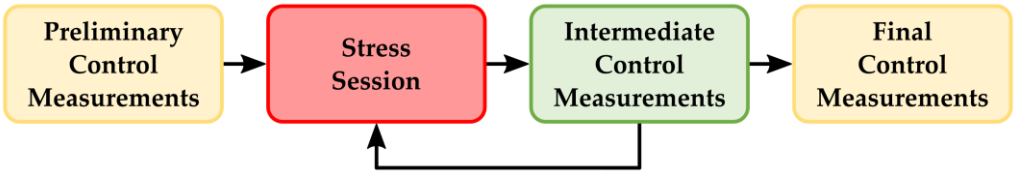

Figure 4. Typical sequence for a stress experiment.

4. Measurement Description

The aim of this experiment is to verify how different operating conditions act on the device degradation. Therefore, we selected two samples from the same 0.15 µm gallium nitride HEMT technology with 600 µm total periphery and characterized each of them with a different stress condition. A preliminary characterization of the technology, which is not reported here for the sake of brevity, has shown an extremely low level of process dispersion between samples, which was necessary to guarantee a fair comparison between the selected samples.

The investigated stress conditions were selected in order to emphasize two possible degradation mechanisms. The first one puts the device under thermal stress, by exploiting a large-signal condition with a high level of power dissipation. To this aim, we selected the tuned-load class-AB operation [35,44] under saturated output power. The second one, on the contrary, has a lower level of power dissipation but forces the device to sustain high electric fields. That is a class-E condition [45,46], which is characterized by a load line that reaches very high drain voltage values [47,48]. We want to point out that the effects of high temperature and electric fields can be (and usually are) investigated by DC measurements. Nevertheless, that condition is not realistic, whereas the low-frequency characterization

provides data under nonlinear dynamic operation that could be directly related to the microwave performance of the device.

Each stress condition was initially applied to a fresh device for a total time of 60 h, keeping the backside temperature at 30 °C. The total stress time was divided into eight shorter sessions of different durations, with DC control measurements in between. Then, the same measurement was repeated on each sample with the same timings but whilst increasing the substrate temperature up to 100 °C.

We report a summary of the measurement sequence in Table 1, whereas the details of the two stress conditions applied to the devices are reported in Table 2. The latter are the results acquired at the very beginning of the measurement at 30 °C, corresponding to the waveforms reported in Figure 5. Figure 5c clearly represents one of the advantages of the low-frequency characterization, i.e., the acquisition of the resistive gate current waveform. In the class-AB condition under saturated power, the forward conduction of the gate junction is evident, with a maximum instantaneous value of about 9 mA/mm. Under class-E operation, there is no forward conduction, but the drain voltage reaches a maximum value that is 63% higher with respect to the class-AB operation.

Table 1. Summary of the stress measurement sequence.

Phase	Description	Details
Preliminary/Final Control Measurements	Full DC I/V Characteristics	V_G = −4–2 V, step 0.5 V, V_D = 0–30 V, step 2 V
	DC I_G—V_D Transcharacteristic	V_G = −4 V, V_D = 0–30 V, step 0.5 V
	DC I_D—V_G Transcharacteristic	V_G = −4–2 V, step 0.1 V, V_D = 4 V
Stress Sessions	Low-Frequency Tuned-Load Class AB	60 h total stress time divided into 8 sessions
	Low-Frequency Class-E	(1 h–1 h–4 h–6 h–12 h–12 h–12 h–12 h)
Intermediate Control Measurements	DC I_G—V_D Transcharacteristic	V_G = −4 V, V_D = 0–30 V, step 0.5 V
	DC I_D—V_G Transcharacteristic	V_G = −4–2 V, step 0.1 V, V_D = 4 V

Table 2. Stress conditions applied at 30 °C.

Parameter	Symbol	Tuned-Load Class AB	Class-E
Quiescent Gate Voltage	V_{GQ}	−1.8 V	−1.9 V
Quiescent Drain Voltage	V_{DQ} *	28 V	28 V
Quiescent Drain Current	I_{DQ}	80 mA/mm	60 mA/mm
Fundamental Frequency	f_0	2 MHz	2 MHz
Load	Z_L	60.5 + j4.7 Ω · mm @ f_0	85.3 + 112 Ω · mm @ f_0
		4.6 − j0.2 Ω · mm @ $2f_0$	35.8 − 144 Ω · mm @ $2f_0$
		3.7 + j0.4 Ω · mm @ $3f_0$	6.40 − j64.0 Ω · mm @ $3f_0$
Average Gate Current	I_{G0}	0.63 mA/mm	≈0 mA/mm
Average Drain Current	I_{D0}	285 mA/mm	185 mA/mm
Input Power Available	P_{av}	16.3 dBm	14.9 dBm
Output Power	P_{out}	5.1 W/mm	3.5 W/mm
Dissipated Power	P_{diss}	2.7 W/mm	1.4 W/mm
Drain Efficiency	η_D	65%	67.8%
Maximum Drain Voltage	v_{Dmax}	53.2 V	86.7 V

* Suggested by the foundry.

The load lines synthesizing the two classes of operation, i.e., tuned-load class AB and class E, were not selected with the aim of designing best-in-class amplifiers, but in order to evidence the theoretical differences existing between the two classes. In particular, the investigated load lines enforced a nonlinear dynamic regime for the device, showing a different drain-gate voltage peak, and the conduction of the Schottky junction, as well as efficiency and output power level.

The variations in the RF performance, expected during a degradation experiment, could be partly related to some drift of the load condition during such a long-lasting characterization. To manage this issue, the adopted load terminations were carefully

designed to minimize the impact of the operating condition (e.g., dissipated power) on their value. Also, external factors, such as the ambient temperature, were controlled to limit their influence on the circuits implementing the load. Indeed, the load condition, which can be monitored directly from the acquired data, demonstrated an excellent stability, and its variations were limited to less than 1 Ω for both the selected stress conditions at both the fundamental and harmonics.

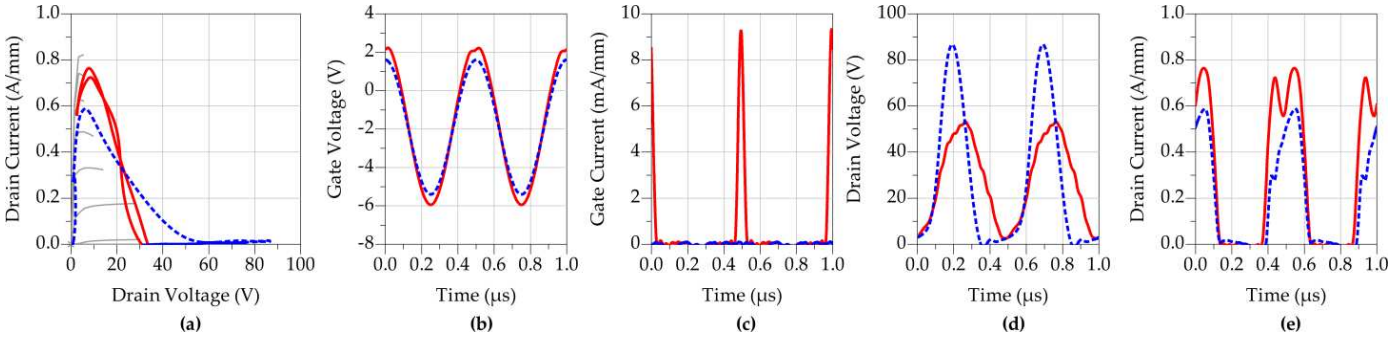

Figure 5. Investigated stress conditions described in Table 1, i.e., tuned-load class AB (red continuous lines) and class E (blue dashed lines): (**a**) load lines, (**b**) gate voltage waveforms, (**c**) gate current waveforms, (**d**) drain voltage waveforms, and (**e**) drain current waveforms.

5. Experimental Results

In the following six subsections, we will describe the achieved experimental results for each of the investigated stress conditions and compare them to analyze how they impact differently on the device degradation.

5.1. Tuned-Load Class-AB Stress at 30 °C

The stress condition has been applied to the DUT at 30 °C for a total of 60 h. We report the measured data in Figure 6, where both the waveforms and the performance are shown over the stress time. We can observe a slight variation in the load line (Figure 6a), mainly due to a reduction in the drain current, visible in Figure 6c. This translates into a decrease in the output power from 5.14 W/mm to 5.00 W/mm (–2.7%), and in the drain efficiency, from 65% to 64.4%, as shown in Figure 6i,j, respectively. Concerning the input side, no significant change was observed for the gate voltage waveform, whereas the peak of the gate current tended to decrease with the stress time from 9.3 mA/mm to 8.5 mA/mm (–8.6%), as depicted in Figure 6f, reducing the average gate current consequently from 634 µA/mm to 562 µA/mm (–11.4%, Figure 6g).

It is worth highlighting that the average currents, especially on the gate side, presented some sudden increases. This behavior was caused by the temporary suspension of the stress condition to perform the intermediate control measurements. During this time, the device experienced some recovery because of the change in the applied operating condition. Nevertheless, such a recovery was not permanent, since, as clearly shown in Figure 6g, after a brief transient, the data aligned to the previous data. This behavior was independent of the applied stress condition and, therefore, is present in all the results shown in the following.

In Figure 7, we report the data collected from the DC control measurements executed in between stress sessions. We note a mild reduction of the saturated drain current from 851 mA/mm to 833 mA/mm (−2.1%, Figure 7b) and a small variation of the threshold voltage, here represented in Figure 7c, where the gate voltage that provides a drain current of 100 mA/mm is reported as function of the stress time.

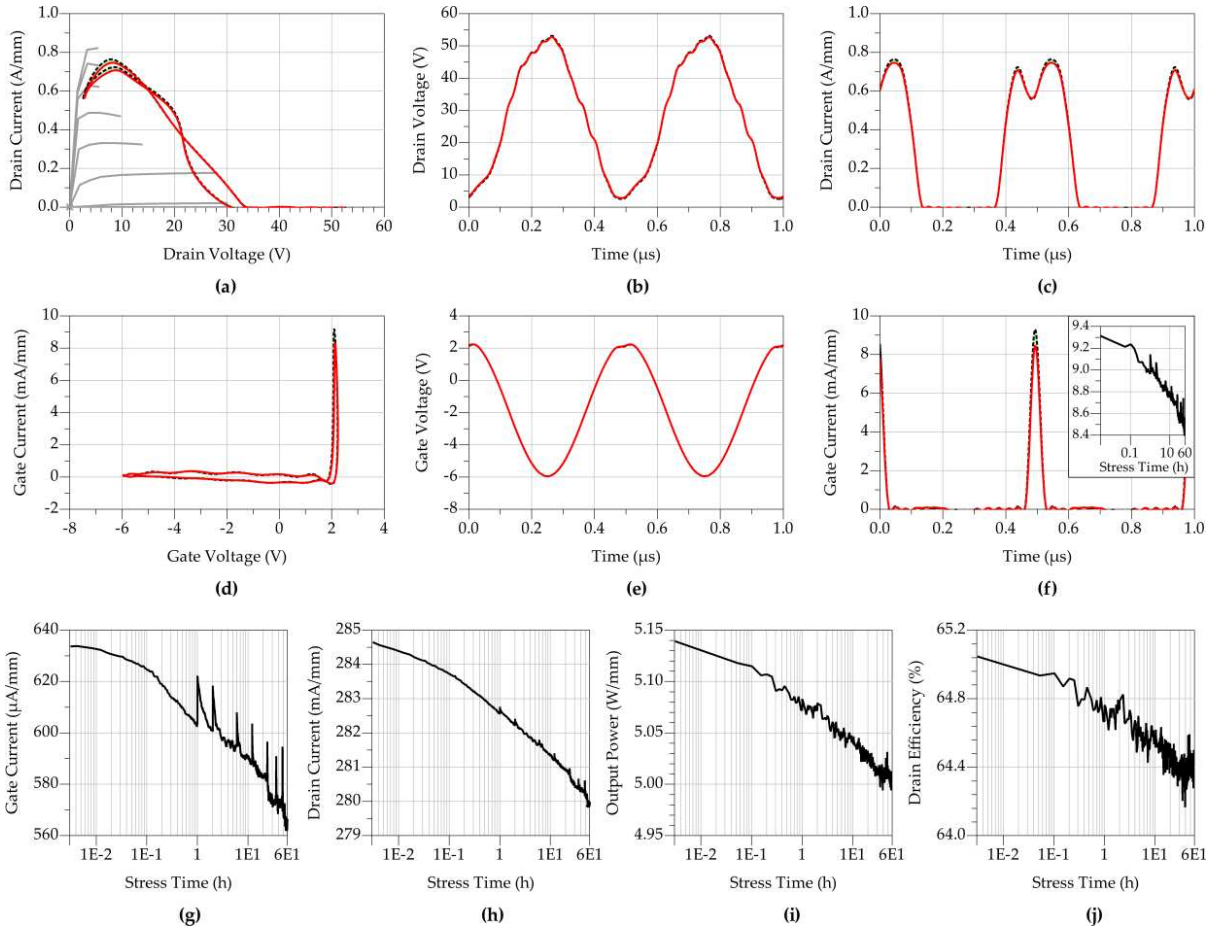

Figure 6. Stress measurement results for the 2 MHz tuned-load class-AB condition at 30 °C: (**a**) load lines vs. initial DC I/V characteristics (grey lines), (**b**) drain voltage waveforms, (**c**) drain current waveforms, (**d**) input loci, (**e**) gate voltage waveforms, (**f**) gate current waveforms with the evolution of its maximum instantaneous value in the inset, (**g**) average gate current, (**h**) average drain current, (**i**) output power, and (**j**) drain efficiency. From (**a**–**f**), the black dashed lines represent the initial state of the DUT, whereas the red continuous lines represent the final state of the DUT.

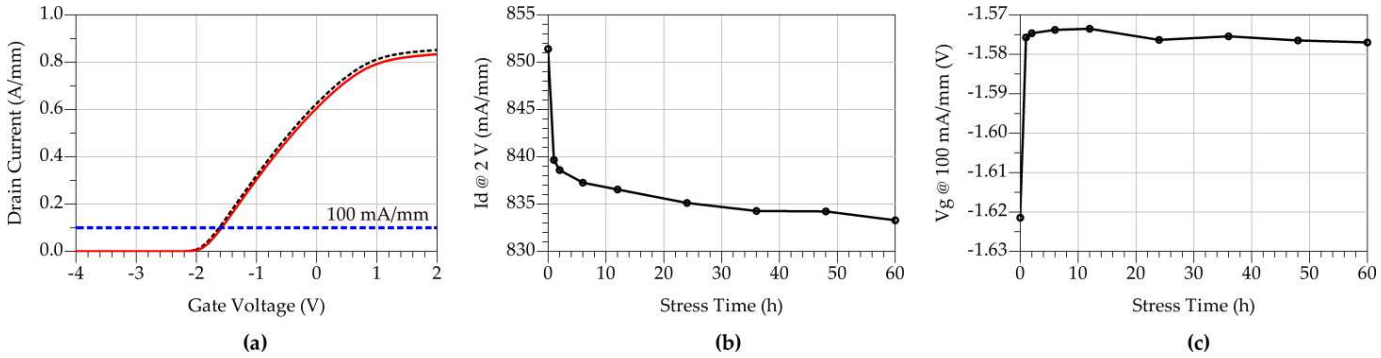

Figure 7. DC control measurements for the 2 MHz tuned-load class-AB condition at 30 °C: (**a**) I_D-V_G trans-characteristic measured before (black dashed line) and after (red continuous line) the stress, (**b**) saturated drain current at V_G = 2 V versus stress time, and (**c**) gate voltage for I_D = 100 mA/mm versus stress time.

5.2. Class-E Stress at 30 °C

As in the previous case, the class-E stress condition was applied to a new sample at 30 °C for a total of 60 h. We report the waveforms and the performance evolution

throughout the stress measurement in Figure 8. We can observe a slight variation of the load line (Figure 8a), this time due to a reduction in both the drain voltage and the drain current, whose peak value decreased from 86.7 V to 85.3 V (−1.6%), as illustrated in Figure 8b,c. This produces a reduction in the output power from 3.48 W/mm to 3.33 W/mm (−4.6%), and in the drain efficiency, from 67.7% to 66.0%, as shown in Figure 8i,j, respectively. In this case, the gate current was negligible throughout the entire experiment, since neither forward nor reverse conduction of the Schottky junction was present. Therefore, no significant change was observed in the input waveforms (Figure 8d–f). The evolution of the average currents over the stress time is also interesting. The average gate current was slightly positive but very small and became very noisy after approximately 0.1 h from the beginning of the measurement. The average drain current also exhibited a peculiar behavior. The largest variation appeared at the very beginning of the test, with a sharp decrease around 0.1 h. Then, it seemed to settle for 10 h, and to decrease again until the end of the measurement. It is interesting to observe that when the average drain current shows the faster variations, the average gate current becomes noisier, highlighting that the device behavior is changing due to some degradation mechanism.

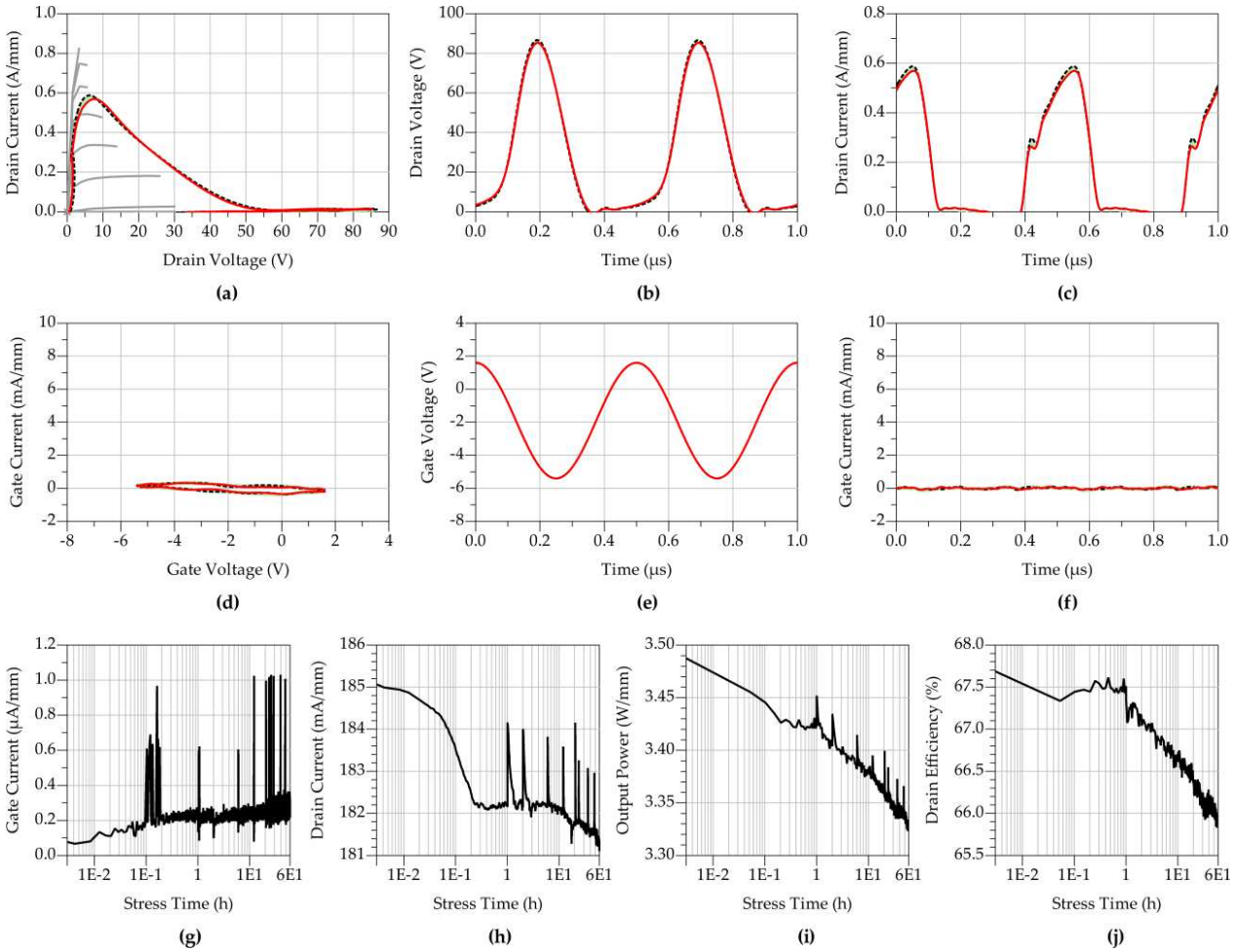

Figure 8. Stress measurement results for the 2 MHz class-E condition at 30 °C: (**a**) load lines vs. initial DC I/V characteristics (grey lines), (**b**) drain voltage waveforms, (**c**) drain current waveforms, (**d**) input loci, (**e**) gate voltage waveforms, (**f**) gate current waveforms, (**g**) average gate current, (**h**) average drain current, (**i**) output power, (**j**) and drain efficiency. From (**a**–**f**), the black dashed lines represent the initial state of the DUT, whereas the red continuous lines represent the final state of the DUT.

In Figure 9, we show the data collected from the DC control measurements executed in between stress sessions. The results show a similar trend to the previous ones, although the decrease in the DC drain current (from 866 mA/mm to 820 mA/mm, −5.3%) and the change in the device threshold seem more accentuated.

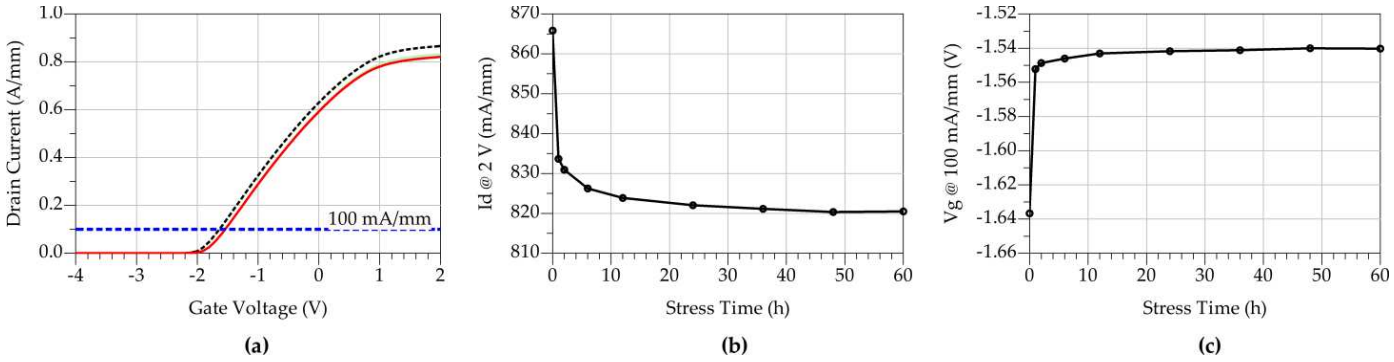

Figure 9. DC control measurements for the 2 MHz class-E condition at 30 °C: (**a**) I_D-V_G transcharacteristic measured before (black dashed line) and after (red continuous line) the stress, (**b**) saturated drain current at V_G = 2 V versus stress time, and (**c**) gate voltage for I_D = 100 mA/mm versus stress time.

5.3. Comparison of the Degradation Obtained at 30 °C

Some of the differences between the two investigated stress conditions have been already discussed. Nevertheless, we can now compare the level of degradation achieved by the devices after the stress tests.

Since the stress conditions are different, we will compare quantities normalized with respect to their initial values, also to compensate for some small process variations always present between samples, although very limited in our case. Therefore, the comparisons shown in Figure 10 are related to the relative percentage variation of various parameters, following the definition in Equation (1):

$$\Delta X_{\%} = 100 \cdot \frac{X(t) - X(0)}{X(0)} \tag{1}$$

where $X(t)$ represents the generic quantity X after a time t from the beginning of the stress experiment (t = 0 s).

From the data reported in Figure 10, the class-E operation produces a higher degradation of the device performance with respect to the class-AB condition in this first experiment. This suggests that the higher drain voltage reached by the class-E load line accelerates the degradation mechanisms. An interesting result confirming this phenomenon can be seen in the different trends of the average drain current (Figure 10b). For the class-E condition, the largest variation of the current appears within the first 20 min, whereas under class-AB the degradation appears more gradual throughout the stress.

Regarding the leakage gate current, one of the most important indicators of the device degradation, we observed a similar variation for both stress conditions. Here, the class-E condition seems less critical, although the measurements of this quantity were very noisy, and a conclusion based only on this parameter is not clear. This is highlighted also in Figure 11, where we compare the complete I-V characteristics measured before and after the stress measurement. By looking at the I_D-V_D characteristics, the global degradation seems negligible, thus suggesting that the effect of the applied stress is mainly related to the dynamic behavior of the transistors.

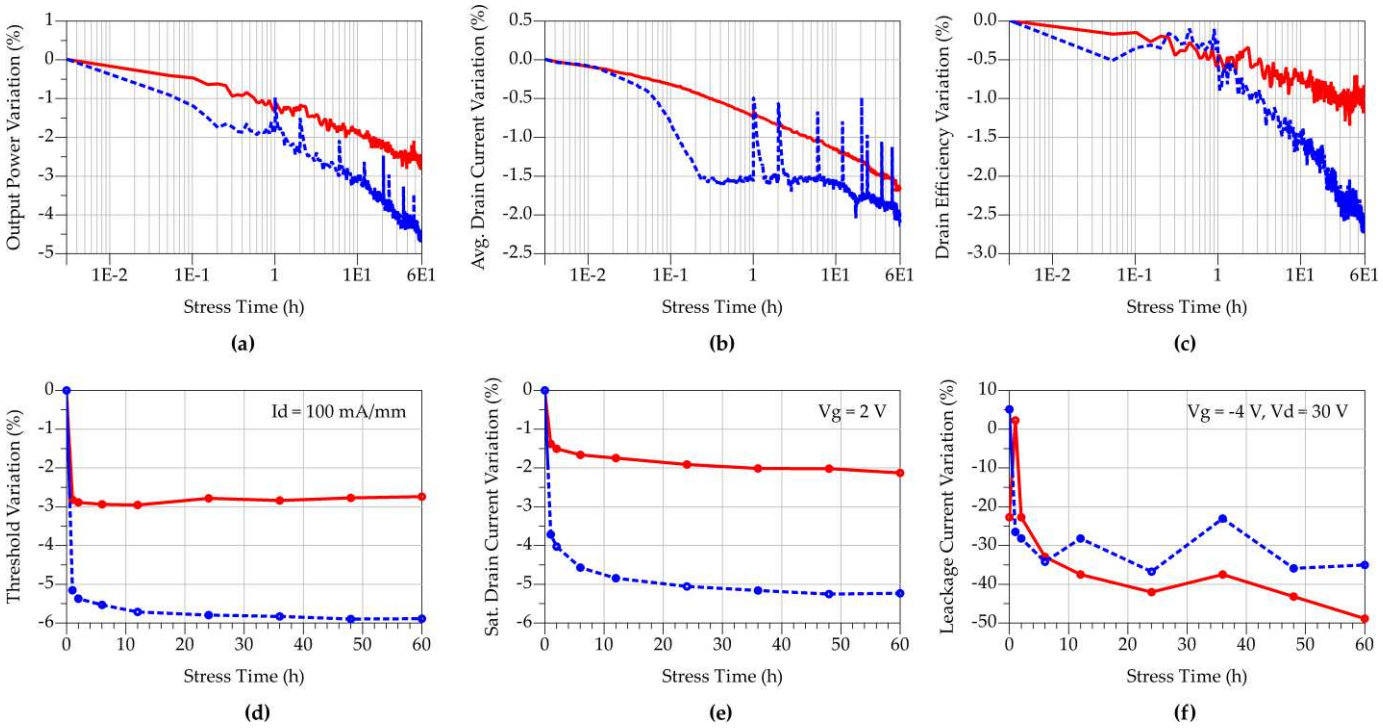

Figure 10. Comparison between the degradation achieved from the class-AB (red continuous lines) and the class-E (blue dashed lines) stress conditions. Variations, along 60 h of stress, of (**a**) output power, (**b**) average drain current, (**c**) drain efficiency, (**d**) threshold voltage at I_D = 100 mA/mm, (**e**) saturated drain current at V_G = 2 V and V_D = 4 V, and (**f**) gate leakage current at V_G = −4 V and V_D = 30 V.

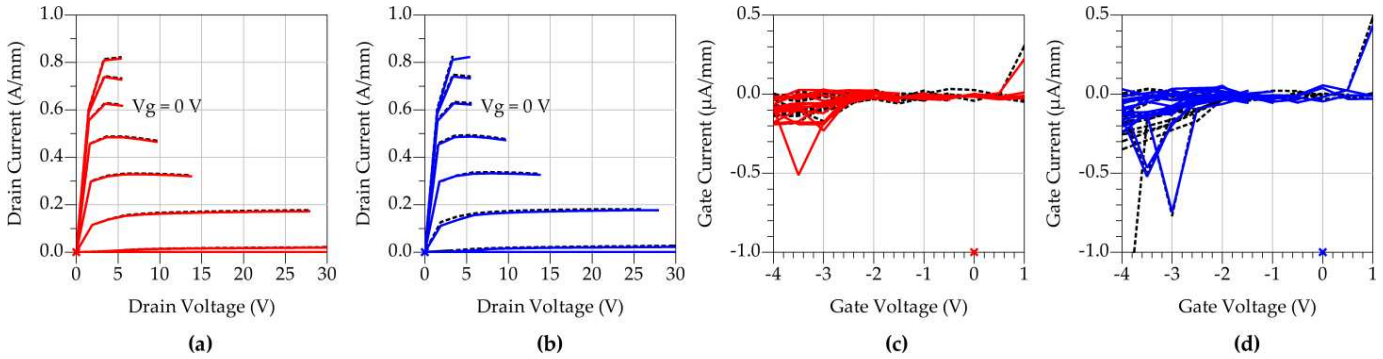

Figure 11. Complete I-V characteristics measured before (black dashed lines) and after (red and blue continuous lines) the 60 h stress. Data collected for the (**a**,**c**) class-AB stress and (**b**,**d**) class-E stress.

5.4. Tuned-Load Class-AB Stress at 100 °C

After the class-AB stress measurement at 30 °C was completed, it was repeated on the same device while raising the backside temperature to 100 °C. By doing this, we expected an acceleration in the degradation phenomena. The results of this characterization are reported in Figures 12 and 13. It is immediately visible that the drain current was lower as compared to the previous cases, which is expected because of the reduction of the carrier mobility due to the higher temperature. During the stress, the load line showed a bigger variation, leading to a reduction in the output power and drain efficiency, respectively from 4.80 W/mm to 4.55 W/mm (−5%) and from 63.6% to 62.0%, as illustrated in Figure 12i,j.

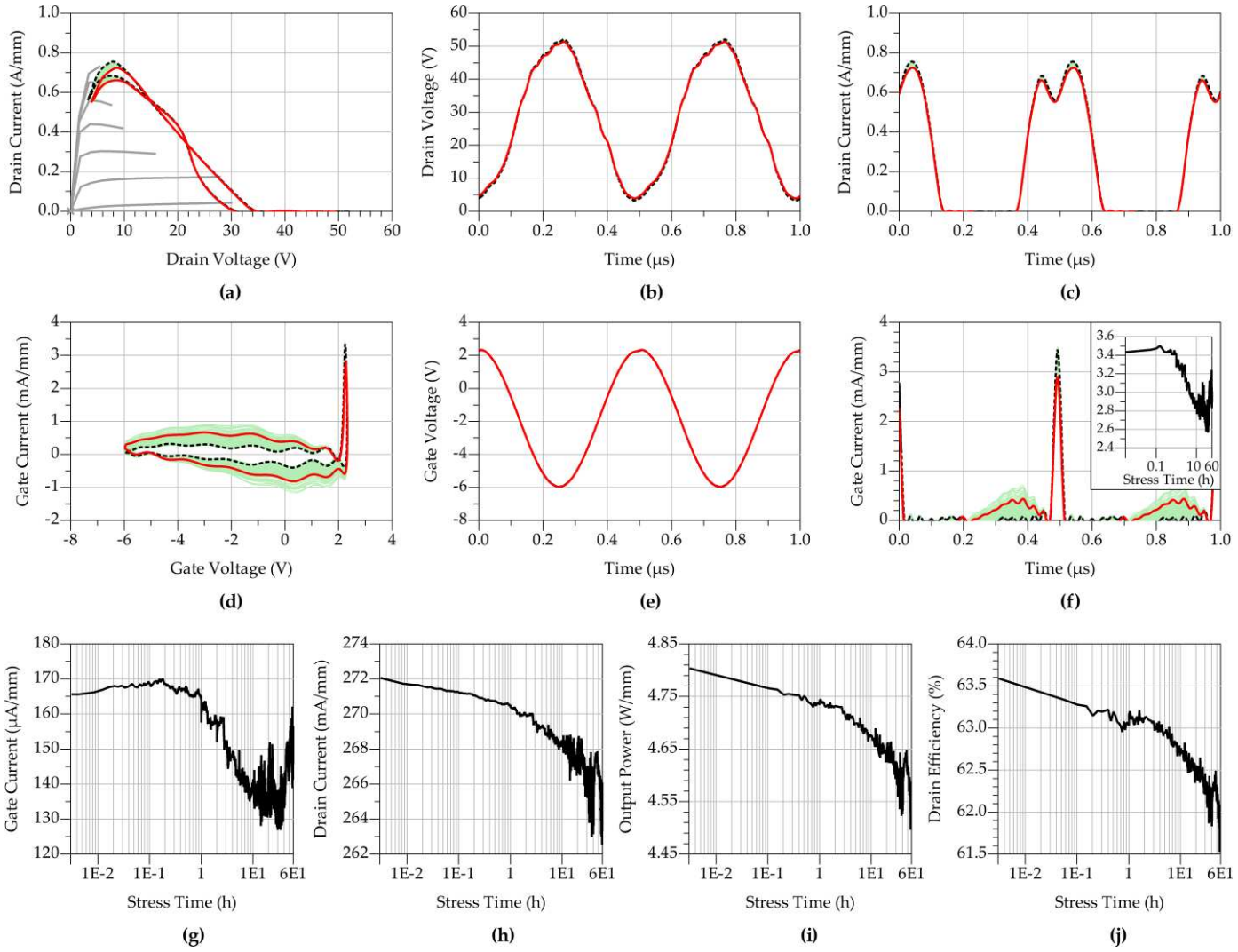

Figure 12. Stress measurement results for the 2 MHz tuned-load class-AB condition at 100 °C: (**a**) load lines vs. initial DC I/V characteristics (grey lines), (**b**) drain voltage waveforms, (**c**) drain current waveforms, (**d**) input loci, (**e**) gate voltage waveforms, (**f**) gate current waveforms with the evolution of its maximum instantaneous value in the inset, (**g**) average gate current, (**h**) average drain current, (**i**) output power, and (**j**) drain efficiency. From (**a**–**f**), the black dashed lines represent the initial state of the DUT, whereas the red continuous lines represent the final state of the DUT.

Interesting results can be seen in the behavior of the gate port. First, the maximum value of the gate current waveform was significantly reduced with respect to the 30 °C case, which was, again, expected because of the higher temperature. The peak on the current reduced with stress time from 3.4 mA/mm to 2.3 mA/mm (−15%), although it seemed to settle after 10 h (Figure 12f), which is confirmed by the data related to the average gate current (Figure 12g). We also note that, during the stress, the shape of the current waveform changed, and a small current appeared when the Schottky junction operated below its threshold. As the gate current is a good indicator of the degradation of the transistor, this clearly confirms that the state of the device changed. We also point out that this kind of variation would be unknown if the measurements were carried out at microwaves frequencies.

The data concerning the DC control measurements are presented in Figure 13. Again, we observed a reduction in the saturated drain current from 720 mA/mm to 690 mA/m (−4.2%, Figure 13b), whereas the device threshold voltage changes during the stress but after 60 h settles on approximately the same value measured before the stress.

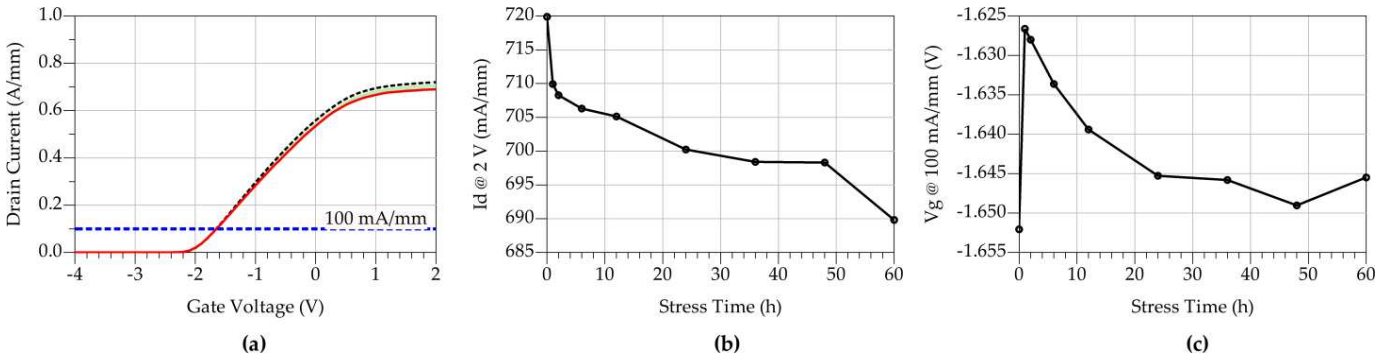

Figure 13. DC control measurements for the 2 MHz tuned-load class-AB condition at 100 °C: (**a**) I_D-V_G trans-characteristic measured before (black dashed line) and after (red continuous line) the stress, (**b**) saturated drain current at V_G = 2 V versus stress time, and (**c**) gate voltage for I_D = 100 mA/mm versus stress time.

5.5. Class-E Stress at 100 °C

The same experiment at 100 °C was carried out on the second device sample, already stressed under class-E operation at 30 °C. The results are reported in Figures 14 and 15. Looking at the waveforms reported in Figure 14, it is immediately evident that the status of the device changed less when compared to the previous measurement. The maximum drain voltage along the load line decreases from 84.7 V to 84.2 V (−0.6%). The output power goes from 3.45 W/mm before the stress to 3.36 W/mm after the stress (−0.3%), and, consequently, the drain efficiency reduces from 68.5% to 67.9%, as shown in Figure 14i,j, respectively.

No significant change was observed on the gate waveforms, where the gate current remained negligible throughout the entire experiment (Figure 14d–f). Looking at the small average gate current over the stress time (Figure 14g), we note very noisy data which became even noisier towards the end of the experiment, although on average they did not highlight any significant variation. The drain current instead has a behavior similar to the one observed at a lower temperature, with a sudden change around 0.1 h, a stable phase up to 5 h and then a more gradual decrease till the end of the experiment.

Figure 15 shows the results from the 100 °C DC control measurements, which have a similar trend with respect to the ones achieved at 30 °C, although the entity of the variations of the drain current (from 722 mA/mm to 705 mA/mm, −2.4%) and of the device threshold are more limited.

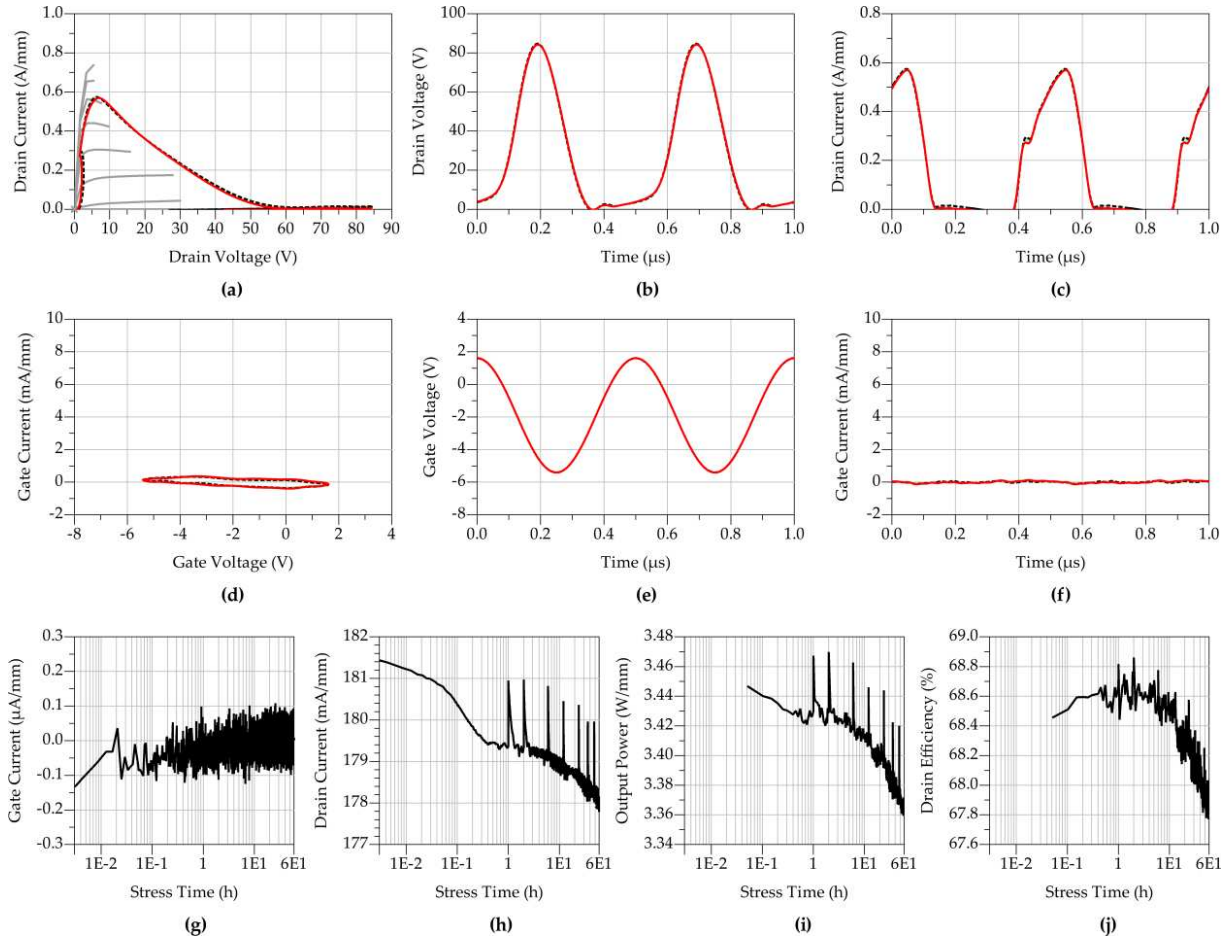

Figure 14. Stress measurement results for the 2 MHz class-E condition at 100 °C: (**a**) load lines vs. initial DC I/V characteristics (grey lines), (**b**) drain voltage waveforms, (**c**) drain current waveforms, (**d**) input loci, (**e**) gate voltage waveforms, (**f**) gate current waveforms, (**g**) average gate current, (**h**) average drain current, (**i**) output power, and (**j**) drain efficiency. From (**a**–**f**), the black dashed lines represent the initial state of the DUT, whereas the red continuous lines represent the final state of the DUT.

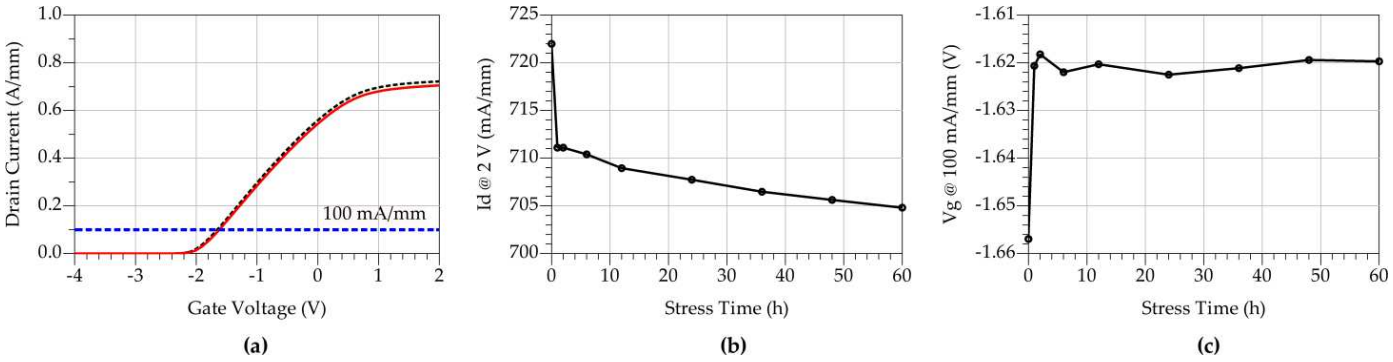

Figure 15. DC control measurements for the 2 MHz class-E condition at 100 °C: (**a**) I_D-V_G trans-characteristic measured before (black dashed line) and after (red continuous line) the stress, (**b**) saturated drain current at V_G = 2 V versus stress time, and (**c**) gate voltage for I_D = 100 mA/mm versus stress time.

5.6. Comparison of the Degradation Obtained at 100 °C

Following the same approach adopted in Section 5.3, we will now compare the level of degradation obtained from the two operating conditions at 100 °C.

Looking at the results presented in Figure 16, in this case the class-AB operation is the one that provides a higher degradation of the device performance. All the reported parameters, including the gate leakage current, show how the performance of the class-E condition remains more stable and produces a lower alteration of the device behavior also under DC operation. This kind of result suggests that the thermal state of the device is the dominant factor in the degradation mechanisms and therefore, in this context, the class-AB operation is unfavorable compared to class-E condition, because of the higher power dissipation.

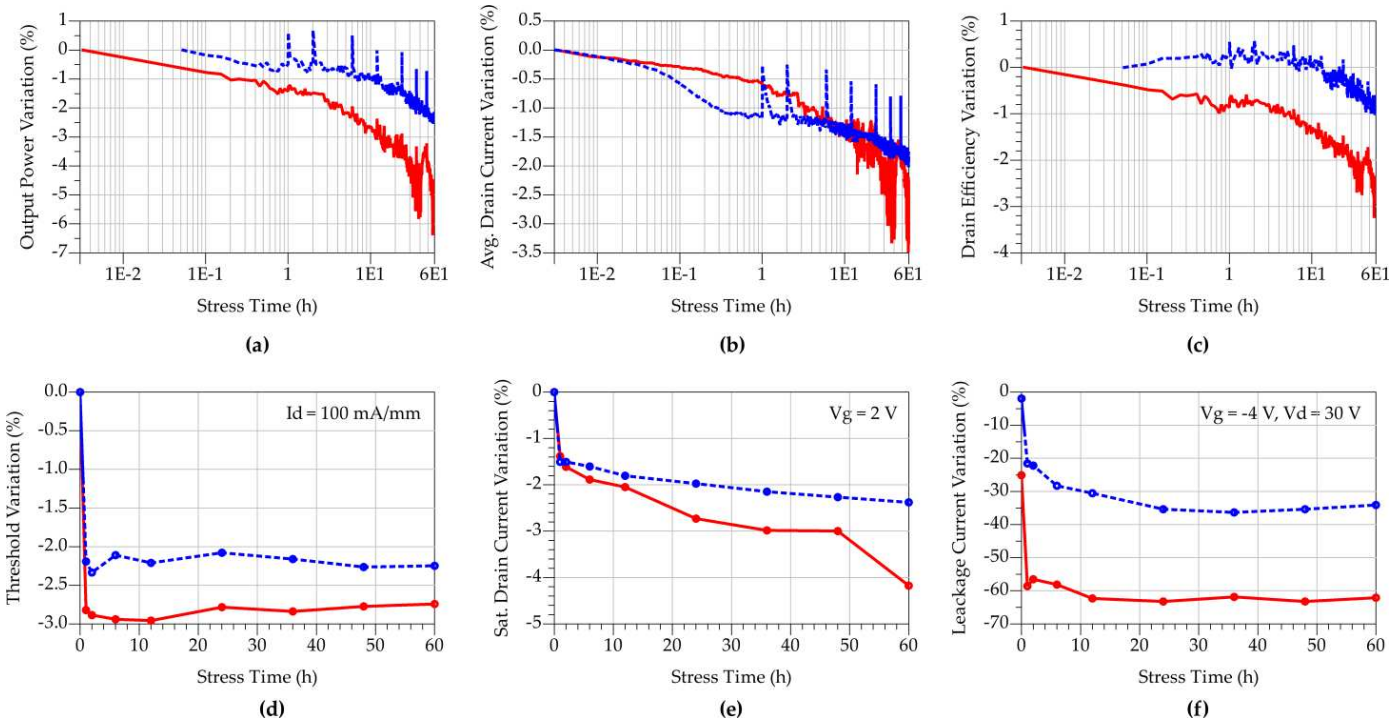

Figure 16. Comparison between the degradation achieved from the class-AB (red continuous lines) and the class-E (blue dashed lines) stress conditions. Variations, along 60 h of stress of (**a**) output power, (**b**) average drain current, (**c**) drain efficiency, (**d**) threshold voltage at I_D = 100 mA/mm, (**e**) saturated drain current at V_G = 2 V and V_D = 4 V, and (**f**) gate leakage current at V_G = −4 V and V_D = 30 V.

We report the complete I-V characteristics measured before and after the stress measurement in Figure 17. Again, these results confirm the previous observations, with the class-AB case showing the largest variation in the DC characteristics. In this case, the different levels of degradation achieved by the two conditions were clearly visible on the gate leakage current, which experienced the biggest variation (−62% vs. −32%) when the device operated under saturated class AB.

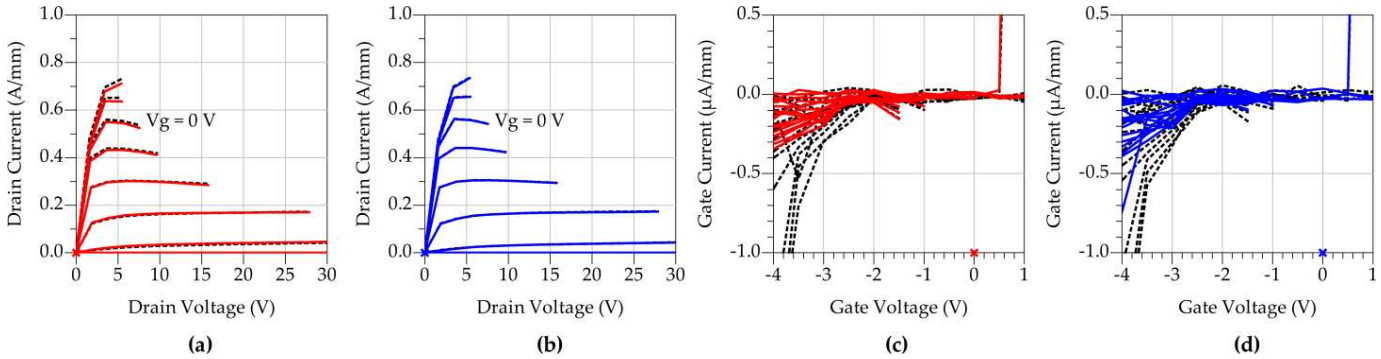

Figure 17. Complete I-V characteristics measured before (black dashed lines) and after (red and blue continuous lines) the 60 h stress. Data collected for the (**a**,**c**) class-AB stress and (**b**,**d**) class-E stress.

6. Conclusions

In this paper, we investigated how a realistic power amplifier operating condition can impact on the performance degradation of a GaN HEMT microwave devices. We compared the effects of a saturated class-AB condition and a high-efficiency class-E condition by means of stress experiments carried out using a low-frequency load-pull system. The thorough comparison of the experimental results clearly shows that:

1. The level of degradation reached by the device under test depends on the actual RF operating condition adopted for the stress experiment. This confirms the need for realistic stress tests to understand what specific degradation mechanisms can impact on the active device when used in actual applications and estimate its realistic lifetime.
2. Thermal degradation effects, magnified by the saturated class-AB condition, are more critical than the effects due to high fields, and dominant when the active device was operated under class-E condition.
3. The developed characterization methodology and the achieved experimental findings can be used to accurately and deeply investigate the degradation and failure mechanisms affecting microwave technology to enhance its performance and robustness for realistic operation in practical microwave applications.

Author Contributions: Conceptualization, G.B. and A.R.; methodology, G.B. and A.R.; software, G.B.; validation, G.B., A.R. and V.V.; formal analysis, G.B., A.R. and V.V.; investigation, G.B. and A.R.; resources, A.R. and R.G.; data curation, G.B.; writing—original draft preparation, G.B. and A.R.; writing—review and editing, V.V., R.G., G.C. and G.V.; supervision, A.R. and G.V.; project administration, A.R.; funding acquisition, A.R. and G.V. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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