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Analysis of Efficiency-Limiting Factors Resulting from Transistor Current Source on Class-F and Inverse Class-F Power Amplifiers

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SUMMARY This paper describes the efficiency-limiting factors resulting from transistor current source in the case of class-F and inverse class-F (F^{-1}) operations under saturated region. We investigated the influence of knee voltage and gate-voltage clipping behaviors on drain efficiency as limiting factors for the current source. Numerical analysis using a simplified transistor model was carried out. As a result, we have demonstrated that the limiting factor for class- F^{-1} operation is the gate-diode conduction rather than knee voltage. On the other hand, class-F PA is restricted by the knee voltage effects. Furthermore, nonlinear measurements carried out on a GaN HEMT validate our analytical results.
key words: HEMTs, microwave amplifiers, harmonics, waveform engineering.

1. Introduction

High-efficiency power amplifiers (PAs) play a very important role in modern microwave and millimeter-wave systems. Among them, class-F and inverse class-F (F^{-1}) PAs are intensively studied [1]-[10]. Previously, class- F^{-1} operation was strongly limited by the transistor breakdown voltage, because the maximum drain voltage of class- F^{-1} is 1.5 times larger than that of class-F operation. GaN high electron-mobility transistor (HEMT) resolves this limitation thanks to its high breakdown voltage based on the excellent material properties.

Although many papers have reported high-efficiency class-F and class- F^{-1} PAs investigating knee voltage effects [11]-[15], relatively few studies have demonstrated the significance of input voltage shaping and its relationship with the knee voltage, especially under saturated operation. Theoretically, an ideal class-F PA requires a squared drain-voltage waveform and a half-sinusoidal drain-current waveform [16]-[18]. In contrast, ideal class- F^{-1} PA requires exchanged output waveforms with respect to class-F ones, i.e., a half-sinusoidal drain-voltage waveform and a squared drain-current waveform [19]. In order to realize proper class- F^{-1} operation, Cipriani et al. [3], [20] and other authors [21]-[24] showed that a quasi-squared current waveform can be obtained by means of a sinusoidal input-voltage

sufficiently large to reach transistor saturated operation. However, the influence of gate junction characteristics on drain efficiency has not been investigated.

Since the input voltage and the knee voltage are strongly related to the current source of a transistor, an accurate evaluation of the drain-current source is essential for improving the efficiency of the PA. Recently, a time-domain measurement setup working at low frequency (LF) was proposed [25]-[28]. This characterization method enables RF characteristics such as output power and drain efficiency to be accurately evaluated as well as dynamic load lines under realistic large-signal operation to be observed.

In this paper, we focus on the efficiency-limiting factors resulting from the transistor current source under class-F and class- F^{-1} operations in a saturated power region. We investigated the influence of the knee voltage effects and the gate-voltage clipping due to the forward conduction of gate junction on drain efficiency. Simulation was carried out by using a simplified transistor model with a gate-voltage clipping behavior, where the gate junction is modeled with a diode as shown in Fig. 1. Class-F and class- F^{-1} amplifiers are numerically compared in terms of optimum load impedance and drain efficiency under saturated operating condition. As a result, we have demonstrated that the class- F^{-1} PA efficiency performance is restricted by the gate-diode forward current. Moreover, gate-diode characteristics generate higher harmonics of gate voltage which results in voltage waveform shaping. On the other hand, class-F PA is limited by the knee voltage effects. Vector nonlinear LF measurements performed on a GaN HEMT empirically support our analytical results.

2. Analysis for Saturated Operation of Class-F and Class- F^{-1} PAs using a Simplified Model

In this section, we investigate the knee of the drain voltage and the clipping behavior of the gate voltage by numerical analysis. In order to investigate such effects, we used a simplified device model implementing two gate-voltage clipping behaviors: nonlinear transconductance and gate-diode characteristics. The former defines drain current clipping due to both lower bound (threshold voltage of current flowing) and upper bound (gate voltage obtaining maximum drain current). The latter defines the gate-

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Schottky-diode characteristics as shown in Fig. 1. The numerical comparison is made between class-F and class-F⁻¹ operating conditions under saturated operation.

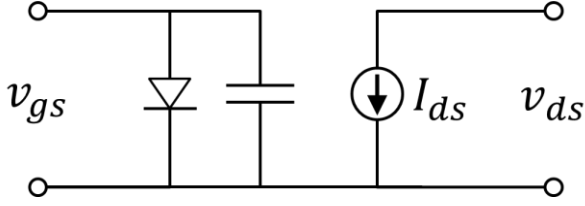


Fig. 1 Simplified transistor model including gate diode.

2.1 Simplified Model Implementing Gate-Voltage Clipping Behavior

As a starting point, we adopted Cripps's simple transistor model [29], which includes knee voltage effect. Since this model does not include gate-clipping behavior, we took this effect into account by modifying the drain-current expression (I_{ds}) as follows:

$$I_{ds} = I_{max} \left(1 - \exp\left(-\frac{v_{ds}}{V_k}\right) \right) f(v_{gs}) \quad (1)$$

where I_{max} is the maximum drain current, and v_{ds} and v_{gs} are the drain-source and gate-source voltages, respectively. The knee-voltage parameter (V_k) is defined as a drain voltage at which the drain current is reduced to 63% of its saturated value $I_{max} f(v_{gs})$. The function $f(v_{gs})$ determines the normalized piece-wise linear transconductance (I_{ds} vs. v_{gs}) profile, which is defined by

$$f(v_{gs}) = \begin{cases} 0, & v_{gs} < V_{th} \\ (v_{gs} - V_{th}) / (V_{gsmax} - V_{th}), & V_{th} \leq v_{gs} \leq V_{gsmax} \\ 1, & V_{gsmax} < v_{gs} \end{cases} \quad (2)$$

where V_{th} and V_{gsmax} are the threshold and maximum gate voltages, respectively.

In addition to the transconductance characteristics, the following gate-Schottky-diode characteristics were also incorporated into the model:

$$I_{gs} = \begin{cases} 0, & v_{gs} \leq V_{gsmax} \\ I_0 (\exp((v_{gs} - V_0)q/kT) - 1), & V_{gsmax} < v_{gs} \end{cases} \quad (3)$$

where I_0 and V_0 are model parameters.

Hereafter, we consider the normalized condition for simplicity, i.e., $I_{max} = V_{gsmax} = I_0 = V_0 = 1$ and $V_{th} = 0$. Figure 2 shows the drain current associated to the simplified transistor model at $V_k = 0.3$. For large-signal analysis, we performed harmonic balance simulation. A schematic used for simulation is shown in Fig. 3. Table 1 summarizes

impedance terminate conditions for the simulations. Harmonics were calculated up to the 20th order for both the input and output sides.

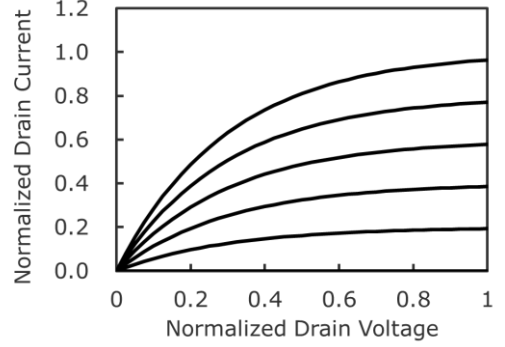


Fig. 2 I_{ds} - V_{ds} characteristics of the simplified model ($V_k = 0.3$).

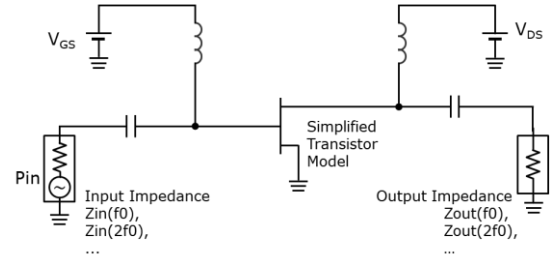


Fig. 3 Schematic used for harmonic-balance simulations

Table 1 Impedance terminate conditions for simulation

		Class-F	Class-F ⁻¹
Output	fundamental frequency f ₀	2 Ω	
	2f ₀ , 4f ₀	Short	Open
	3f ₀ , 5f ₀	Open	Short
	6f ₀ to 20f ₀	50 Ohms	
Input	f ₀ to 20f ₀	50 Ohms	

2.2 Effects of Gate Voltage Clipping on Class-F⁻¹ PAs

As mentioned previously, two different kinds of voltage clipping behaviors can be incorporated into the model. First, we performed harmonic-balance simulation using our simplified model implementing only the effect in (2) under class-F⁻¹ operation. For such a class, even harmonic impedances (2nd and 4th) are open terminated, and odd harmonic impedances (3rd and 5th) are short terminated, as shown in Table 1. Source impedances including higher harmonics were fixed at 50 Ohms throughout the analysis. Normalized input power is defined as the power injected (i.e., available) into the input of the DUT under the input impedance shown in Table 1. Figure 4(a) shows the drain efficiency and gate current versus normalized input power (P_{in}) at V_k of 0.2 and 0.3, for a normalized output impedance of 2 and a class-B gate bias. Next, we conducted simulations using our model including both the effects in (2) and (3), as shown in Fig. 4(b).

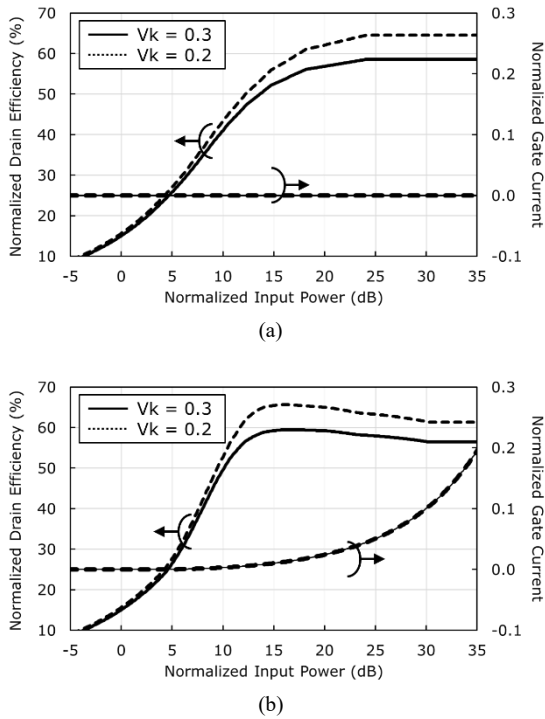


Fig. 4 Simulated drain efficiency and gate current of the class- F^{-1} PA: (a) the model implementing only the clipping effect in (2), (b) the model implementing both clipping effects in (2) and (3).

Figure 4(a) confirms the expected results from theory, that is, drain efficiency monotonically increases with input power and reaches efficiency limit restricted by the knee voltage effects. Obviously, the gate current never flows because the model does not include diode characteristics. In contrast, gate-current flowing is observed when the input power increases as shown in Fig. 4(b), when we take into account the gate-diode characteristics. As a consequence of the gate-current flowing, drain efficiency slightly decreases at saturated operating condition. More interestingly, higher drain efficiency is obtained at lower input power (around $P_{in} = 15$ dB) when the gate-diode characteristics are taken into account.

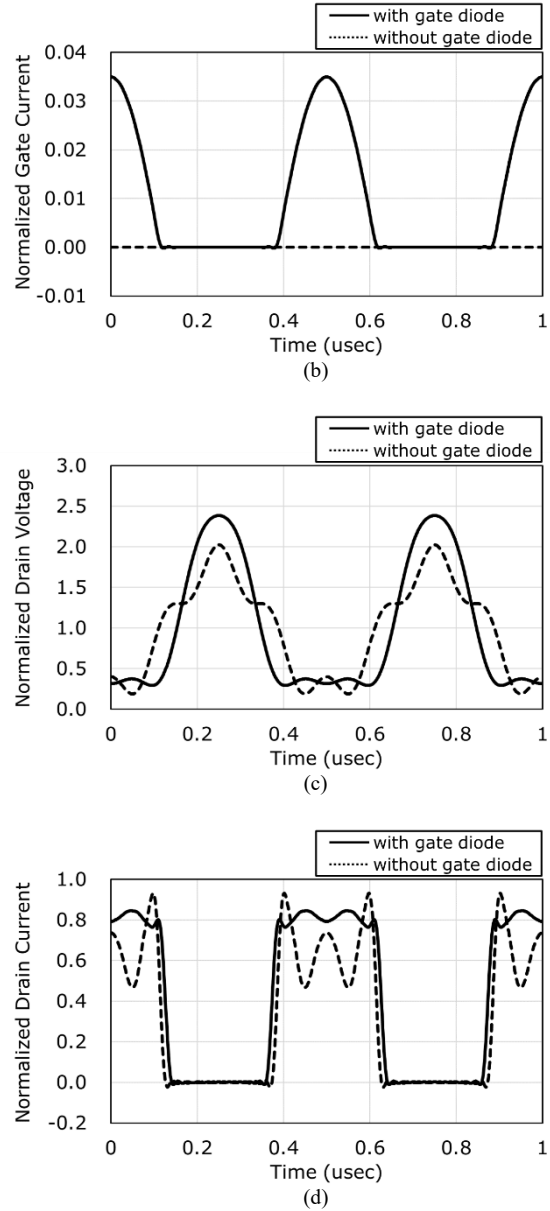
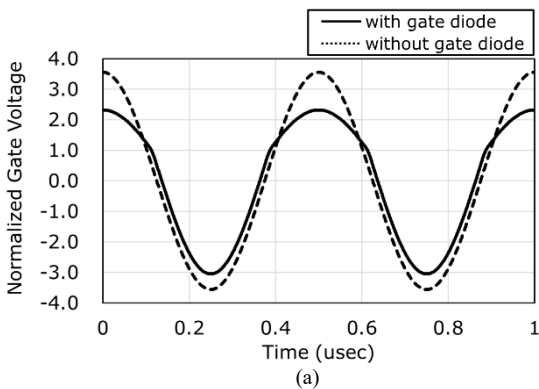


Fig. 5 Simulated waveforms of the class- F^{-1} operation at a normalized $P_{in} = 15$ dB: (a) the normalized gate voltage, (b) the normalized gate current, (c) the normalized drain voltage, (d) the normalized drain current.

In order to investigate these differences, we analyzed input and output waveforms. Figure 5 illustrates normalized waveforms simulated at a normalized $P_{in} = 15$ dB and $V_k = 0.3$. We clearly found that the gate voltage is clipped if the gate diode is implemented as shown in Fig. 5(a). Several studies have reported the improvement of class- F^{-1} PA efficiency by controlling input harmonic impedances [20]-[24]. Although input harmonic impedances are not intentionally tuned in our simulation, gate-diode characteristics generate higher harmonics of gate-voltage which result in voltage waveform shaping. Since drain current is amplified by the transconductance (g_m) with respect to gate voltage, the drain current is rectangularly shaped by the harmonics included in the gate voltage. We

found that the simulated maximum gate-voltage reached V_{gsmax} in Eq. (3) at $P_{in} = 3.9$ dB. Therefore, the gate voltage clipping occurs, if P_{in} is greater than 3.9 dB.

In practical terms, the drain efficiency of the model with the gate diode is 59.2%, which is higher than that (i.e., 52.5%) of the model without gate diode at $P_{in} = 15$ dB. The maximum drain efficiencies of the model with and without the gate diode are 59.5% and 58.6%, respectively. However, it must be observed that from the reliability point of view, the limitation of forward gate-current is determined by various reliability tests. If the gate current limitation is relatively severe, the attainable maximum drain efficiency will decrease.

2.3 Effects of Gate Voltage Clipping on Class-F PAs

In the same manner as the investigation of the class-F⁻¹ PA, we performed harmonic-balance simulations using our simplified model implemented without (Fig. 6(a)) and with gate diode (Fig. 6(b)) under class-F operation. For such a class, even harmonic impedances (2nd and 4th) are short terminated, and odd harmonic impedances (3rd and 5th) are open terminated, as shown in Table 1.

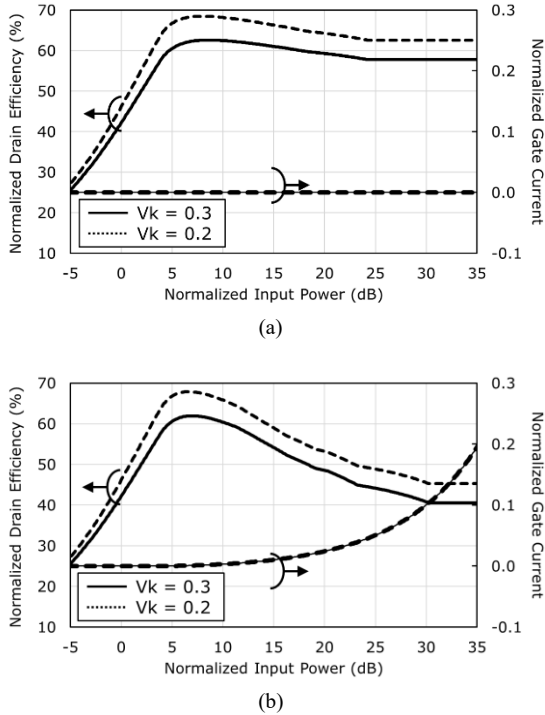


Fig. 6 Simulated drain efficiency and gate current of the class-F PA: (a) the model implementing only the clipping effect in (2), (b) the model implementing both clipping effects (2) and (3).

Unlike the class-F⁻¹ PA, the maximum value of drain efficiency does not change regardless of gate-diode implementation as shown in Fig. 6. Moreover, Fig. 7

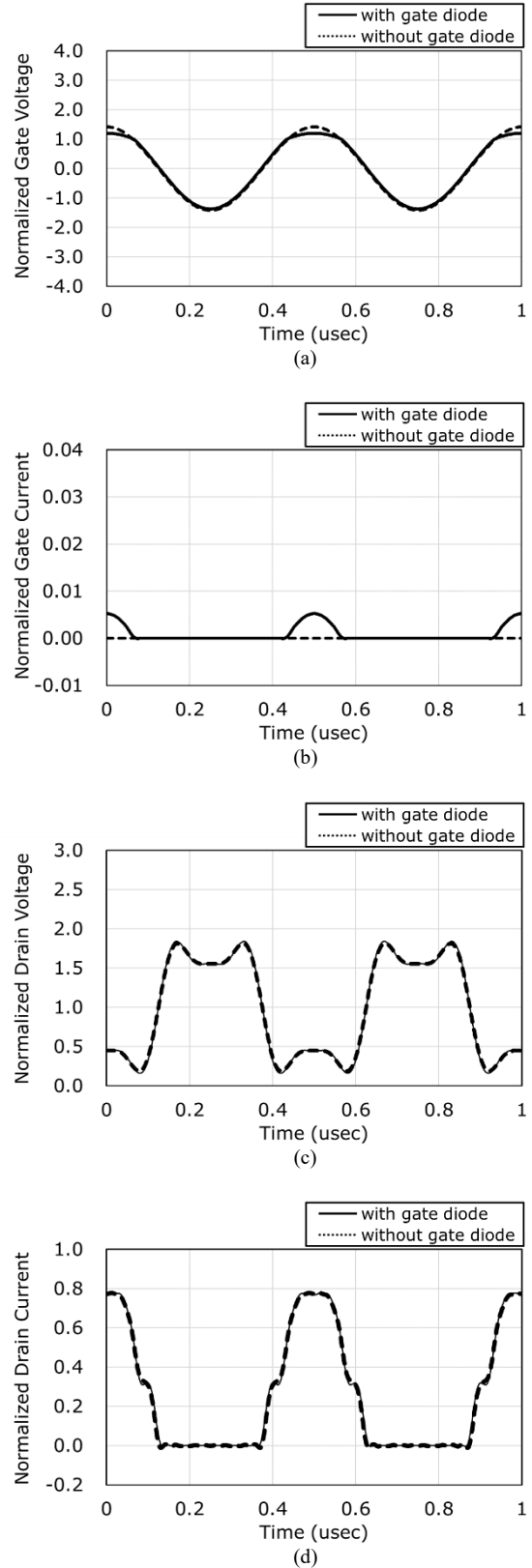


Fig. 7 Simulated waveforms of the class-F operation at a normalized $P_{in} = 7$ dB: (a) the normalized gate voltage, (b) the normalized gate current, (c) the normalized drain voltage, (d) the normalized drain current.

illustrates normalized gate-voltage waveforms simulated at a normalized $P_{in} = 7$ dB (where the efficiency maximum is obtained) and $V_k = 0.3$. We found that the gate voltage is not clipped enough to generate higher harmonics even if the gate diode is implemented. Therefore, class-F PA efficiency performance is restricted by the knee voltage effects. This justifies why efficiency improvement of class-F PA is mainly manipulated with output harmonic impedances [3].

3. Validation by Nonlinear Measurements

In order to validate the previous analysis, LF measurements were performed on a GaN HEMT, whose gate periphery is 1 mm and gate length is $0.60 \mu\text{m}$ [30]. We adopted the LF measurement setup presented in [28]. In a few megahertz measurements, the measured reference plane is located at almost the same position as located at the intrinsic reference plane of the device. More precisely, resistive parasitic elements are present but they can be easily de-embedded. In addition, since at such frequency all the nonlinear dynamic effects associated to the intrinsic capacitances are negligible, the LF measurements allow for a direct characterization of the intrinsic drain-current source. Since device performances are deeply related to the current source, LF measurements allow for an accurate evaluation of gate-voltage clipping and knee voltage effects of transistors.

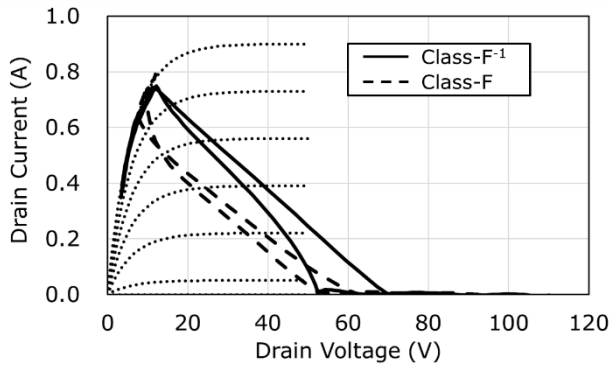


Fig. 8 Measured load line in saturated region with the optimum impedance for output power under class-F operation (dashed line, 108Ω for the load impedance) and class-F⁻¹ operation (solid line, 155Ω for the load impedance). Dotted lines indicate I_{ds} -curve obtained by the simplified model.

Figure 8 shows the measured load line under class-F⁻¹ (solid line) and class-F operation (dashed line). The operating frequency is 2 MHz. In this case the measurements were carried out with a quiescent drain current (I_{d0}) of 0.5 mA and a quiescent drain voltage (V_{d0}) of 50 V. Input and output harmonics were acquired up to 15th order. The load line is obtained in saturated region with the optimum impedance for output power (i.e., 155Ω for class-F⁻¹ and 108Ω for class-F). We also adjusted the parameters of our simplified model and show the associated I_{ds} curve (dotted lines in Fig. 8).

Figure 9 shows measured gate-voltage waveforms

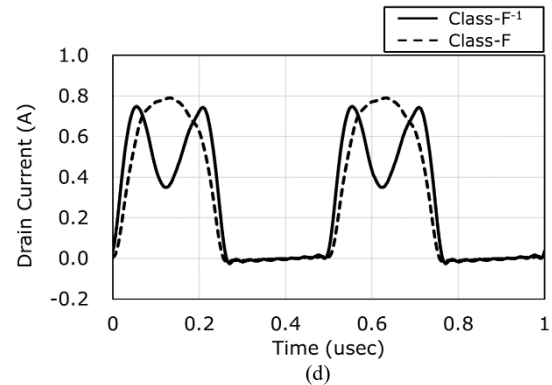
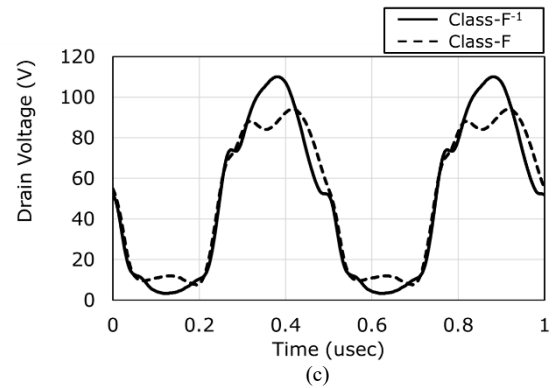
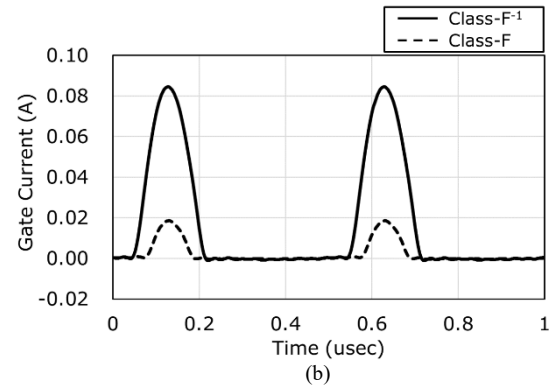
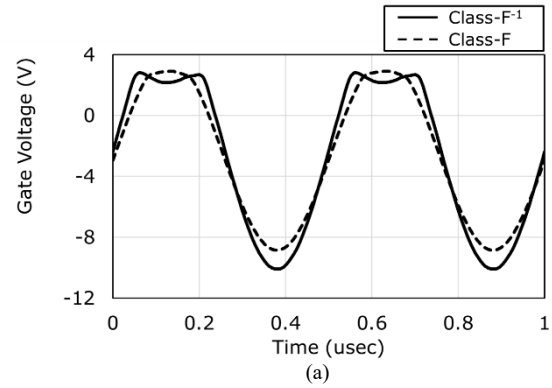


Fig. 9 Measured waveforms under class-F operation (dashed line) and class-F⁻¹ operation (solid line): (a) gate voltage, (b) gate current, (c) drain voltage, (d) drain current. Load impedances are the ones considered in Fig. 8.

under class-F and class-F⁻¹ obtained at the same condition in Fig. 8. As we have previously confirmed in Figs. 5 and 7, gate-voltage clipping is clearly observed under class-F⁻¹ operation in contrast to class-F operation. Similarly, as seen in Fig. 5, the drain current is reshaped by the clipped gate voltage.

Figure 10 reports measured drain efficiency as a function of the load impedance under class-F and class-F⁻¹. In this case, the amplitude of the input incident signal is also swept in order to reach saturated output power and efficiency under the limitation of maximum average gate current of 20 mA.

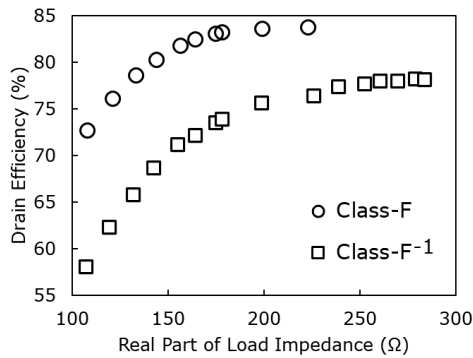


Fig. 10 Measured drain efficiency as a function of load impedance.

Similar to the measurements, we performed simulation under the limitation of maximum average gate current of 20 mA. Figure 11 shows simulated results of drain efficiency by using the extracted model whose I/V characteristics are reported in Fig. 8. As shown in these figures, the simplified model is in good agreement with the experimental characterization in Figure 10 when the gate-current limitation is taken into account.

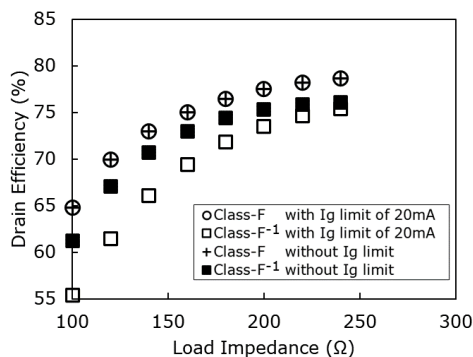


Fig. 11 Simulated drain efficiency as a function of load impedance.

In order to further clarify the limiting factor of the gate current associated to transistor reliability, we performed simulation without the gate current limitation, which are also shown in Figure 11. For the class-F⁻¹ PA, the efficiency improves when the gate current limitation is not considered, while no change in efficiency was observed in the class-F PA. Hence, the class-F⁻¹ PA is restricted by the maximum

gate currents, whereas the class-F PA is restricted by the knee voltage effects. As a result, the LF measurements on a GaN HEMT support our analytical results.

Needless to say, for high-frequency PAs, influence of reactive components (e.g., nonlinear gate capacitance) of transistor should be also taken into an account.

4. Conclusions

In this paper, we describe the efficiency-limiting factors resulting from current source in case of class-F and class-F⁻¹ operations under saturated regime. We investigated the influence of the knee-voltage effects and the gate-voltage clipping due to the gate-diode characteristics on GaN HEMT drain efficiency. Numerical analysis was carried out using a simplified transistor model with a gate-voltage clipping behavior. Class-F and class-F⁻¹ amplifiers are numerically compared in terms of load impedance and drain efficiency under saturated operating condition. As a result, we have demonstrated that the limiting factor for the class-F⁻¹ operation is the gate-diode current rather than knee voltage. Moreover, the gate-diode characteristics generate higher harmonics of gate voltage which results in gate voltage and drain current waveform shaping. On the other hand, the class-F PA performance is limited by the knee voltage effects. Finally, nonlinear LF measurements carried out on a GaN HEMT definitely assess our analytical results.

Acknowledgments

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